XM25RU512D DATASHEET

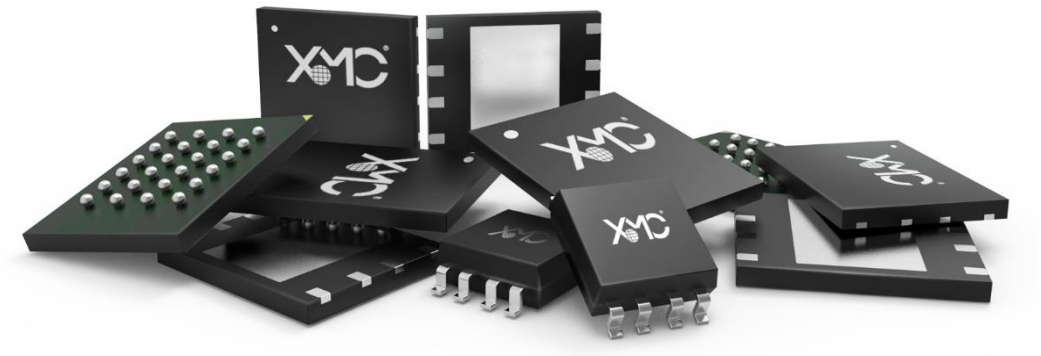


TABLE OF CONTENTS

1 FEATURES 5
2 GENERAL DESCRIPTIONS 6
3 ORDERING INFORMATION 7
4 BLOCK DIAGRAM 8
5 CONNECTION DIAGRAMS 9
5.1 CONNECTION DIAGRAMS 9
6 PIN DESCRIPTIONS 12
6.1 Chip Select (/CS) 12
6.2 Serial Data Input, Output and IOs (SI, SO and IO0, IO1, IO2, IO3) 12
6.3 Write Protect (/WP) 12
6.4 HOLD (/HOLD) 12
6.5 Serial Clock (CLK) 12
6.6 Reset (/RESET) 12
7 FUNCTIONAL DESCRIPTIONS 13
7.1 SPI Operation 13
7.1.1 Standard SPI Instructions 13
7.1.2 Dual SPI Instructions 13
7.1.3 Quad SPI Instructions 14
7.2 3-Byte / 4-Byte Address Modes 14
7.3 Hold Function 15
7.4 Software Reset & Hardware /RESET pin 15
7.5 Write Protection 16
7.5.1 Write Protect Features 16
7.6 RPMC OPERATIONS 17
7.6.1 RPMC Initialization 17
7.6.2 RPMC Operation Flow 18
7.6.3 Operations Allowed / Disallowed During RPMC Operation 18
7.6.4 RPMC Status Register Definition 19
8 STATUS AND CONFIGURATION REGISTERS 20
8.1 Status Registers 20
8.1.1 Erase/Write in Progress (BUSY) - Status Only 20
8.1.2 Write Enable Latch (WEL) – Status Only 20
8.1.3 Block Protect Bits (BP3, BP2, BP1, BP0) – Volatile/Non-Volatile Writable 21
8.1.4 Top/Bottom Block Protect (TB) – Volatile/Non-Volatile Writable 21
8.1.5 Complement Protect (CMP) – Volatile/Non-Volatile Writable 21
8.1.6 Status Register Protect (SRP, SRL) – Volatile/Non-Volatile Writable 21
8.1.7 Erase/Program Suspend Status (SUS) – Status Only 22
8.1.8 Security Register Lock Bits (LB3, LB2, LB1) – Volatile/Non-Volatile OTP Writable 22
8.1.9 Quad Enable (QE) – Volatile/Non-Volatile Writable 23
8.1.10 Current Address Mode (ADS) – Status Only 23
8.1.11 Power-Up Address Mode (ADP) – Non-Volatile Writable 23
8.1.12 WPSEL – Non-Volatile Writable 23
8.1.13 Output Driver Strength (DRV1, DRV0) – Volatile/Non-Volatile Writable 24
8.1.14 /HOLD or /RESET Pin Function (HOLD/RESET) – Volatile/Non-Volatile Writable 24

8.1.15 Dummy Cycle Bits 24
8.1.16 Reserved Bits – Non Functional 24
8.2 Extended Address Register – Volatile Writable Only 27
9 INSTRUCTIONS 28
9.1 Device ID and Instruction Set Tables 28
9.1.1 Manufacturer and Device Identification 28
9.1.2 Instruction Set Table 1 (Standard/Dual/Quad SPI Instructions)(1) 29
9.1.3 Instruction Set Table 2 (Standard/Dual/Quad SPI Instructions,3-Byte Address Mode) 30
9.1.4 Instruction Set Table 6 (Standard/Dual/Quad SPI Instructions, 4-Byte Address Mode)(1) 31
9.1.5 Instruction Set Table 5 (Dual/Quad SPI Instructions, 4-Byte Address Mode) 33
9.1.6 Instruction Set Table 2-1 (RPMC Input Instruction, OP1)(1) 35
9.1.7 Instruction Set Table 2-2 (RPMC Output Instruction, OP2) (1) 35
9.2 Instruction Descriptions 36
9.2.1 Write Enable (06h) 36
9.2.2 Write Enable for Volatile Status Register (50h) 36
9.2.3 Write Disable (04h) 37
9.2.4 Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h) 37
9.2.5 Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h) 38
9.2.6 Read Extended Address Register (C8h) 39
9.2.7 Write Extended Address Register (C5h) 40
9.2.8 Enter 4-Byte Address Mode (B7h) 40
9.2.9 Exit 4-Byte Address Mode (E9h) 41
9.2.10 Read Data (03h) 41
9.2.11 Read Data with 4-Byte Address (13h) 42
9.2.12 Fast Read (0Bh) 42
9.2.13 Fast Read with 4-Byte Address (0Ch) 42
9.2.14 Fast Read Dual Output (3Bh) 44
9.2.15 Fast Read Dual Output with 4-Byte Address (3Ch) 45
9.2.16 Fast Read Quad Output (6Bh) 46
9.2.17 Fast Read Quad Output with 4-Byte Address (6Ch) 47
9.2.18 Fast Read Dual I/O (BBh) 48
9.2.19 Fast Read Dual I/O with 4-Byte Address (BCh) 49
9.2.20 Fast Read Quad I/O (EBh) 50
9.2.21 Fast Read Quad I/O with 4-Byte Address (ECh) 51
9.2.22 Word Read Quad I/O (E7h) 53
9.2.23 Set Burst with Wrap (77h) 56
9.2.24 Page Program (02h) 57
9.2.25 Page Program with 4-Byte Address (12h) 58
9.2.26 Quad Input Page Program (32h) 59
9.2.27 Quad Page Program (33h) 60
9.2.28 Quad Input Page Program with 4-Byte Address (34h) 61
9.2.29 Sector Erase (20h) 62
9.2.30 Sector Erase with 4-Byte Address (21h) 62
9.2.31 32KB Block Erase (52h) 63
9.2.32 32KB Block Erase with 4-Byte Address (5Ch) 64
9.2.33 64KB Block Erase (D8h) 65

9.2.34 64KB Block Erase with 4-Byte Address (DCh) 65
9.2.35 Chip Erase (C7h / 60h) 66
9.2.36 Erase / Program Suspend (75h) 66
9.2.37 Erase / Program Resume (7Ah) 67
9.2.38 Power-down (B9h) 68
9.2.39 Release Power-down / Device ID (ABh) 69
9.2.40 Read Manufacturer / Device ID (90h) 70
9.2.41 Read Manufacturer / Device ID Dual I/O (92h) 71
9.2.42 Read Manufacturer / Device ID Quad I/O (94h) 72
9.2.43 Read Unique ID Number (4Bh) 73
9.2.44 Read JEDEC ID (9Fh) 74
9.2.45 Read SFDP Register (5Ah) 75
9.2.46 Erase Security Registers (44h) 86
9.2.47 Program Security Registers (42h) 87
9.2.48 Read Security Registers (48h) 88
9.2.49 Enable Reset (66h) and Reset Device (99h) 89
9.2.50 Ultra-Deep Power-Down (79H) 90
9.2.51 Exit Ultra-Deep Power-Down 91
9.2.52 Write Root Key Register (9Bh + 00h) 92
9.2.53 Update HMAC Key (9Bh + 01h) 93
9.2.54 Increment Monotonic counters (9Bh + 02h) 94
9.2.55 Request Monotonic counters (9Bh + 03h) 95
9.2.56 Reserved RPMC Commands (9Bh + 04h~FFh) 96
9.2.57 Read RPMC Status / Data (96h) 96
10 ELECTRICAL CHARACTERISTICS 97
10.1 Absolute Maximum Ratings (1)(2) 97
10.2 Operating Ranges 97
10.3 Power-Up Power-Down Timing and Requirements (1) 97
10.4 DC Characteristics 99
10.5 AC Measurement Conditions(1) 100
10.6 AC Characteristics(5) 101
10.7 Serial Input Timing 103
10.8 Serial Output Timing 103
10.9 Resume to Suspend Timing Diagram 103
10.10 DQS Output Timing (STR) 103
11 PACKAGE INFORMATION 104
11.1 SOP 300 16L (Package K) 104
11.2 WSON 6×8 8L (Package X) 105
12 REVISION HISTORY 106

1 FEATURES

- **New Family of SPI Flash Memories**
  - XM25RU512D: 512M-bit / 64-byte
  - Standard SPI: CLK, /CS, SI, SO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO0, IO1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO0, IO1, IO2, IO3
- **High Speed Clock Frequency**
  - 133 MHz Single, Dual/Quad SPI clocks
  - Configurable dummy cycle number for fast read operation
  - More than 100,000 erase/program cycles
  - More than 20-year data retention
  - Burst Read with 8/16/32/64 Byte Wrap
- **Efficient "Continuous Read"**
  - Continuous Read with 8/16/32/64-Byte Wrap
  - Allows true XIP (execute in place) operation
- **High Performance Program/Erase speed**
  - Page Page program time: 0.25ms typical
  - Sector erase time: 25ms typical
  - 32KB Block erase time 80ms typical
  - 64KB Block erase time 120ms typical
  - Chip erase time: 60 seconds typical
- **Single Power Supply Voltage**
  - Full voltage range: 1.65-2.0V
- **Low Power Consumption**
  - 20 µA typical standby current
  - 5 µA typical deep power down current
  - 10 mA typical active read current (108MHz Quad I/O)
- **Flexible Architecture with 4KB Sectors**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 byte per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Top/Bottom, Complement array protection
  - 128-Bit Unique ID for each device
  - Support Serial Flash Discoverable Parameters (SFDP) signature
  - 3 sets of OTP lockable 2048-Byte security pages
  - Volatile & Non-volatile Status Register Bits
  - Replay Protection Monotonic Counter (RPMC)
- **Space Efficient Packaging**
  - SOP 300mil 16L
  - WSON 8x6mm 8L
  - Contact XMC for KGD and other options

Note:

When ECC is enabled, it is required to program minimum one or multiple aligned 16-Byte granularities. Every aligned 16-Byte granularity should only be programmed once before Erase to ensure correct ECC operations.

2 GENERAL DESCRIPTIONS

The XM25RU512D (512M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25RU series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 1.65V to 2.0V power supply with current consumption as low as 1μA for deep power-down. All devices are offered in space- saving packages.

The XM25RU512D array is organized into 262,144 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The XM25RU512D has 16,384 erasable sectors and 1,024 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See Figure 1.)

The XM25RU512D support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI. SPI clock frequencies of up to 133MHz are supported allowing equivalent clock rates of 266MHz for Dual I/O and 532MHz for Quad I/O when using the Fast Read Dual/Quad I/O instructions. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 128-bit Unique Serial Number and three 2048-bytes Security Registers.

The XM25RH series is also equipped with an enhanced authentication security feature by Replay Protection Monotonic Counter (RPMC). It provides a high level secured communication between the flash device and the controller to reduce the system vulnerabilities to hardware attacks.

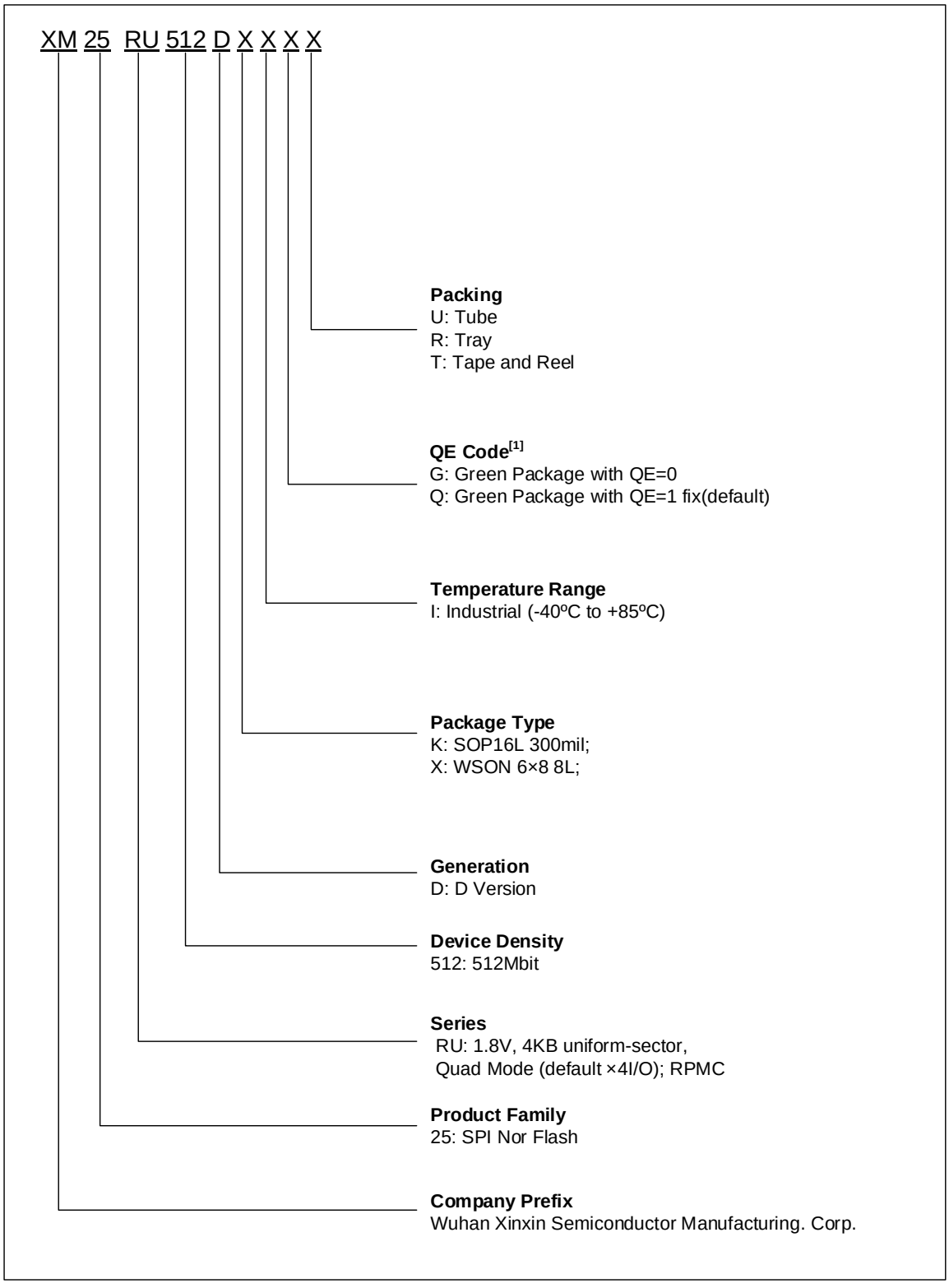
Read performance Comparison Table

Numbers of Dummy Cycles	Fast Read (0BH) (MHZ)	Fast Read Dual Output (3BH) (MHZ)	Fast Read Quad Output (6BH) (MHZ)	Fast Read Dual I/O (BBH) (MHZ)	Word Read Quad I/O (E7H) (MHZ)	Fast Read Quad I/O (EBH) (MHZ)
4	-	-	-	80*	80*	80
6	-	-	-	-	-	133*
8	133*	133*	133*	133*	133*	133*
10	-	-	-	-	-	133*

Notes: ** mean default status.*

3 ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following:



Note [1]. “Q” & “G” default “Dedicate reset open and DQS disable.

4 BLOCK DIAGRAM

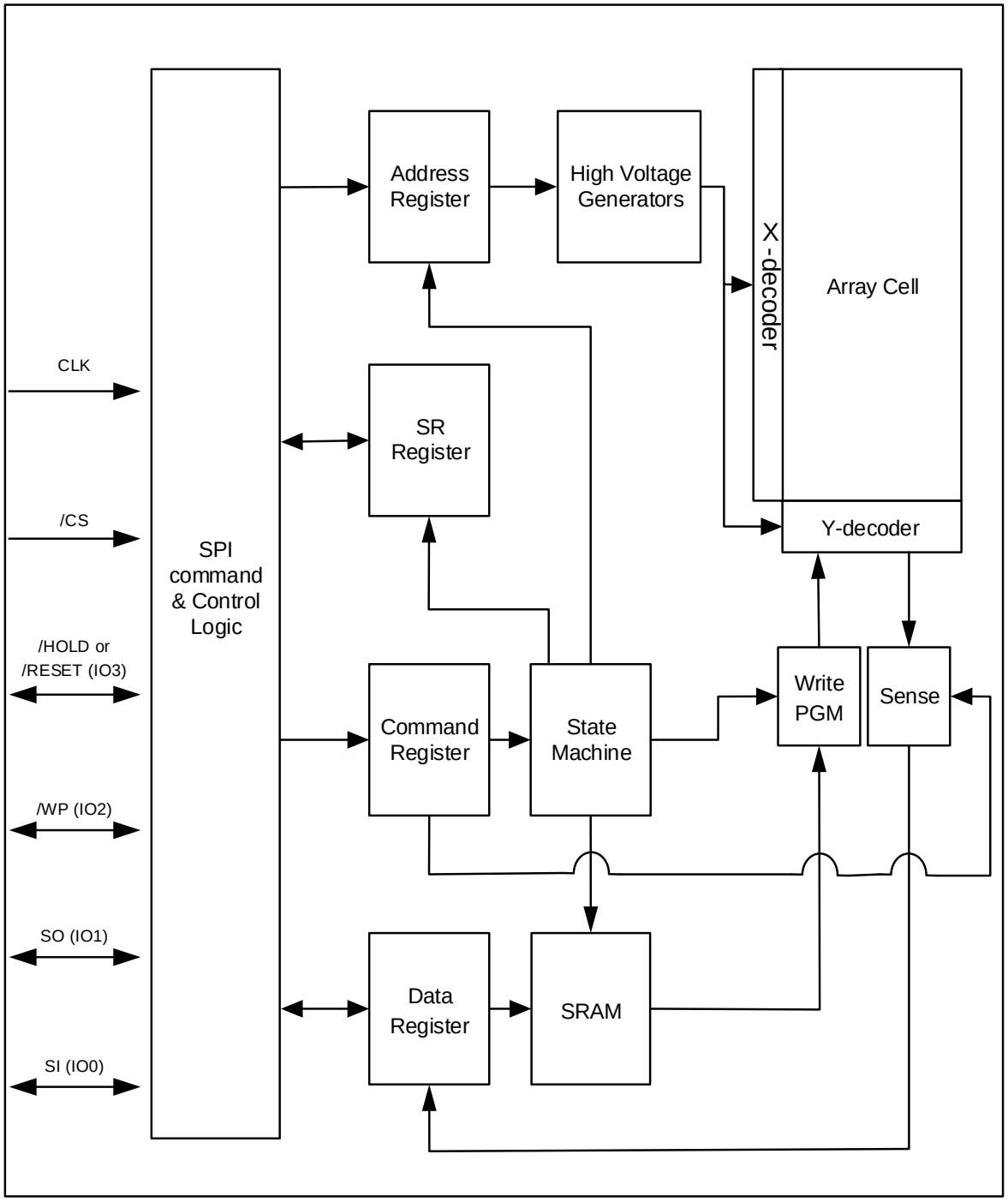


Figure 4-1 XM25RU512D Serial Flash Memory Block Diagram

5 CONNECTION DIAGRAMS

5.1 CONNECTION DIAGRAMS

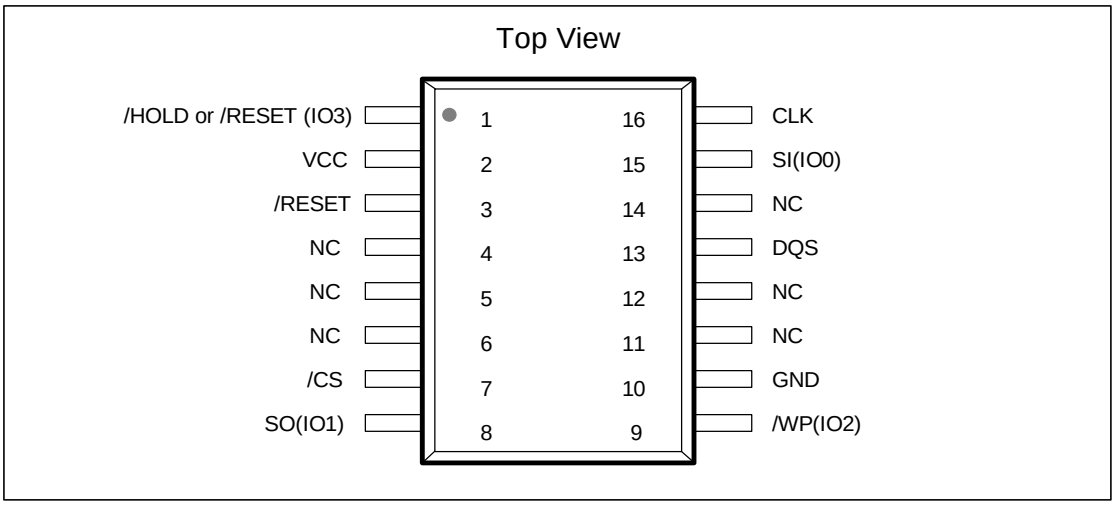


Figure 5-1 16-pin SOP 300mil 16L (Package Code K)

● PIN DESCRIPTION

Table 1. Pin Description for SOP16 Package

Pin No.	Pin Name	I/O	Description
1	/HOLD or /RESET (IO3)	I/O	HOLD or RESET input (Data Input Output 3) [2]
2	VCC		Power Supply
3	/RESET	I	Reset Input
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	SO (IO1)	I/O	Data Output (Data Input Output 1) [1]
9	/WP(IO2)	I/O	Write Protect Input (Data Input Output 2) [2]
10	GND		Ground
11	N/C		No Connect
12	N/C		No Connect
13	DQS	O	Data Strobe Signal Output
14	N/C		No Connect
15	SI (IO0)	I/O	Data Input (Data Input Output 0) [1]
16	CLK	I	Serial Clock Input

Notes:

[1] IO0 and IO1 are used for Standard and Dual SPI instructions.

[2] IO0 – IO3 are used for Quad SPI instructions, /HOLD (or /RESET) function is only available for Standard/Dual SPI.

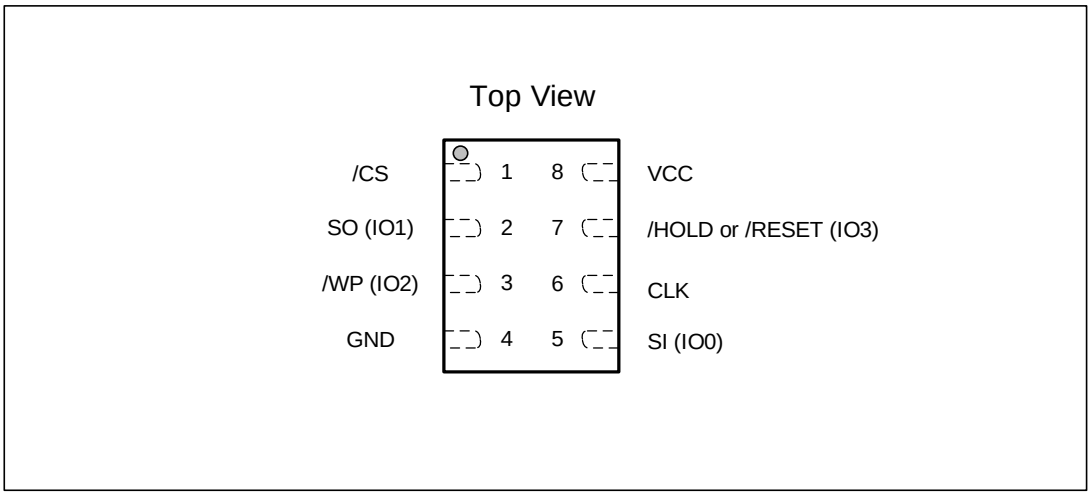


Figure 5-2. 8-pin WSON (Package Code X)

● PIN DESCRIPTION

Table 2. Pin Description for WSON8 Package

Pin No.	Pin Name	I/O	Description
1	/CS	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1) [1]
3	/WP(IO2)	I/O	Write Protect Input (Data Input Output 2) [2]
4	GND		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0) [1]
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	HOLD or RESET input (Data Input Output 3) [2]
8	VCC		Power Supply

Notes:
[1] IO0 and IO1 are used for Standard and Dual SPI instructions;
[2] IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI

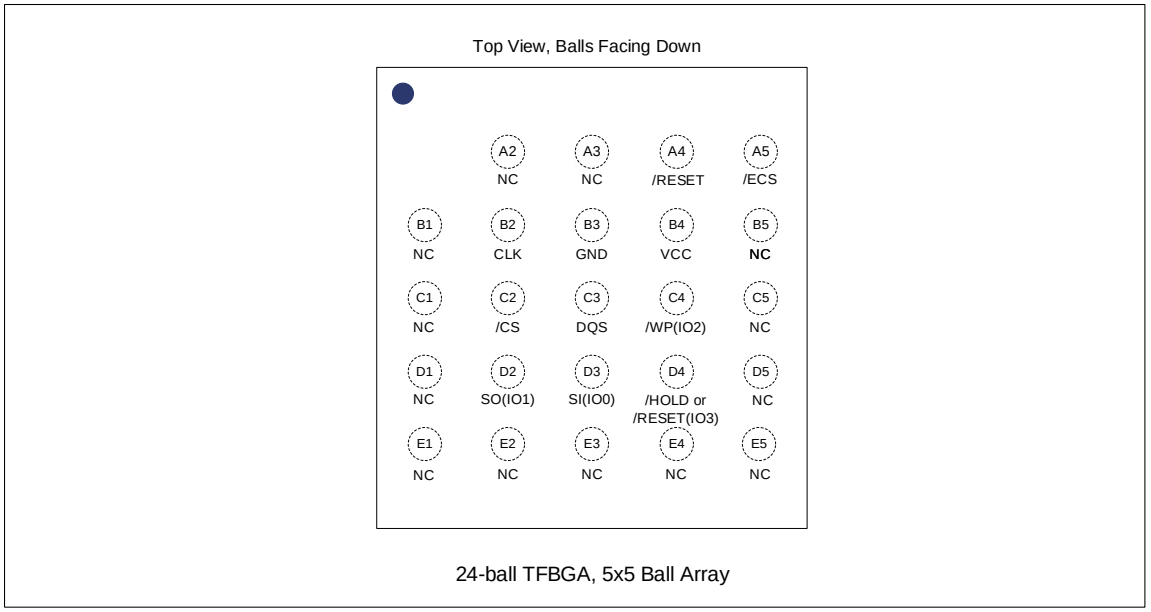


Figure 5-3 TFBGA 6x8 24ball (Package Code B2, 5x5 ball array)

● PIN DESCRIPTION

Table 3. Pin Description for TFBGA 6x8 (5x5 ball array)

Pin No.	Pin Name	I/O	Description[3]
A4	/RESET	I	Reset Input
A5	/ECS	O	ECC Correction Signal
B2	CLK	I	Serial Clock Input
B3	GND		Ground
B4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C3	DQS	O	Data Strobe Signal Output
C4	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2) [2]
D2	SO (IO1)	I/O	Data Output (Data Input Output 1) [1]
D3	SI (IO0)	I/O	Data Input (Data Input Output 0)[1]
D4	/HOLD or /RESET (IO3)	I/O	HOLD or RESET input (Data Input Output 3) [2]

Note:
[1] IO0 and IO1 are used for Standard and Dual SPI instructions;
[2] IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.
[3] /CS must be driven high if chip is not selected. Please don't leave /CS floating any time after power is on.

6 PIN DESCRIPTIONS

6.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (SO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (see “Write Protection” and Figure 59). Note that there was an internal pull-up resister on the /CS pin to achieve this.

6.2 Serial Data Input, Output and IOs (SI, SO and IO0, IO1, IO2, IO3)

The XM25RU512D supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional SI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional SO (output) to read data or status from the device on the falling edge of CLK. Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

6.3 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register’s Block Protect (CMP, TB, BP, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2. See Figure 2.1a-d for the pin configuration of Quad I/O operation. Note that there was an internal pull-up resistor on the /WP pin to avoid accidentally trigging WP function by pin floating.

6.4 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the SO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /HOLD pin function is not available since this pin is used for IO3. See Figure 2.1a-d for the pin configuration of Quad I/O operation. Note that there was an internal pull-up resistor on the /HOLD pin to avoid accidentally trigging HOLD function by pin floating.

6.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

6.6 Reset (/RESET)

The /RESET pin allows the device to be reset by the controller. For 8-pin packages, when QE=0, the IO3 pin can be configured either as a /HOLD pin or as a /RESET pin depending on Status Register setting. When QE=1, the /HOLD or /RESET function is not available for 8-pin configuration. Note that there was an internal pull-up resistor on the /RESET pin to avoid accidentally trigging /RESET function by pin floating.

7 FUNCTIONAL DESCRIPTIONS

7.1 SPI Operation

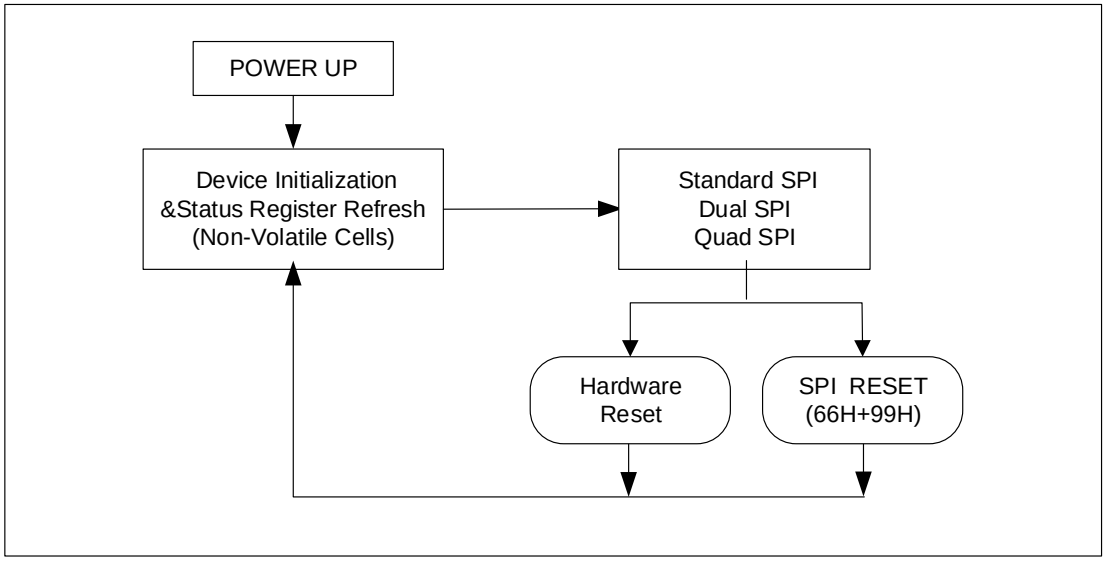


Figure 7-1 XM25RU512D Serial Flash Memory Operation Diagram

7.1.1 Standard SPI Instructions

The XM25RU512D is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (SO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The SO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

7.1.2 Dual SPI Instructions

The XM25RU512D supports Dual SPI operation when using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These instructions allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read instructions are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non- speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions, the SI and SO pins become bidirectional I/O pins: IO0 and IO1

7.1.3 Quad SPI Instructions

The XM25RU512D supports Quad SPI operation when using instructions such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)”, and”Word Read Quad I/O (E7h)”. These instructions allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read instructions offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instructions the SI and SO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non- volatile Quad Enable bit (QE) in Status Register-2 to be set.

7.2 3-Byte / 4-Byte Address Modes

The XM25RU512D provides two Address Modes that can be used to specify any byte of data in the memory array. The 3-Byte Address Mode is backward compatible to older generations of serial flash memory that only support up to 128M-bit data. To address the 256M-bit or more data in 3-Byte Address Mode, Extended Address Register must be used in addition to the 3-Byte addresses.

4-Byte Address Mode is designed to support Serial Flash Memory devices from 256M-bit to 32G-bit. The extended Address Register is not necessary when the 4-Byte Address Mode is enabled.

Upon power up, the XM25RU512D can operate in either 3-Byte Address Mode or 4-Byte Address Mode, depending on the Non-Volatile Status Register Bit ADP (S17) setting. If ADP=0, the device will operate in 3-Byte Address Mode; if ADP=1, the device will operate in 4-Byte Address Mode. The factory default value for ADP is 0.

To switch between the 3-Byte or 4-Byte Address Modes, “Enter 4-Byte Mode (B7h)” or “Exit 4-Byte Mode (E9h)” instructions must be used. The current address mode is indicated by the Status Register Bit ADS (S16).

XM25RU512D also supports a set of basic SPI instructions which requires dedicated 4-Byte address regardless the device Address Mode setting. Please refer to Instruction Set Table for details.

7.3 Hold Function

For Standard SPI and Dual SPI operations, the /HOLD signal allows the XM25RU512D operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The /HOLD function is only available for standard SPI and Dual SPI operation, not during Quad SPI. The Quad Enable Bit QE in Status Register-2 is used to determine if the pin is used as /HOLD pin or data I/O pin. When QE=0, the pin is /HOLD, when QE=1(factory default), the pin will become an I/O pin, /HOLD function is no longer available.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the

/HOLD condition will terminate after the next falling edge of CLK. During a /HOLD condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

7.4 Software Reset & Hardware /RESET pin

The XM25RU512D can be reset to the initial power-on state by a software Reset sequence, either in SPI mode. This sequence must include two consecutive commands: Enable Reset (66h) & Reset (99h). If the command sequence is successfully accepted, the device will take approximately 28uS (tSR) to reset. No command will be accepted during the reset period.

For the WSON-8 and TFBGA package types, XM25RU512D can also be configured to utilize a hardware /RESET pin. The HOLD/RESET bit in the Status Register-3 is the configuration bit for /HOLD pin function or RESET pin function. When HOLD/RESET=0 (factory default), the pin acts as a /HOLD pin as described above; when HOLD/RESET=1, the pin acts as a /RESET pin. Drive the /RESET pin low for a minimum period of ~1us (tRESET*) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While /RESET is low, the device will not accept any command input.

If QE bit is set to 1, the /HOLD or /RESET function will be disabled, the pin will become one of the four data I/O pins.

Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum period of ~1us (tRESET*) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP and/or /HOLD).

Note:

While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum is recommended to ensure reliable operation.

7.5 Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the XM25RU512D provides several means to protect the data from inadvertent writes.

7.5.1 Write Protect Features

- *Device resets when VCC is below threshold*
- *Time delay write disable after Power-up*
- *Write enable/disable instructions and automatic write disable after erase or program*
- *Software and Hardware (/WP pin) write protection using Status Registers*
- *Write Protection using Power-down instruction*
- *Lock Down write protection for Status Register until the next power-up*
- *One Time Program (OTP) write protection for array and Security Registers using Status Register**
- *Note: This feature is available upon special order. Please contact XMC for details.*

Upon power-up or at power-down, the XM25RU512D will maintain a reset condition while VCC is below the threshold value of VWI, (See Power-up Timing and Voltage Levels and Figure 10-1). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds VWI, all program and erase related instructions are further disabled for a time delay of tPU. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and tVSL time delay is reached, and it must also track the VCC supply level at power-down to prevent adverse command sequence. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, TB, BP[3:0]) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

7.6 RPMC OPERATIONS

To prevent hardware vulnerability attack, RPMC provides a building block towards providing Confidentiality and Integrity of read/write flash memory data. The XM25RU512D is equipped with four 32-bit Monotonic counters and can be addressed individually by the 8-bit Counter Address. These Monotonic counters are used by the SPI flash controllers to ensure the physical authenticity of the attached flash devices.

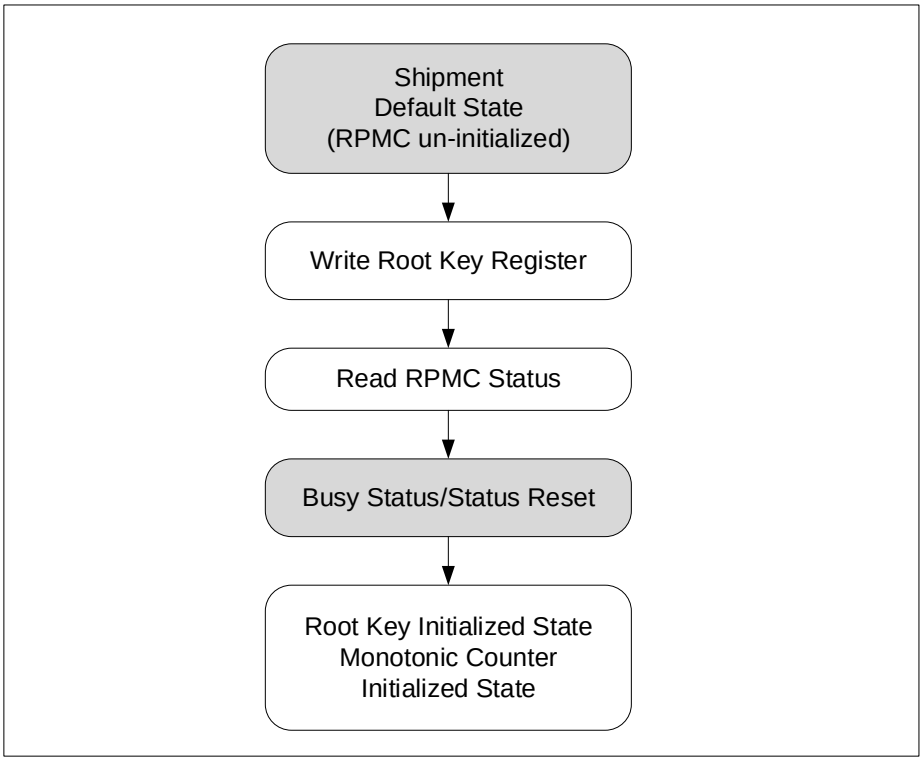
RPMC operation is based on the HMAC-SHA-256 cryptographic algorithm. HMAC-SHA-256 is a type of keyed hash algorithm that is constructed from the SHA-256 hash function and used as a Hash-based Message Authentication Code (HMAC). The HMAC process mixes a secret key with the message data, hashes the result with the hash function, mixes that hash value with the secret key again, and then applies the hash function a second time. The output hash is 256 bits in length.

An HMAC can be used to determine whether a message sent over an insecure channel has been tampered with, provided that the sender and receiver share a secret key. The sender computes the hash value for the original data and sends both the original data and hash value as a single message. The receiver recalculates the hash value on the received message and checks that the computed HMAC matches the transmitted HMAC. Any change to the data or the hash value results in a mismatch, because knowledge of the secret key is required to change the message and reproduce the correct hash value. Therefore, if the original and computed hash values match, the message is authenticated.

7.6.1 RPMC Initialization

RPMC operation is initialized in an OEM manufacturing environment by issuing the “Write Root Key Register” command. When this command is successfully received and executed, a 256-bit Root Key will be written into the flash device permanently, and the corresponding Monotonic counters will also be initialized to 0. After the initialization procedure, the Root Key value can no longer be altered or accessed externally through the SPI interface. The initialized Monotonic counters is ready to accept the authenticated RPMC commands.

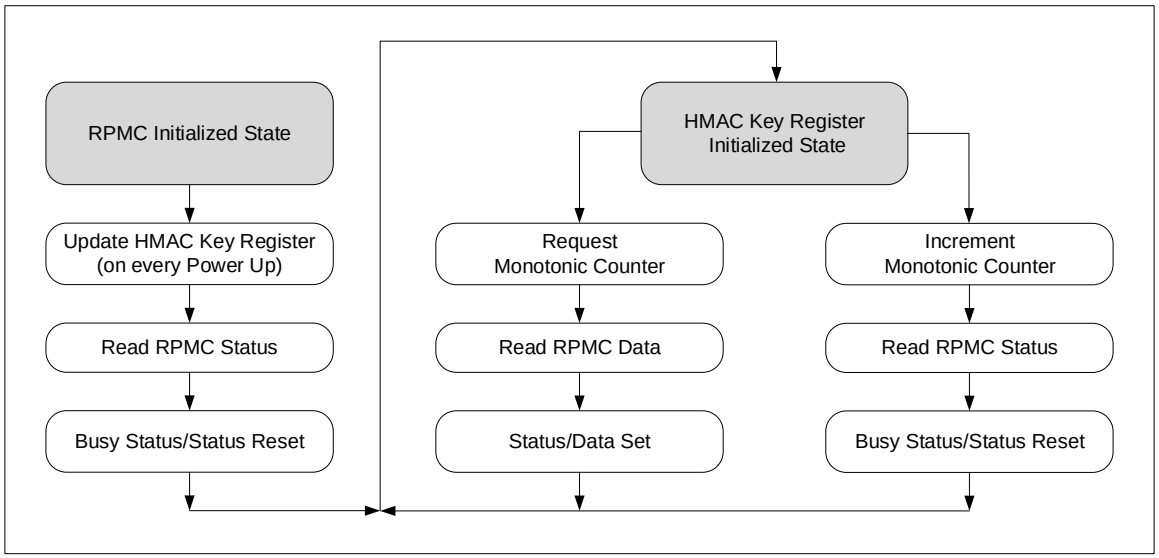
Figure 7-2 XM25RU512D RPMC Initialization Flow Diagram



7.6.2 RPMC Operation Flow

Once the root key and the Monotonic counters have been initialized, every time after the device is powered on, prior to any RPMC operations, the external SPI flash controller must update the HMAC Key register in the XM25RU512D. After initializing the HMAC key register, there are two different RPMC operations can be performed. “Increment Monotonic counters” is used to increase the Monotonic counters value by 1. “Request Monotonic counters” is used to read out the existing Monotonic counters data.

Figure 7-3 XM25RU512D RPMC Operation Flow Diagram



7.6.3 Operations Allowed / Disallowed During RPMC Operation

The RPMC operation is independent to the other SPI flash operations. The RPMC input command OP1 (9Bh) will initial internal operations after the authenticated command is accepted by the device. During the internal operation period, the BUSY bit in the RPMC Status Register (bit 0) will be set to 1. The RPMC internal operation cannot be suspended and can only be interrupted by the Device Reset command (99h). While the RPMC internal operation is going on, other SPI flash commands can be issued and executed. Please refer to the table below for details.

Operations	Device Behavior
Suspend/Resume	Only main flash memory Program/Erase operations can be suspended and resumed later. RPMC operations cannot be suspended.
Read/Program/Erase main memory array	All memory Read/Program/Erase commands are accepted while a RPMC operation is on-going.
Read/Write SPI flash Status Registers	The SPI flash Status Register-1&2 can be read out or written to during any internal RPMC operations.
RPMC OP1 command	The RPMC input command OP1 will be ignored while a RPMC operation is on-going. This command can be accepted and executed while a main memory Program/Erase operation is on-going.
Read RPMC Status/Data OP2 command	The RPMC Status Register can be read out while a RPMC operation is ongoing and this is the way to check if the RPMC operation has finished or not. If the BUSY bit of RPMC Status Register is set as 1, the RPMC data output following the Status Register is not reliable. During the SPI flash internal Program/Erase operations, this command can still be used to check the RPMC status or read out RPMC data.
Device Reset	The software reset sequence can be issued any time during SPI flash or RPMC internal operations. All volatile settings will be reset and data corruption may happen if there’s an on-going Program/Erase operation.

7.6.4 RPMC Status Register Definition

During the RPMC operations, an 8-bit Status Register is used to indicate various states of the command execution and device status. A “Read RPMC Status” command can be issued during any RPMC operation to check the Status Register.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Successful Completion	Not Defined	Fatal Error (Pgm/Erase Fail or no valid counter found)	Counter_Address Mismatch	HMAC Key Reg Uninitialized	Signature Mismatch or Counter Address out of range or Write_Mode out of range	Root Keys Overwrite or Root Keys length mismatch or TruncatedSig Mismatch	BUSY

RPMC Status Register[7:0]	Applicable Cmd Type (s)	Description
00000000	/	Power On State (Read RPMC Status is issued directly after powerup).
10000000	00, 01, 02, 03	This status must be set on successful completion (no errors) of OP1 command (9Bh).
0xxxxxx1	00, 01, 02, 03, 04-FF	This bit must be set to 1, when device is busy executing OP1 command (9Bh). It is reset to 0 when the command execution is done.
0xxxxx1x	00, 01	This bit is set only when the correct payload size is received. For CmdType = 00, this bit must be set on Root Key Register Overwrite or Counter Address out of range or Truncated Signature mis-match error. For CmdType = 01, this bit is set when the corresponding Monotonic counters is uninitialized.
0xxxx1xx	00, 01, 02, 03	This bit must be set on Signature Mismatch, Counter Address out of range when correct payload size is received; or CmdType is out of range; or incorrect payload size is received.
0xxx1xxx	02, 03	This bit must be set on HMAC Key Register (or Monotonic counters) uninitialized on previous OP1 command when correct payload size is received.
0xx1xxxx	02	This bit must be set on Counter_AddressMismatch on previous increment when correct payload size is received.
0x1xxxxx	/	Fatal Error, e.g. program fail, no valid counter found after initialization.
Current value	/	Status register will naturally not be updated until first 8 bits of OP1 (9Bh) is received. However it is expected that the correct error type is reflected for any OP1 operation that exceeds a minimum of 16 clocks with active chip-select.

8 STATUS AND CONFIGURATION REGISTERS

Three Status and Configuration Registers are provided for XM25RU512D. The Read Status Register- 1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, output driver strength, power-up and current Address Mode. The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, Hold/Reset functions, output driver strength and power- up Address Mode. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

8.1 Status Registers

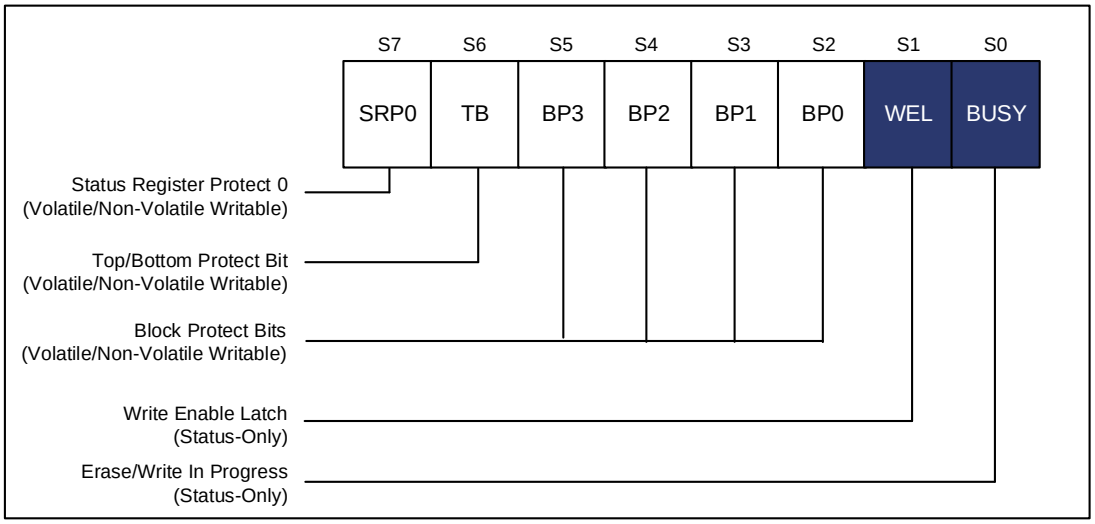


Figure 8-1 Status Register-1

8.1.1 Erase/Write in Progress (BUSY) - Status Only

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

8.1.2 Write Enable Latch (WEL) – Status Only

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.

8.1.3 Block Protect Bits (BP3, BP2, BP1, BP0) – Volatile/Non-Volatile Writable

The Block Protect Bits (BP3, BP2, BP1, BP0) are non-volatile read/write bits in the status register (S5, S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

8.1.4 Top/Bottom Block Protect (TB) – Volatile/Non-Volatile Writable

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of WEL bits.

8.1.5 Complement Protect (CMP) – Volatile/Non-Volatile Writable

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with TB, BP3, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by TB, BP3, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 64KB block can be protected while the rest of the array is not; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.

8.1.6 Status Register Protect (SRP, SRL) – Volatile/Non-Volatile Writable

Three Status and Configuration Registers are provided for XM25RU512D. The Read Status Register-1/2/3 instructions can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Register lock status, Erase/Program Suspend status, and output driver strength, The Write Status Register instruction can be used to configure the device write protection features, Quad SPI setting, Security Register OTP locks, output driver. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP, SRL), the Write Enable instruction, and during Standard/Dual SPI operations, the /WP pin.

SR	SR	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status register can be written to after a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	X	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle.(1)
1	X	X	One Time Program(2)	Status Register is permanently protected and cannot be written to. (enabled by adding prefix command AAh, 55h,refer to the follow waveform)

Note:

[1] When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state;

[2] This feature is available upon special order. Please contact XMC for details.

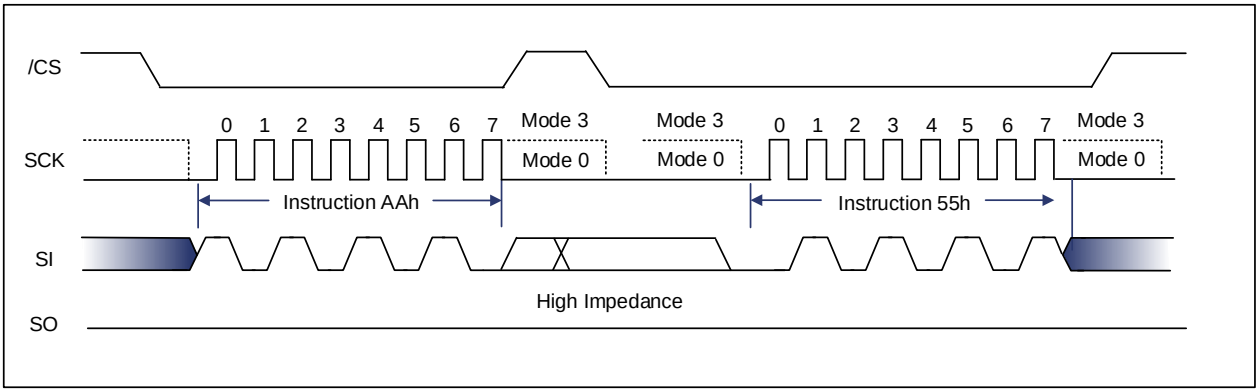


Figure 8-2 One Time Program prefix command(AAh,55h)

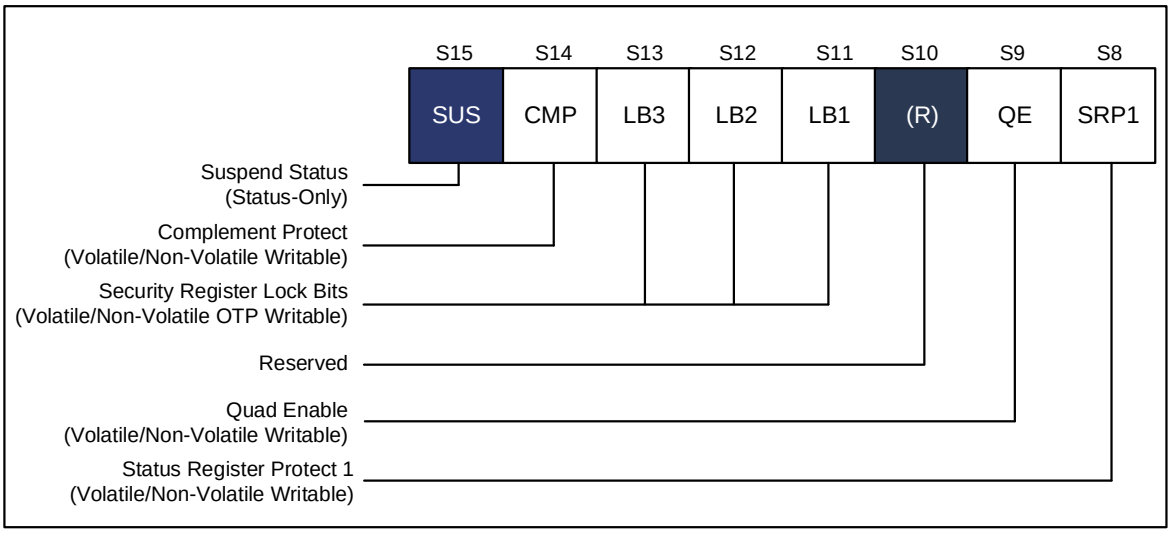


Figure 8-3 Status Register-2

8.1.7 Erase/Program Suspend Status (SUS) – Status Only

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

8.1.8 Security Register Lock Bits (LB3, LB2, LB1) – Volatile/Non-Volatile OTP Writable

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0, Security Registers are unlocked. LB3-1 can be set to 1 individually using the Write Status Register instruction. LB3-1 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

8.1.9 Quad Enable (QE) – Volatile/Non-Volatile Writable

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default for part number with ordering options “G”), the /WP pin and /HOLD are enabled. When the QE bit is set to a 1(factory default for Quad Enabled part numbers with ordering option “Q”), the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

WARNING: If the /WP or /HOLD pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

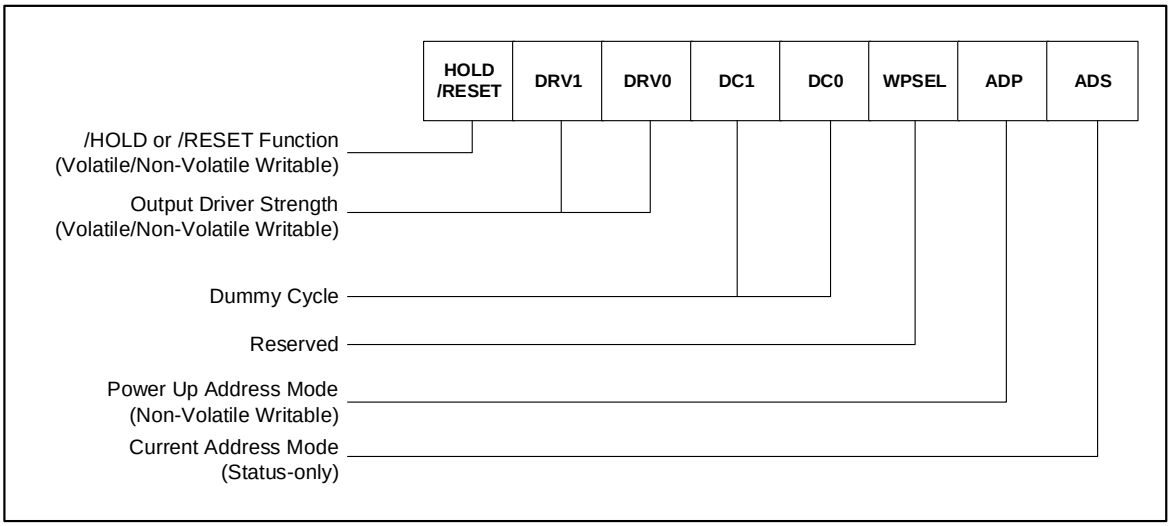


Figure 8-4 Status Register-3

8.1.10 Current Address Mode (ADS) – Status Only

The Current Address Mode bit is a read only bit in the Status Register-3 that indicates which address mode the device is currently operating in. When ADS=0, the device is in the 3-Byte Address Mode, when ADS=1, the device is in the 4-Byte Address Mode.

8.1.11 Power-Up Address Mode (ADP) – Non-Volatile Writable

The ADP bit is a non-volatile bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period, and it is only writable by the non-volatile Write Status sequence (06h + 11h). When ADP=0(factory default), the device will power up into 3-Byte Address Mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte Address Mode directly.

8.1.12 WPSEL – Non-Volatile Writable

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, TB, BP[3:0] bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

8.1.13 Output Driver Strength (DRV1, DRV0) – Volatile/Non-Volatile Writable

The DRV1 & DRV0 bits are used to determine the output driver strength for the Read operations.

DRV1, DRV0	Driver Strength
0, 0	100%
0, 1	75% (default)
1, 0	50%
1, 1	25%

8.1.14 /HOLD or /RESET Pin Function (HOLD/RESET) – Volatile/Non-Volatile Writable

The HOLD/RESET bit is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin. When HOLD/RESET=0 (factory default), the pin acts as /HOLD; when HOLD/RESET=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

8.1.15 Dummy Cycle Bits

The Dummy Cycle Bits (DC1&DC0) are used to determine the Max Frequency for the Read operations.

DC[1:0]	Numbers of Dummy clock cycles	Fast Read	Fast Read Dual Output	Fast Read Quad Output
00(Default)	8	133MHz	133MHz	133MHz
01	8	133MHz	133MHz	133MHz
10	8	133MHz	133MHz	133MHz
11	8	133MHz	133MHz	133MHz

DC[1:0]	Numbers of Dummy clock cycles	Fast Read Dual I/O	Word Read Quad I/O
00(default)	4	80MHz	80MHz
01	8	133MHz	133MHz
10	4	80MHz	80MHz
11	8	133MHz	133MHz

DC[1:0]	Numbers of Dummy clock cycles	Fast Read Quad I/O
00(Default)	6	133MHz
01	4	80MHz
10	8	133MHz
11	10	133MHz

8.1.16 Reserved Bits – Non Functional

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

XM25RU512D Status Register Memory Protection (CMP = 0)

STATUS REGISTER(1)					XM25RU512D (512Mb / 64M-BYTE) MEMORY PROTECTION(2)			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
0	0	0	0	1	1023	03FF0000h – 03FFFFFFh	64KB	Upper 1/1024
0	0	0	1	0	1022 thru 1023	03FE0000h – 03FFFFFFh	128KB	Upper 1/512
0	0	0	1	1	1020 thru 1023	03FC0000h – 03FFFFFFh	256KB	Upper 1/256
0	0	1	0	0	1016 thru 1023	03F80000h – 03FFFFFFh	512KB	Upper 1/128
0	0	1	0	1	1008 thru 1023	03F00000h – 03FFFFFFh	1MB	Upper 1/64
0	0	1	1	0	992 thru 1023	03E00000h – 03FFFFFFh	2MB	Upper 1/32
0	0	1	1	1	960 thru 1023	03C00000h – 03FFFFFFh	4MB	Upper 1/16
0	1	0	0	0	896 thru 1023	03800000h – 03FFFFFFh	8MB	Upper 1/8
0	1	0	0	1	768 thru 1023	03000000h – 03FFFFFFh	16MB	Upper 1/4
0	1	0	1	0	512 thru 1023	02000000h – 03FFFFFFh	32MB	Upper 1/2
0	1	0	1	1	0 thru 1023	00000000h – 03FFFFFFh	64MB	ALL
0	1	1	0	0	0 thru 1023	00000000h – 03FFFFFFh	64MB	ALL
0	1	1	0	1	0 thru 1023	00000000h – 03FFFFFFh	64MB	ALL
0	1	1	1	0	0 thru 1023	00000000h – 03FFFFFFh	64MB	ALL
0	1	1	1	1	0 thru 1023	00000000h – 03FFFFFFh	64MB	ALL
1	0	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	0	00000000h – 0000FFFFh	64KB	Lower 1/1024
1	0	0	1	0	0 thru 1	00000000h – 0001FFFFh	128KB	Lower 1/512
1	0	0	1	1	0 thru 3	00000000h – 0003FFFFh	256KB	Lower 1/256
1	0	1	0	0	0 thru 7	00000000h – 0007FFFFh	512KB	Lower 1/128
1	0	1	0	1	0 thru 15	00000000h – 000FFFFFh	1MB	Lower 1/64
1	0	1	1	0	0 thru 31	00000000h – 001FFFFFh	2MB	Lower 1/32
1	0	1	1	1	0 thru 63	00000000h – 003FFFFFh	4MB	Lower 1/16
1	1	0	0	0	0 thru 127	00000000h – 007FFFFFh	8MB	Lower 1/8
1	1	0	0	1	0 thru 255	00000000h – 00FFFFFFh	16MB	Lower 1/4
1	1	0	1	0	0 thru 511	00000000h – 01FFFFFFh	32MB	Lower 1/2
1	1	0	1	1	0 thru 1023	00000000h – 03FFFFFFh	64MB	ALL
1	1	1	0	0	0 thru 1023	00000000h – 03FFFFFFh	64MB	ALL
1	1	1	0	1	0 thru 1023	00000000h – 03FFFFFFh	64MB	ALL
1	1	1	1	0	0 thru 1023	00000000h – 03FFFFFFh	64MB	ALL
1	1	1	1	1	0 thru 1023	00000000h – 03FFFFFFh	64MB	ALL

Note:
[1] X = don't care;
[2] L = Lower; U = Upper;
[3] If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored

XM25RU512D Status Register Memory Protection (CMP = 1)

STATUS REGISTER(1)					XM25RU512D (512b / 64M-BYTE) MEMORY PROTECTION(2)			
TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
0	0	0	0	0	ALL	00000000h - 07FFFFFFh	ALL	ALL
0	0	0	0	1	0 thru 1022	00000000h – 03FEFFFFh	65,472KB	Lower 1023/1024
0	0	0	1	0	0 thru 1021	00000000h – 03FDFFFFh	65,408KB	Lower 511/512
0	0	0	1	1	0 thru 1019	00000000h – 03FBFFFFh	65,280KB	Lower 255/256
0	0	1	0	0	0 thru 1015	00000000h – 03F7FFFFh	65,024KB	Lower 127/128
0	0	1	0	1	0 thru 1007	00000000h – 03EFFFFFh	63MB	Lower 63/64
0	0	1	1	0	0 thru 991	00000000h – 03DFFFFFh	62MB	Lower 31/32
0	0	1	1	1	0 thru 959	00000000h – 03BFFFFFh	60MB	Lower 15/16
0	1	0	0	0	0 thru 895	00000000h – 037FFFFFh	56MB	Lower 7/8
0	1	0	0	1	0 thru 767	00000000h – 02FFFFFFh	48MB	Lower 3/4
0	1	0	1	0	0 thru 511	00000000h – 01FFFFFFh	32MB	Lower 1/2
0	1	0	1	1	NONE	NONE	NONE	NONE
0	1	1	0	0	NONE	NONE	NONE	NONE
0	1	1	0	1	NONE	NONE	NONE	NONE
0	1	1	1	0	NONE	NONE	NONE	NONE
0	1	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	0	ALL	00000000h – 03FFFFFFh	ALL	ALL
1	0	0	0	1	1 thru 1023	00010000h – 03FFFFFFh	65,472KB	Upper 1023/1024
1	0	0	1	0	2 thru 1023	00020000h – 03FFFFFFh	65,408KB	Upper 511/512
1	0	0	1	1	4 thru 1023	00040000h – 03FFFFFFh	65,280KB	Upper 255/256
1	0	1	0	0	8 thru 1023	00080000h – 03FFFFFFh	65,024KB	Upper 127/128
1	0	1	0	1	16 thru 1023	00100000h – 03FFFFFFh	63MB	Upper 63/64
1	0	1	1	0	32 thru 1023	00200000h – 03FFFFFFh	62MB	Upper 31/32
1	0	1	1	1	64 thru 1023	00400000h – 03FFFFFFh	60MB	Upper 15/16
1	1	0	0	0	128 thru 1023	00800000h – 03FFFFFFh	56MB	Upper 7/8
1	1	0	0	1	256 thru 1023	01000000h – 03FFFFFFh	48MB	Upper 3/4
1	1	0	1	0	512 thru 1023	02000000h – 03FFFFFFh	32MB	Upper 1/2
1	1	0	1	1	NONE	NONE	NONE	NONE
1	1	1	0	0	NONE	NONE	NONE	NONE
1	1	1	0	1	NONE	NONE	NONE	NONE
1	1	1	1	0	NONE	NONE	NONE	NONE
1	1	1	1	1	NONE	NONE	NONE	NONE

Note:
[1] X = don't care;
[2] L = Lower; U = Upper;
[3] If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored

8.2 Extended Address Register – Volatile Writable Only

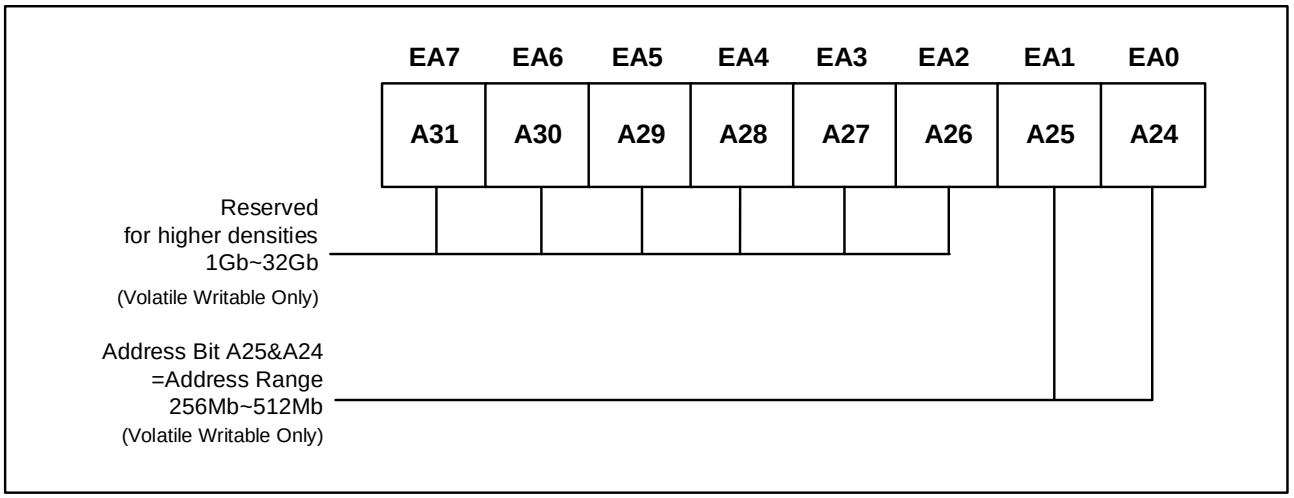


Figure 8-5 Extended Address Register

In addition to the Status Registers, XM25RU512D provides a volatile Extended Address Register which consists of the 4th byte of memory address. The Extended Address Register is accessible by Read Extended Address Register (C8h) and Write Extended Address Register (C5h) instructions. The Extended Address Register is used only when the device is operating in the 3-Byte Address Mode (ADS=0). The separate 128Mb memory array ranges (or regions) of 00000000h–00FFFFFFh, 01000000h–01FFFFFFh, 02000000h–02FFFFFFh and 03000000h– 03FFFFFFh are accessible depending on the setting of Extended Address Register A25 and A24 bits as shown on the table below.

A25, A24	Memory Array Address Range
0, 0	00000000h – 00FFFFFFh
0, 1	01000000h – 01FFFFFFh
1, 0	02000000h – 02FFFFFFh
1, 1	03000000h – 03FFFFFFh

Any command with dedicated 4-byte address input will use the 4th Address Byte (A31-A24) input and not the Extended Address Register. If the device powers up with ADP bit set to 1, or an “Enter 4-Byte Address Mode (B7h)” instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Register setting will be ignored. The 4th Byte Address input will not alter the content of Extended Address Register.

Upon power up or after the execution of a Software/Hardware Reset, the Extended Address Register values will be cleared to 0.

9 INSTRUCTIONS

The Standard/Dual/Quad SPI instruction set of the XM25RU512D consists of 48 basic instructions that are fully controlled through the SPI bus (see Instruction Set Table). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the SI input provides the instruction code. Data on the SI input is sampled on the rising edge of clock with most significant bit (MSB) first.

The Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figure 9-1 to Figure 9-58. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

9.1 Device ID and Instruction Set Tables

9.1.1 Manufacturer and Device Identification

MANUFACTURER ID	(MF7 – MF0)	
XMC Serial Flash	20h	
Device ID	(ID7 – ID0)	(ID15 – ID0)
Instruction	ABh, 90h, 92h, 94h	9Fh
XM25RU512D	19h	4420h

9.1.2 Instruction Set Table 1 (Standard/Dual/Quad SPI Instructions)(1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock	8	8	8	8	8	8	8
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)2)		
Manufacturer/Device ID	90h	Dummy	Dummy	00h	MF7-MF0)	(ID7-ID0)	
JEDEC ID	9Fh	MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Read Unique ID	4Bh	Dummy	Dummy	Dummy	Dummy	(UID63-0)	
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)		
Read Data with 4-Byte Address	13h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Fast Read with 4-Byte Address	0Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Page Program with 4-Byte Address	12h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0			
Sector Erase (4KB) with 4-Byte Address	21h	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB) with 4-Byte Address	DCh	A31-A24	A23-A16	A15-A8	A7-A0		
Chip Erase	C7h/60h						
Read Status Register-1	05h	(S7-S0)(2)					
Write Status Register-1(4)	01h	(S7-S0)(4)					
Read Status Register-2	35h	(S15-S8)(2)					
Write Status Register-2	31h	(S15-S8)					
Read Status Register-3	15h	(S23-S16)(2)					
Write Status Register-3	11h	(S23-S16)					
Read Extended Addr. Reg.	C8h	(EA7-EA0)(2)					
Write Extended Addr. Reg.	C5h	(EA7-EA0)					
Read SFDP Register	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase Security Register(5)	44h	A23-A16	A15-A8	A7-A0			
Program Security Register(5)	42h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)	
Read Security Register(5)	48h	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase / Program Suspend	75h						
Erase / Program Resume	7Ah						
Power-down	B9h						
Ultra-Deep Power-down	79h						
Enter 4-Byte Address Mode	B7h						
Exit 4-Byte Address Mode	E9h						
Enable Reset	66h						
Reset Device	99h						

9.1.3 Instruction Set Table 2 (Standard/Dual/Quad SPI Instructions,3-Byte Address Mode)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10
Number of Clock	8	8	8	8	4	4	4	4	4	4
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0) (7)	…		
Fast Read Dual Output with 4-Byte Address	3Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0) (7)	…	
Number of Clock	8	4	4	4	4	4	4	4	4	4
Mftr./Device ID Dual I/O	92h	A23-A16	A15-A8	0	Dummy (11)	MF7-MF0	(D7-D0)			
Fast Read Dual I/O	BBh	A23-A16	A15-A8	A7-A0	Dummy (11)	(D7-D0)	…			
Fast Read Dual I/O with 4-Byte Address	BCh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy (11)	(D7-D0)	…		
Number of Clock	8	8	8	8	2	2	2	2	2	2
Quad Input Page Program	32h	A23-A16	A15-A8	A7-A0	(D7-D0)(9)	(D7-D0)(3)	…			
Quad Page Program with 4-Byte Address	34h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	…	…		
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0) (9)	…
Number of Clock	8	8	8	8	8	2	2	2	2	2
Fast Read Quad Output with 4-Byte Address	6Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0) (9)
Number of Clock	8	2	2	2	2	2	2	2	2	2
Quad Page Program	33h	A23-A16	A15-A8	A7-A0	(D7-D0) (9)					
Mftr./Device ID Quad I/O	94h	A23-A16	A15-A8	0	Dummy (11)	Dummy	Dummy	MF7-MF0	(D7-D0)	
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	Dummy (11)	Dummy	Dummy	(D7-D0)	…	
Fast Read Quad I/O with 4-Byte Address	ECh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy (11)	Dummy	Dummy	(D7-D0)	…
Word Read Quad I/O	E7h	A23-A16	A15-A8	A7-A0	Dummy (11)	Dummy	(D7-D0)			
Set Burst with Wrap	77h	Dummy	Dummy	Dummy	W7-W0					

9.1.4 Instruction Set Table 6 (Standard/Dual/Quad SPI Instructions, 4-Byte Address Mode)(1)

Data In Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock	8	8	8	8	8	8	8
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Read Unique ID	4Bh	Dummy	Dummy	Dummy	Dummy	Dummy	(UID63-0)
Read Data	03h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Read Data with 4-Byte Address	13h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	0Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Fast Read with 4-Byte Address	0Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Page Program	02h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Page Program with 4-Byte Address	12h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Sector Erase (4KB) with 4-Byte Address	21h	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	52h	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB) with 4-Byte Address							
Block Erase (64KB)	D8h	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB) with 4-Byte Address	DCh	A31-A24	A23-A16	A15-A8	A7-A0		
Chip Erase	C7h/ 60h						
Read Status Register-1	05h	(S7-S0)(2)					
Write Status Register-1(4)	01h	(S7-S0)(4)					
Read Status Register-2	35h	(S15-S8)(2)					
Write Status Register-2	31h	(S15-S8)					
Read Status Register-3	15h	(S23-S16)(2)					
Write Status Register-3	11h	(S23-S16)					
Read Extended Addr. Reg.	C8h	(EA7-EA0)(2)					

Write Extended Addr. Reg.	C5h	(EA7-EA0)					
Read SFDP Register	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Erase Security Register[5]	44h	A31-A24	A23-A16	A15-A8	A7-A0		
Program Security Register[5]	42h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0[3]
Read Security Register[5]	48h	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Erase / Program Suspend	75h						
Erase / Program Resume	7Ah						
Power-down	B9h						
Ultra-Deep Power-down	79h						
Enter 4-Byte Address Mode	B7h						
Exit 4-Byte Address Mode	E9h						
Enable Reset	66h						
Reset Device	99h						

9.1.5 Instruction Set Table 5 (Dual/Quad SPI Instructions, 4-Byte Address Mode)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte9	Byte10
Number of Clock	8	8	8	8	8	8	4	4		
Fast Read Dual Output	3Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0,…)(7)			
Fast Read Dual Output with 4-Byte Address	3Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0,…)(7)			
Number of Clock	8	4	4	4	4	4	4	4		
Mftr./Device ID Dual I/O	92h	A31-A24	A23-A16	A15-A8	00	Dummy(11)	(MF7-MF0)	(ID7-ID0)		
Fast Read Dual I/O	BBh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(11)	(D7-D0)			
Fast Read Dual I/O with 4-Byte Address	BCh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(11)	(D7-D0)			
Number of Clock	8	8	8	8	8	4	4	4		
Quad Input Page Program	32h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)(9)	(D7-D0)(3)..			
Quad Page Program with 4-Byte Address	34h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0	D7-D0	D7-D0	
Fast Read Quad Output	6Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)(9)		
Fast Read Quad Output with 4-Byte Address	6Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)(9)		
Number of Clock	8	2	2	2	2	2	2	2	2	2
Quad Page Program	33h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)(9)				
Mftr./Device ID Quad I/O	94h	A31-A24	A23-A16	A15-A8	00	Dummy(11)	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)
Fast Read Quad I/O	EBh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(11)	Dummy	(D7-D0)		
Fast Read Quad I/O with 4-Byte Address	Ech	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(11)	Dummy	(D7-D0)		
Word Read Quad I/O	E7h	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(11)	Dummy	(D7-D0)		
Set Burst with Wrap	77h	Dummy	Dummy	Dummy	Dummy	W7-W0				

Notes:

1 Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data output from the device on either 1, 2 or 4 IO pins.

2 The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.

3 At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.

4 Write Status Register-1 (01h) can also be used to program Status Register-1&2, see section 8.2.5.

5. Security Register Address:

Security Register 1: A23-16 = 00h; A15-8 = 10h; A7-0 = byte address;

Security Register 2: A23-16 = 00h; A15-8 = 20h; A7-0 = byte address;

Security Register 3: A23-16 = 00h; A15-8 = 30h; A7-0 = byte address

6. Dual SPI address input format:

IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0,

IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1

7. Dual SPI data output format:

IO0 = (D6, D4, D2, D0) IO1 = (D7, D5, D3, D1)

8. Quad SPI address input format:

IO0 = A20, A16, A12, A8, A4, A0, M4, M0

IO1 = A21, A17, A13, A9, A5, A1, M5, M1

IO2 = A22, A18, A14, A10, A6, A2, M6, M2

IO3 = A23, A19, A15, A11, A7, A3, M7, M3

Set Burst with Wrap input format:

IO0 = x, x, x, x, x, x, W4, x

IO1 = x, x, x, x, x, x, W5, x

IO2 = x, x, x, x, x, x, W6, x

IO3 = x, x, x, x, x, x, x, x

9. Quad SPI data input/output format:

IO0 = (D4, D0, …..)

IO1 = (D5, D1, …..)

IO2 = (D6, D2, …..)

IO3 = (D7, D3, …..)

10.Fast Read Quad I/O data output format:

IO0 = (x, x, x, x, D4, D0, D4, D0)

IO1 = (x, x, x, x, D5, D1, D5, D1)

IO2 = (x, x, x, x, D6, D2, D6, D2)

IO3 = (x, x, x, x, D7, D3, D7, D3)

11. Word Read Quad I/O data output format:

IO0 = (x, x, D4, D0, D4, D0, D4, D0)

IO1 = (x, x, D5, D1, D5, D1, D5, D1)

IO2 = (x, x, D6, D2, D6, D2, D6, D2)

IO3 = (x, x, D7, D3, D7, D3, D7, D3)

9.1.6 Instruction Set Table 2-1 (RPMC Input Instruction, OP1)(1)

INSTRUCTION NAME	BYTE 0	BYTE 1 (Cmd Type)	BYTE 2	BYTE 3(2)		
Write Root Key Register	**9Bh**	00h	CounterAddr [7:0]	Reserved [7:0]	Byte 4 - 35 RootKey[255:0]	Byte 36 - 63 TruncatedSign[223:0]
Update HMAC Key Register	**9Bh**	01h	CounterAddr [7:0]	Reserved [7:0]	Byte 4 - 7 KeyData[31:0]	Byte 8 - 39 Signature[255:0]
Increment Monotonic Counter	**9Bh**	02h	CounterAddr [7:0]	Reserved [7:0]	Byte 4 - 7 CounterData[31:0]	Byte 8 - 39 Signature[255:0]
Request Monotonic Counter	**9Bh**	03h	CounterAddr [7:0]	Reserved [7:0]	Byte 4 - 15 Tag[95:0]	Byte 16 - 47 Signature[255:0]
Reserved Commands	**9Bh**	04h~FFh	Reserved			

9.1.7 Instruction Set Table 2-2 (RPMC Output Instruction, OP2) (1)

INSTRUCTION NAME	BYTE0	BYTE 1	BYTE 2	BYTE 3 - 14	BYTE 15 - 18	BYTE 19 - 50
Read RPMC Status / Data(3)(4)	**96h**	dummy	(RPMC Status[7:0])	(Tag [95:0])	(Counter Data [31:0])	(Signature[255:0])

Notes:

1. All RPMC instructions are in Standard SPI format. Each Input/Output Byte requires 8 clocks.

2. The Reserved[7:0] field for RPMC OP1 must be all 0s (00000000 ’ b).

3. The controller may terminate the Read RPMC Status/Data instruction at any time without going through the entire data output sequence.

4. When BUSY=1, from Byte-3 and beyond, the device will output the RPMC_Status[7:0] value continuously until /CS terminates the instruction. The device will not output Tag, CounterData & Signature fields when BUSY=1. Once BUSY becomes 0, another OP2 command must be issued to read out the correct Tag, CounterData & Signature fields.

9.2 Instruction Descriptions

9.2.1 Write Enable (06h)

The Write Enable instruction (Figure 9-1) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (SI) pin on the rising edge of CLK, and then driving /CS high.

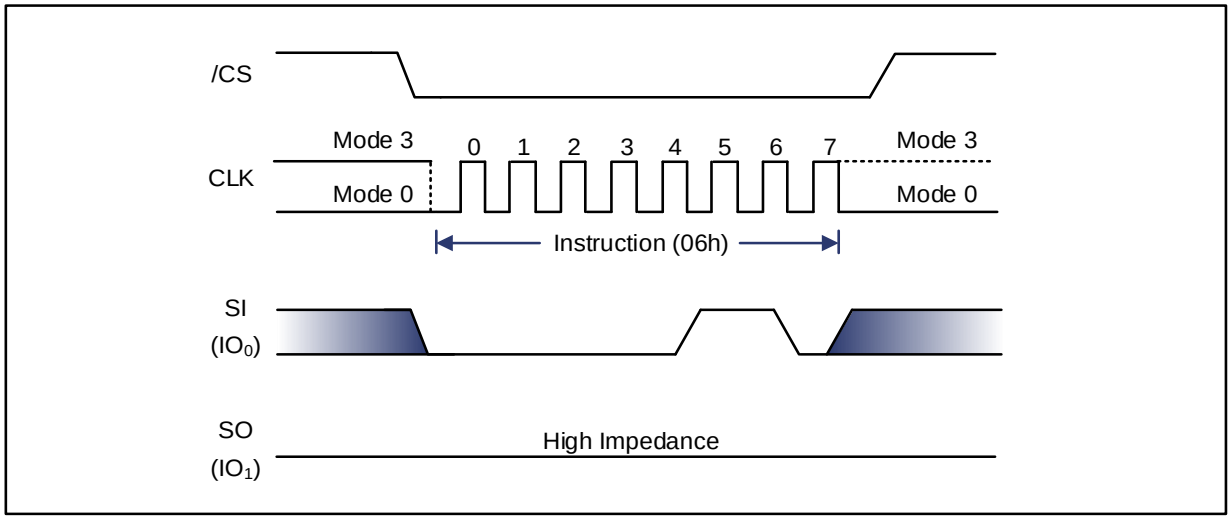


Figure 9-1 Write Enable Instruction for SPI Mode

9.2.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 7.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 9-2) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

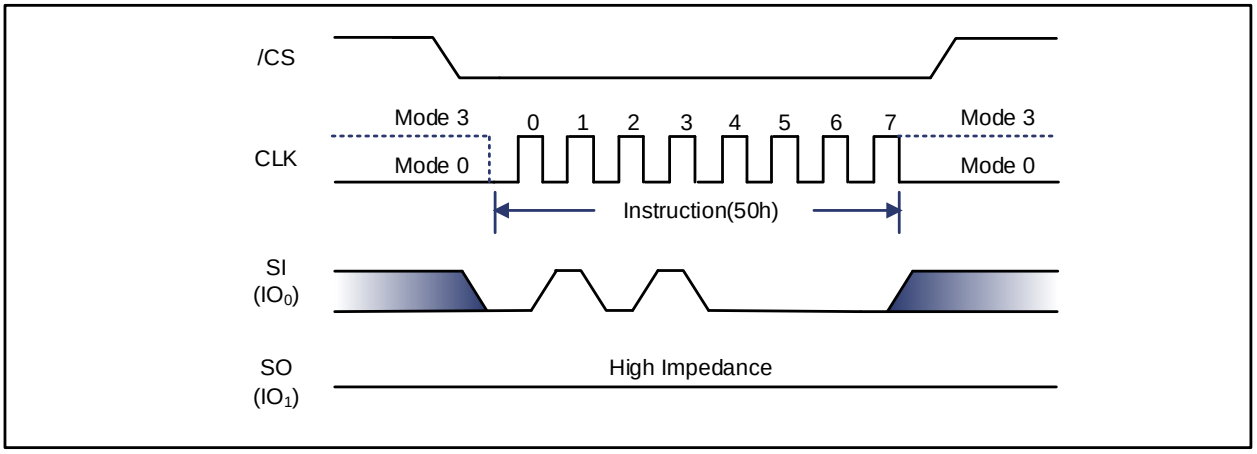


Figure 9-2 Write Enable for Volatile Status Register Instruction for SPI Mode

9.2.3 Write Disable (04h)

The Write Disable instruction resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the SI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions.

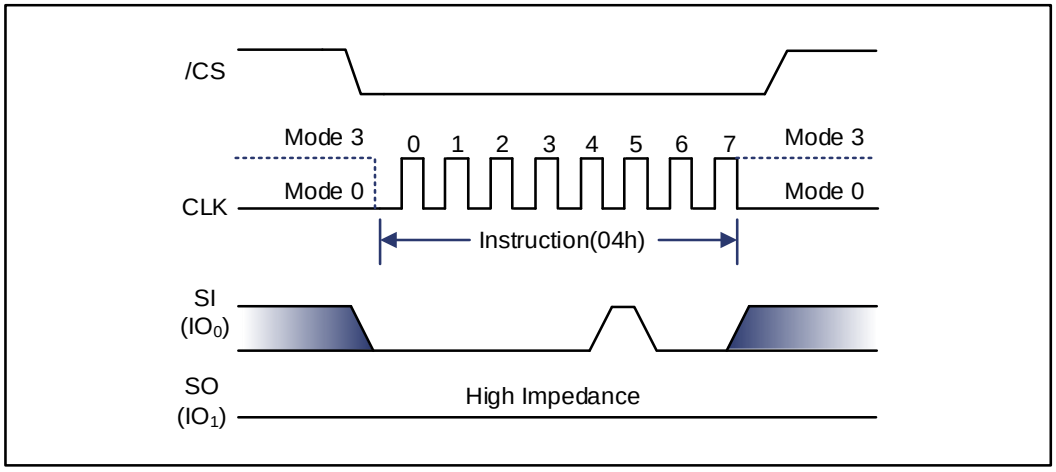


Figure 9-3 Write Disable Instruction for SPI Mode

9.2.4 Read Status Register-1 (05h), Status Register-2 (35h) & Status Register-3 (15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 into the SI pin on the rising edge of CLK. The status register bits are then shifted out on the SO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 9-4. Refer to section 8.1 for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 9-4. The instruction is completed by driving /CS high.

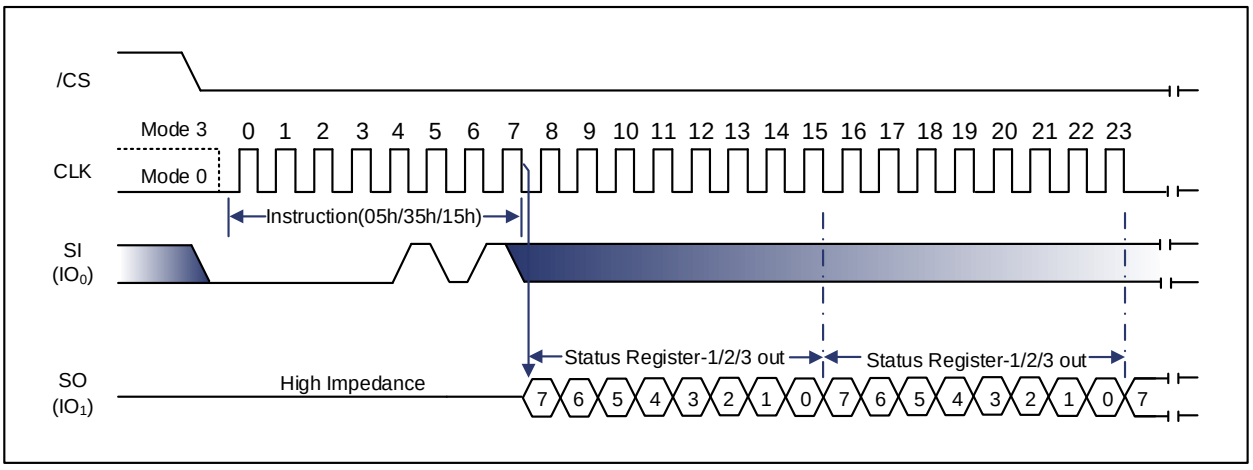


Figure 9-4 Read Status Register Instruction (SPI Mode)

9.2.5 Write Status Register-1 (01h), Status Register-2 (31h) & Status Register-3 (11h)

The Write Status Register instruction allows the Status Registers to be written. The writable Status Register bits include: SRP0, TB, BP[2:0] in Status Register-1; CMP, LB[3:1], QE, SRP1 in Status Register-2; HOLD/RESET, DRV1, DRV0 ,DC1,DC0,ADP in Status Register-3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non- volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h/31h/11h”, and then writing the status register data byte as illustrated in Figure 9-5.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must have been executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRP1 and LB[3:1] cannot be changed from “1” to “0” because of the OTP protection for these bits. Upon power off or the execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tW (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of tSHSL2 (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

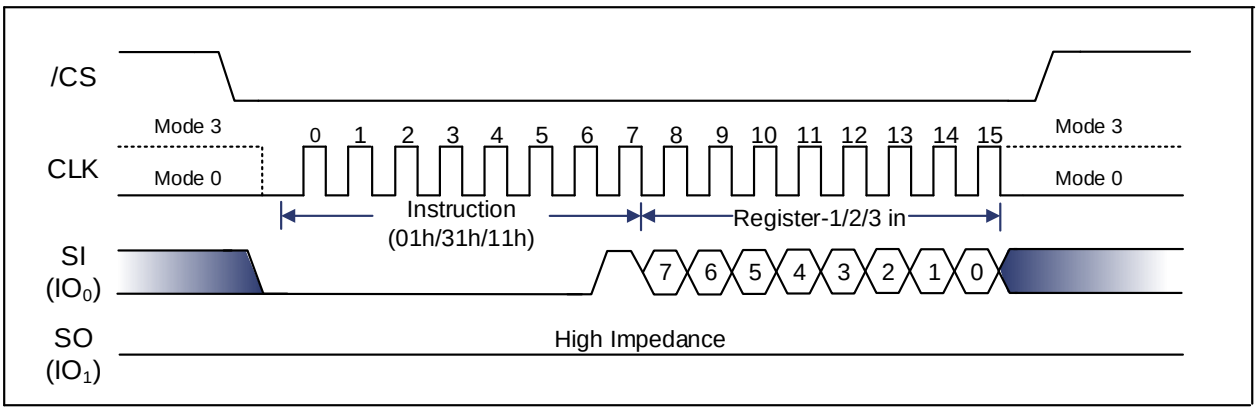


Figure 9-5 Write Status Register-1/2/3 Instruction (SPI Mode)

The XM25RU512D is also backward compatible to XMC's previous generations of serial flash memories, in which the Status Register-1&2 can be written using a single "Write Status Register-1 (01h)" command. To complete the Write Status Register-1&2 instructions, the /CS pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 9-6. If /CS is driven high after the eighth clock, the Write Status Register-1 (01h) instruction will only program the Status Register-1, the Status Register-2 will not be affected (Previous generations will clear CMP and QE bits).

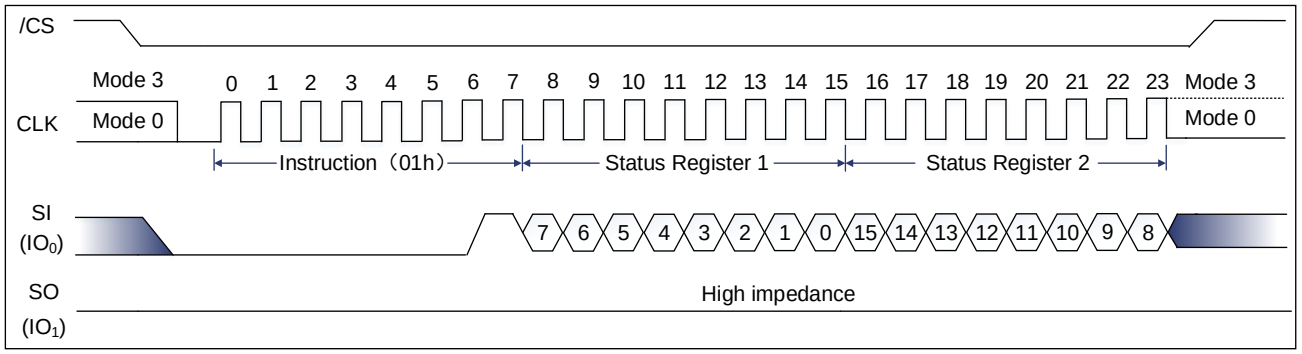


Figure 9-6 Write Status Register-1/2 Instruction (SPI Mode)

9.2.6 Read Extended Address Register (C8h)

When the device is in the 3-Byte Address Mode, the Extended Address Register is used as the 4th address byte A[31:24] to access memory regions beyond 128Mb. The Read Extended Address Register instruction is entered by driving /CS low and shifting the instruction code "C8h" into the SI pin on the rising edge of CLK. The Extended Address Register bits are then shifted out on the SO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 9-7.

When the device is in the 4-Byte Address Mode, the Extended Address Register is not used.

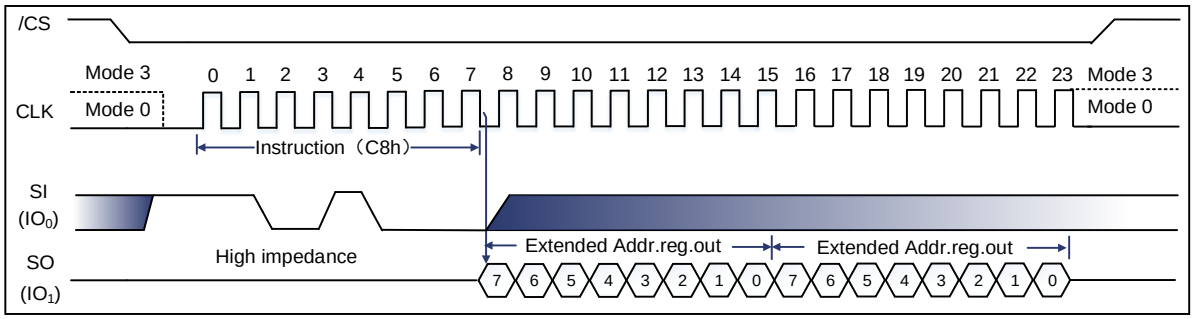


Figure 9-7 Read Extended Address Register Instruction (SPI Mode)

9.2.7 Write Extended Address Register (C5h)

The Extended Address Register is a volatile register that stores the 4th byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0). To write the Extended Address Register bits, a Write Enable (06h) instruction must previously have been executed for the device to accept the Write Extended Address Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “C5h”, and then writing the Extended Address Register data byte as illustrated in Figure 9-8.

Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register bit values will be cleared to 0.

The Extended Address Register is only effective when the device is in the 3-Byte Address Mode. When the device operates in the 4-Byte Address Mode (ADS=1), any command with address input of A31-A24 will replace the Extended Address Register values. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4-Byte to 3-Byte Address Mode.

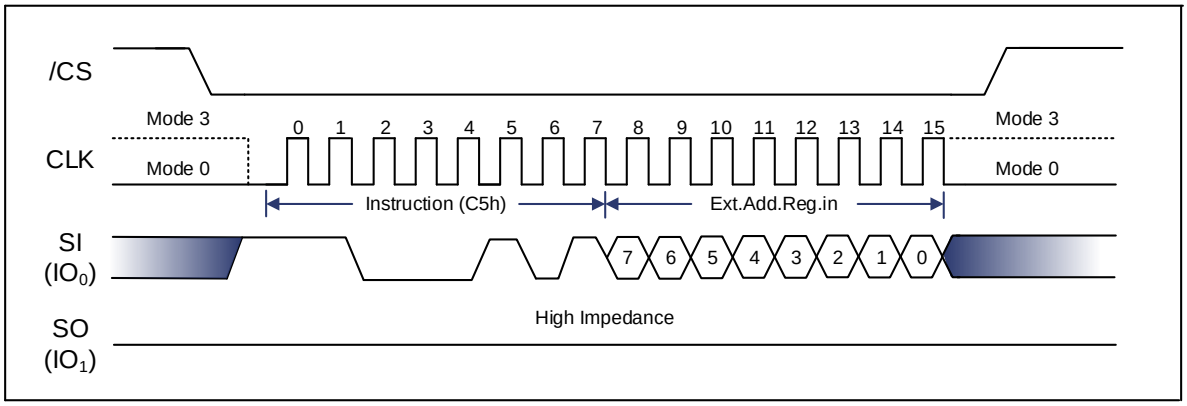


Figure 9-8 Write Extended Address Register Instruction (SPI Mode)

9.2.8 Enter 4-Byte Address Mode (B7h)

The Enter 4-Byte Address Mode instruction (Figure 9-9) will allow 32-bit address (A31-A0) to be used to access the memory array beyond 128Mb. The Enter 4-Byte Address Mode instruction is entered by driving /CS low, shifting the instruction code “B7h” into the SI pin and then driving /CS high.

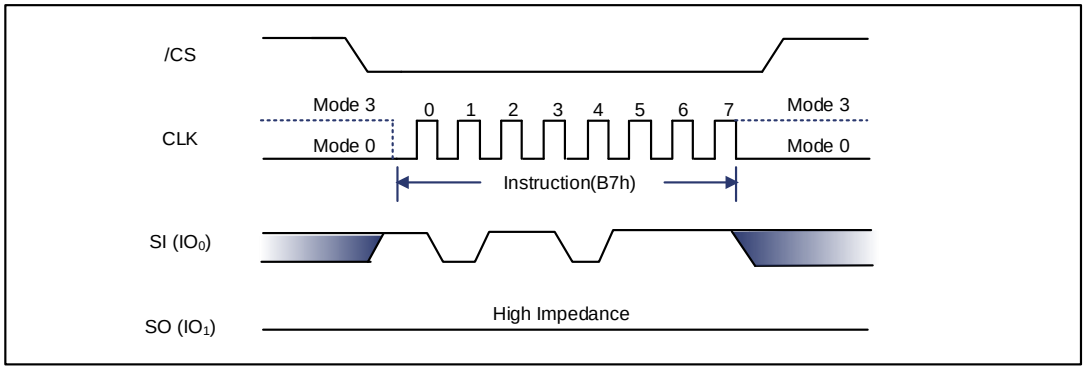


Figure 9-9 Enter 4-Byte Address Mode instruction for SPI Mode

9.2.9 Exit 4-Byte Address Mode (E9h)

In order to be backward compatible, the Exit 4-Byte Address Mode instruction (Figure 9-10) will only allow 24-bit address (A23-A0) to be used to access the memory array up to 128Mb. The Extended Address Register must be used to access the memory array beyond 128Mb. The Exit 4-Byte Address Mode instruction is entered by driving /CS low, shifting the instruction code “E9h” into the SI pin and then driving /CS high.

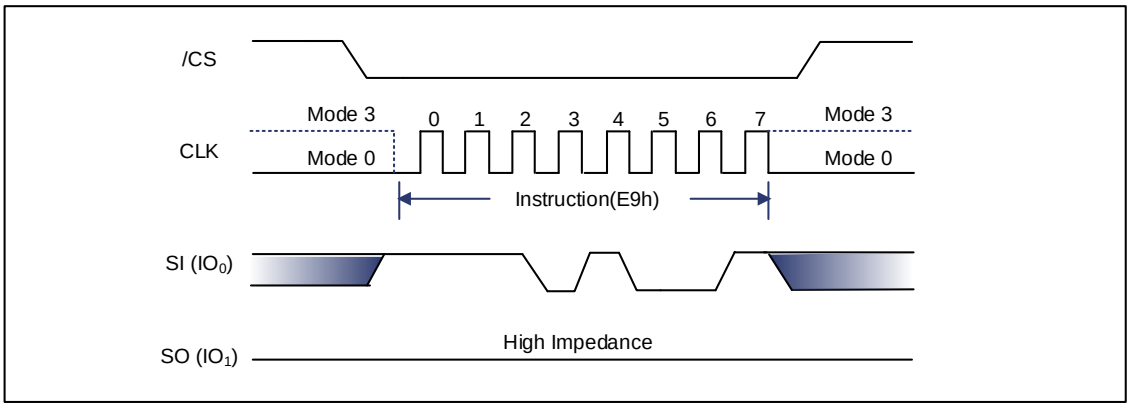


Figure 9-10 Exit 4-Byte Address Mode instruction for SPI Mode

9.2.10 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24/32-bit address into the SI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in Figure 9-11. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

The Read Data (03h) instruction is only supported in Standard SPI mode.

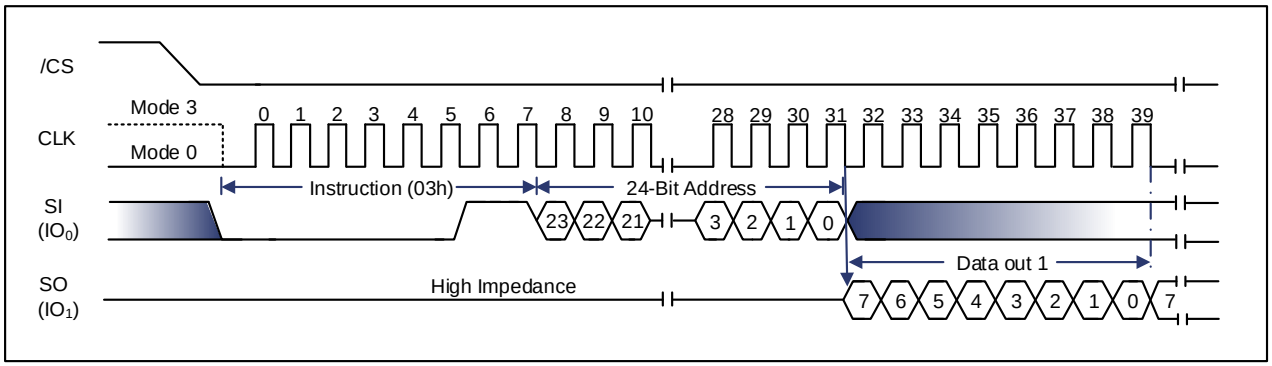


Figure 9-11 Read Data Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.2.11 Read Data with 4-Byte Address (13h)

The Read Data with 4-Byte Address instruction is similar to the Read Data (03h) instruction. Instead of 24- bit address, 32-bit address is needed following the instruction code 13h. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 512Mb memory.

The Read Data with 4-Byte Address instruction sequence is shown in Figure 9-12. If this instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data with 4-Byte Address instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

The Read Data with 4-Byte Address (13h) instruction is only supported in Standard SPI mode.

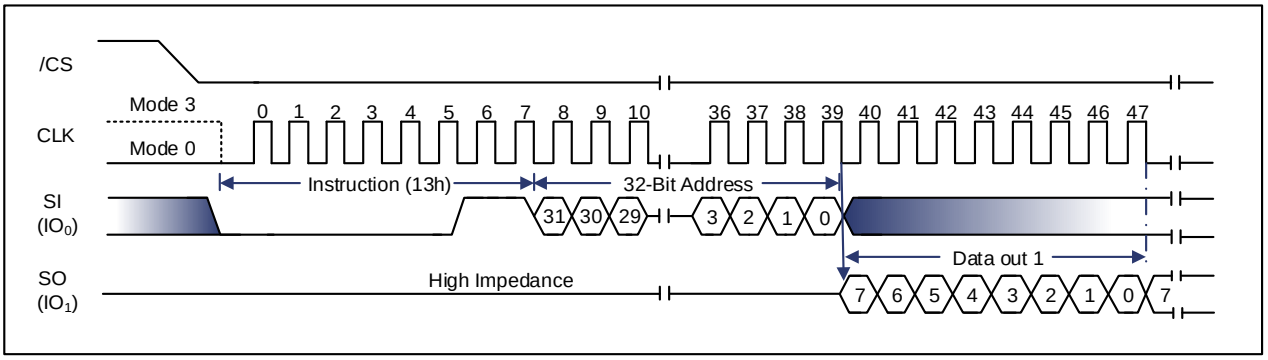


Figure 9-12 Read Data with 4-Byte Address Instruction(SPI Mode only)

9.2.12 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of fc (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24/32-bit address as shown in Figure 9-13. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the SO pin is a “don’t care”.

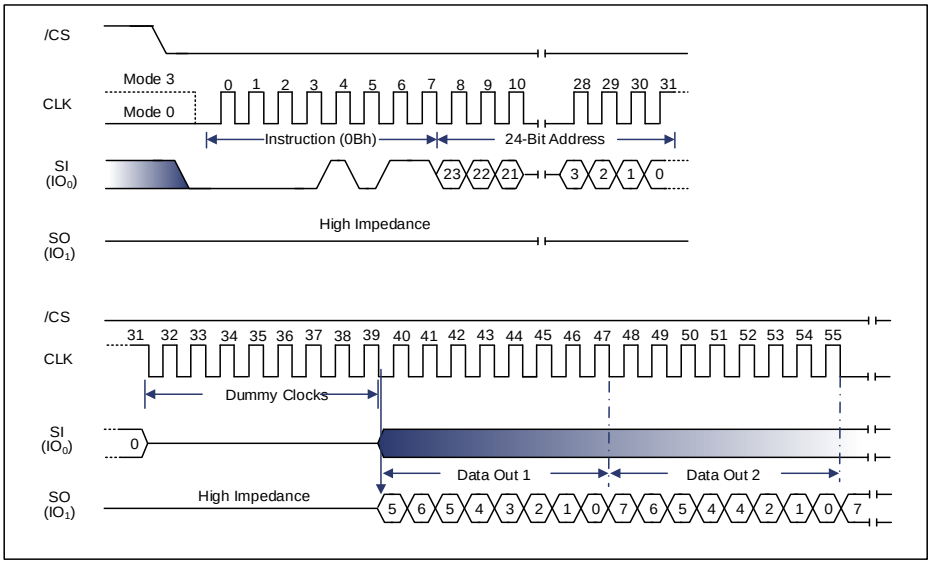


Figure 9-13 Fast Read Instruction (SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.2.13 Fast Read with 4-Byte Address (0Ch)

The Fast Read with 4-Byte Address instruction is similar to the Fast Read instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 512Mb memory. The Fast Read with 4-Byte Address (0Ch) instruction is only supported in Standard SPI mode.

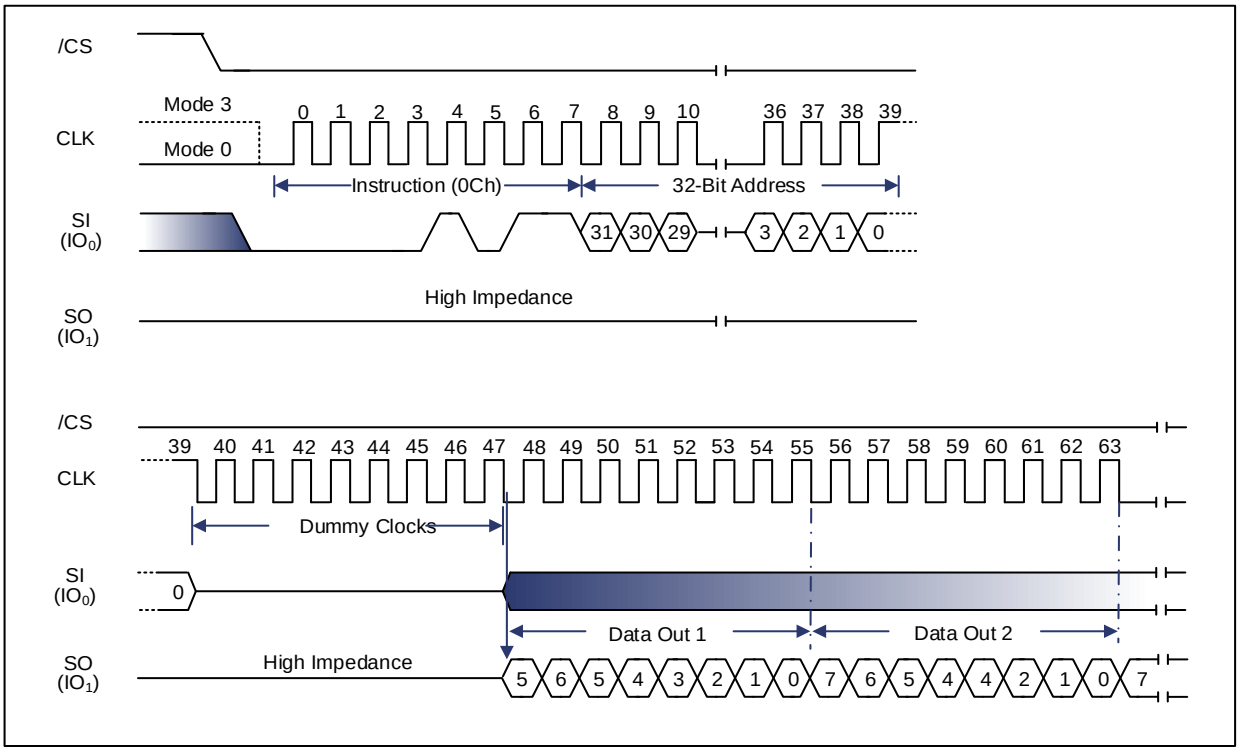


Figure 9-14 Fast Read with 4-Byte Address Instruction (SPI Mode only)

9.2.14 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO0 and IO1. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of fc (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24/32-bit address as shown in Figure 9-15. The dummy clocks allow the device’s internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO0 pin should be high-impedance prior to the falling

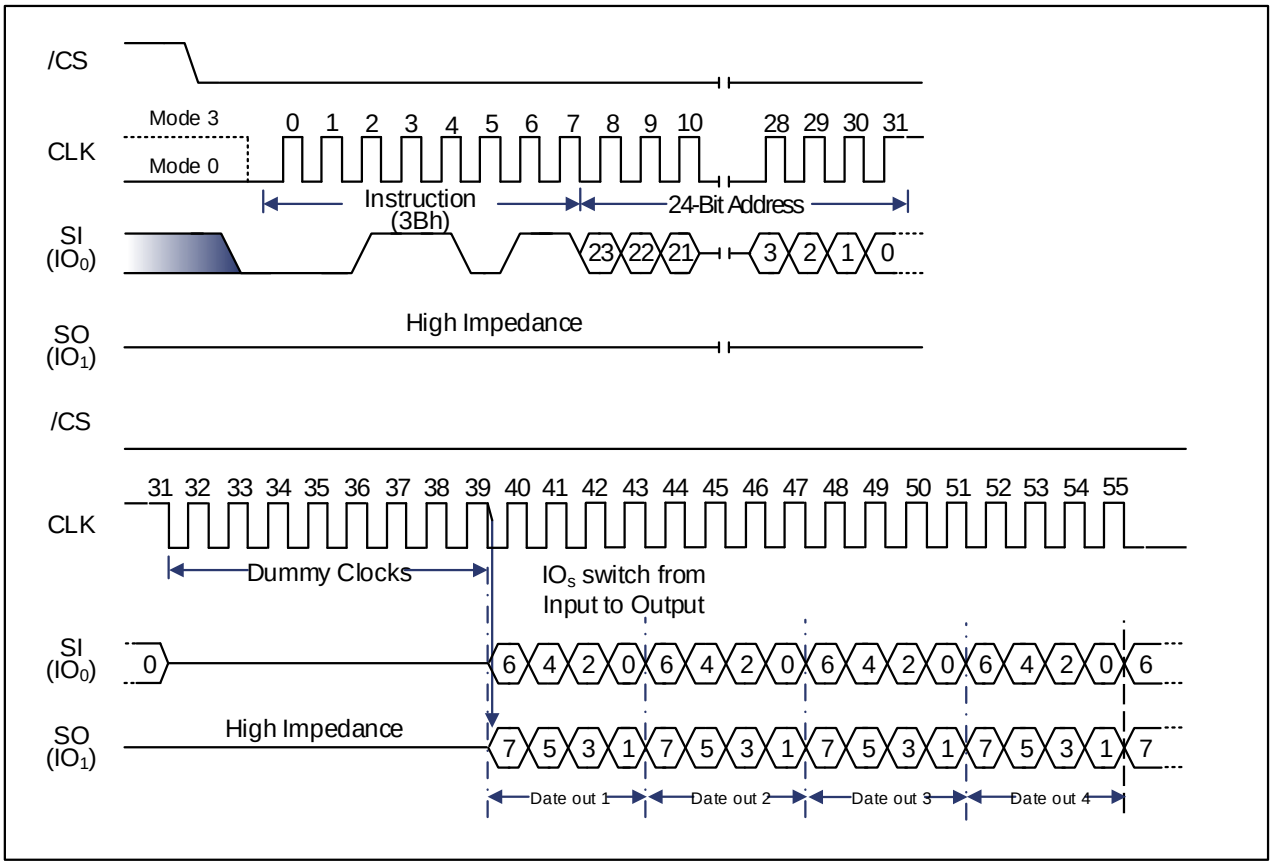


Figure 9-15 Fast Read Dual Output Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.2.15 Fast Read Dual Output with 4-Byte Address (3Ch)

The Fast Read Dual Output with 4-Byte Address instruction is similar to the Fast Read Dual Output instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Dual Output with 4-Byte Address instruction will always require 32-bit address to access the entire 512Mb memory.

The Fast Read Dual Output with 4-Byte Address (3Ch) instruction is only supported in Standard SPI mode.

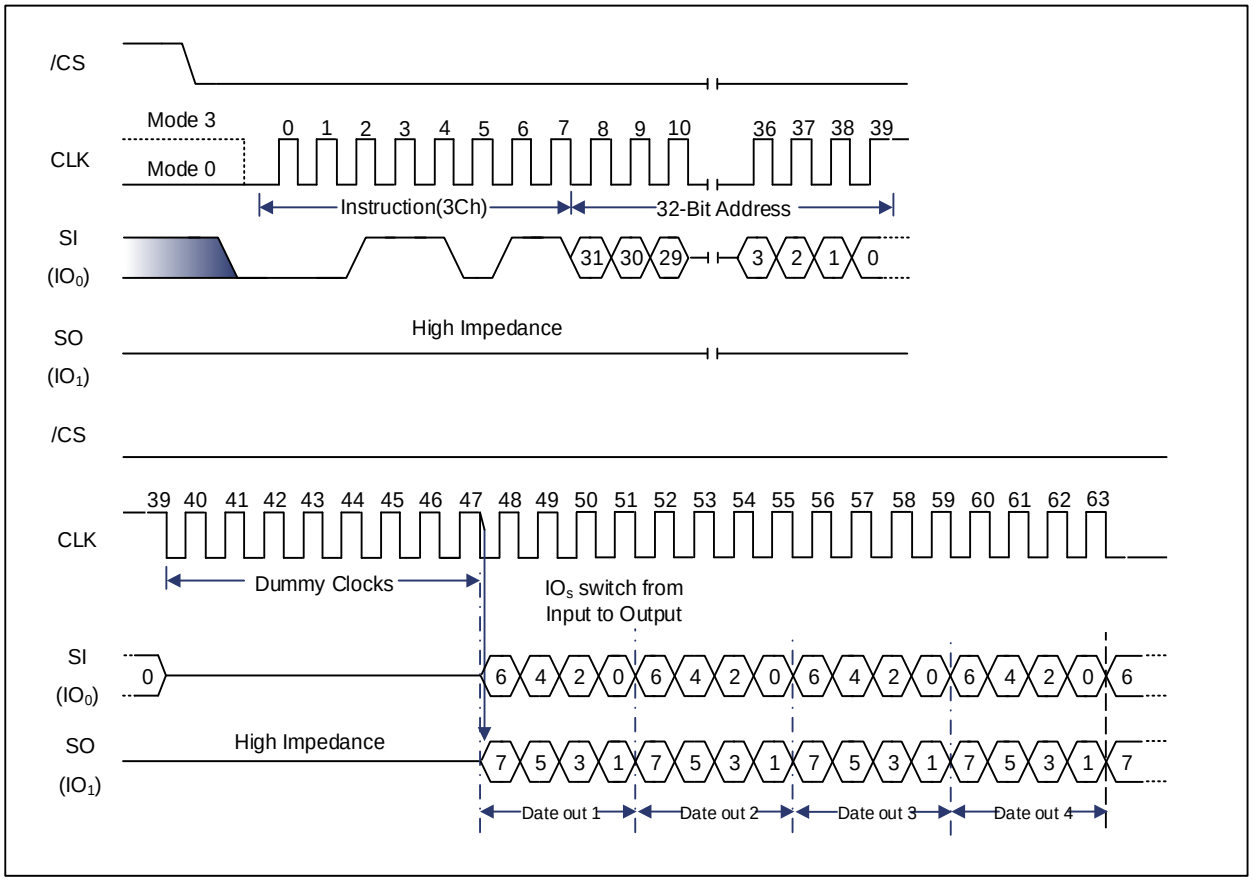


Figure 9-16 Fast Read Dual Output with 4-Byte Address Instruction (SPI Mode only)

9.2.16 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO0, IO1, IO2, and IO3. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of fc (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24/32-bit address as shown in Figure 9-17. The dummy clocks allow the device’s internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

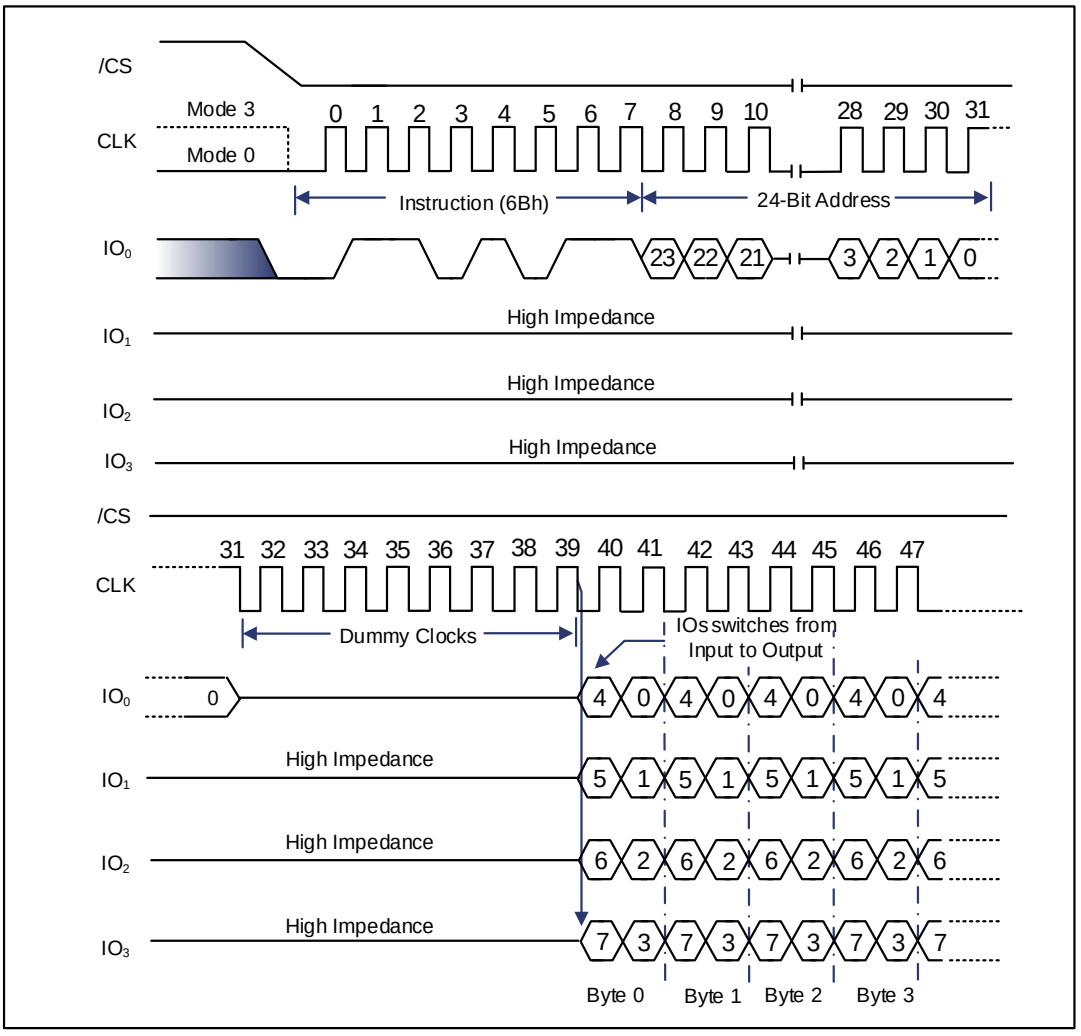


Figure 9-17 Fast Read Quad Output Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.2.17 Fast Read Quad Output with 4-Byte Address (6Ch)

The Fast Read Quad Output with 4-Byte Address instruction is similar to the Fast Read Quad Output instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad Output with 4-Byte Address instruction will always require 32-bit address to access the entire 512Mb memory.

The Fast Read Quad Output with 4-Byte Address (6Ch) instruction is only supported in Standard SPI mode.

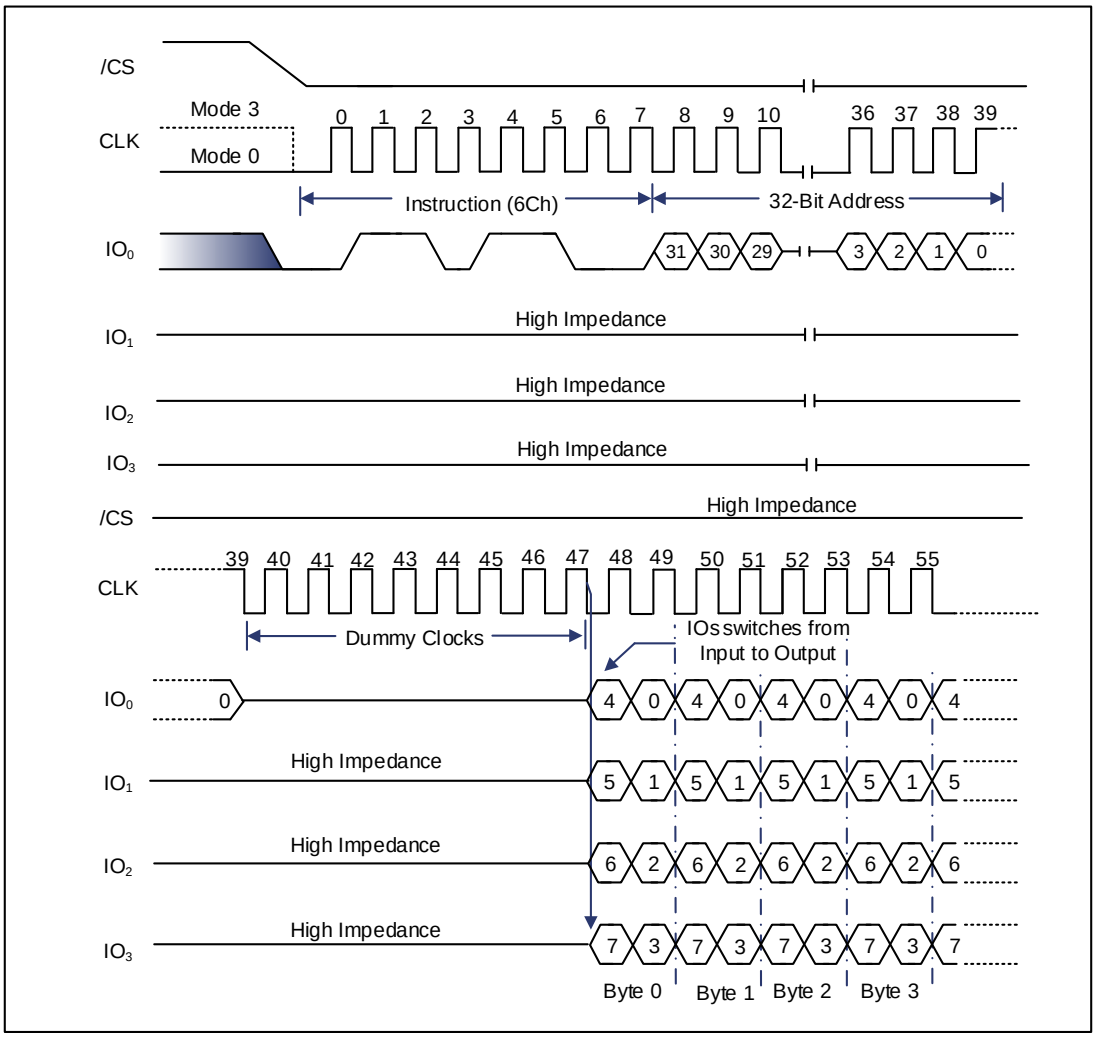


Figure 9-18 Fast Read Quad Output with 4-Byte Address Instruction (SPI Mode only)

9.2.18 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23/A31-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

- **Fast Read Dual I/O with "Read Command Bypass Mode"**

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23/A31-0), as shown in Figure 9-19. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in Figure 9-20. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFh on IO0 for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

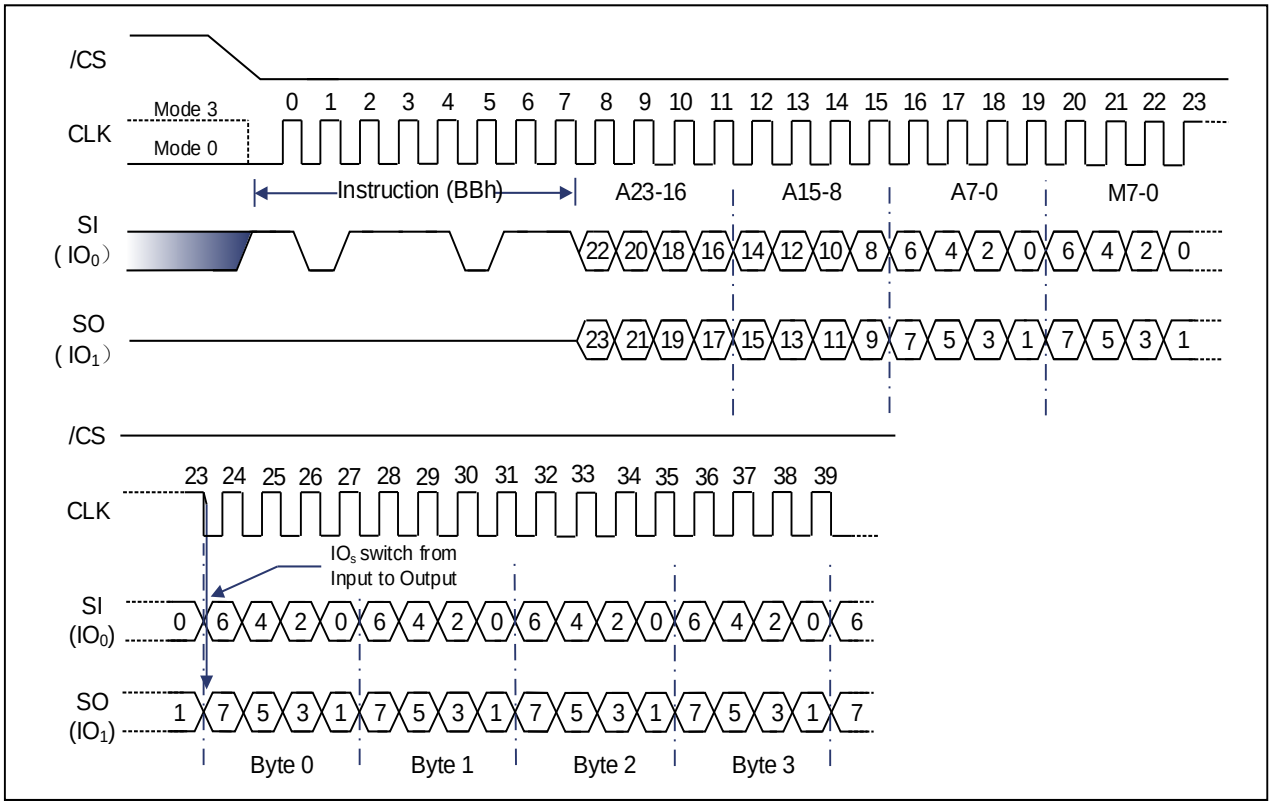


Figure 9-19 Fast Read Dual I/O (Initial instruction or previous M5-4 10, SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

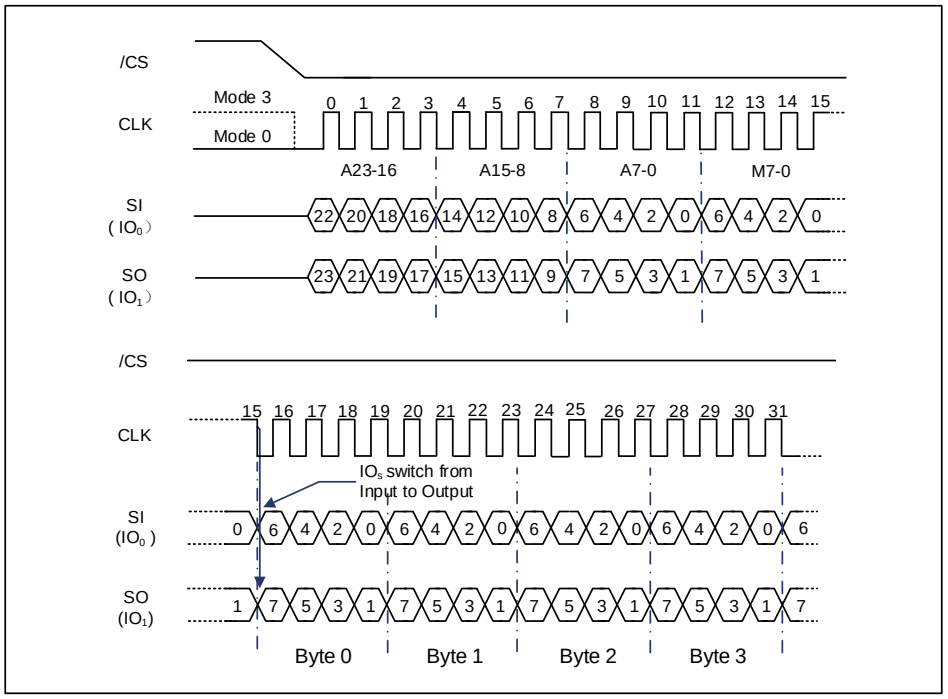


Figure 9-20 Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode only)
32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.2.19 Fast Read Dual I/O with 4-Byte Address (BCh)

The Fast Read Dual I/O with 4-Byte Address instruction is similar to the Fast Read Dual I/O instruction except that it requires 32-bit address instead of 24/32-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Dual I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 512Mb memory.

The Fast Read Dual I/O with 4-Byte Address (BCh) instruction is only supported in Standard SPI mode.

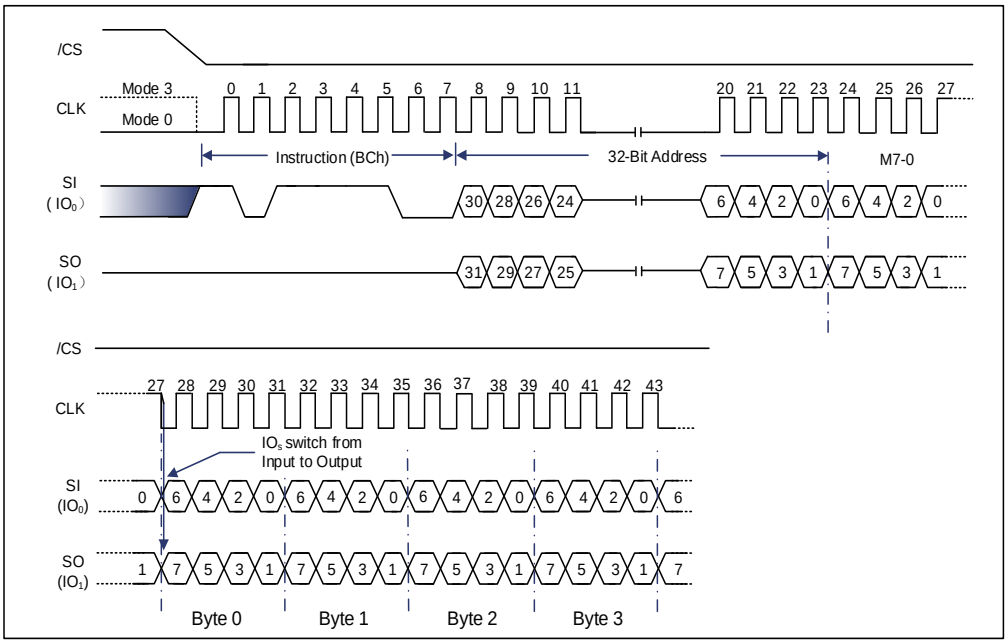


Figure 9-21 Fast Read Dual I/O with 4-Byte Address Instruction. (Previous instruction set M5-4 ≠ 10, SPI Mode only)

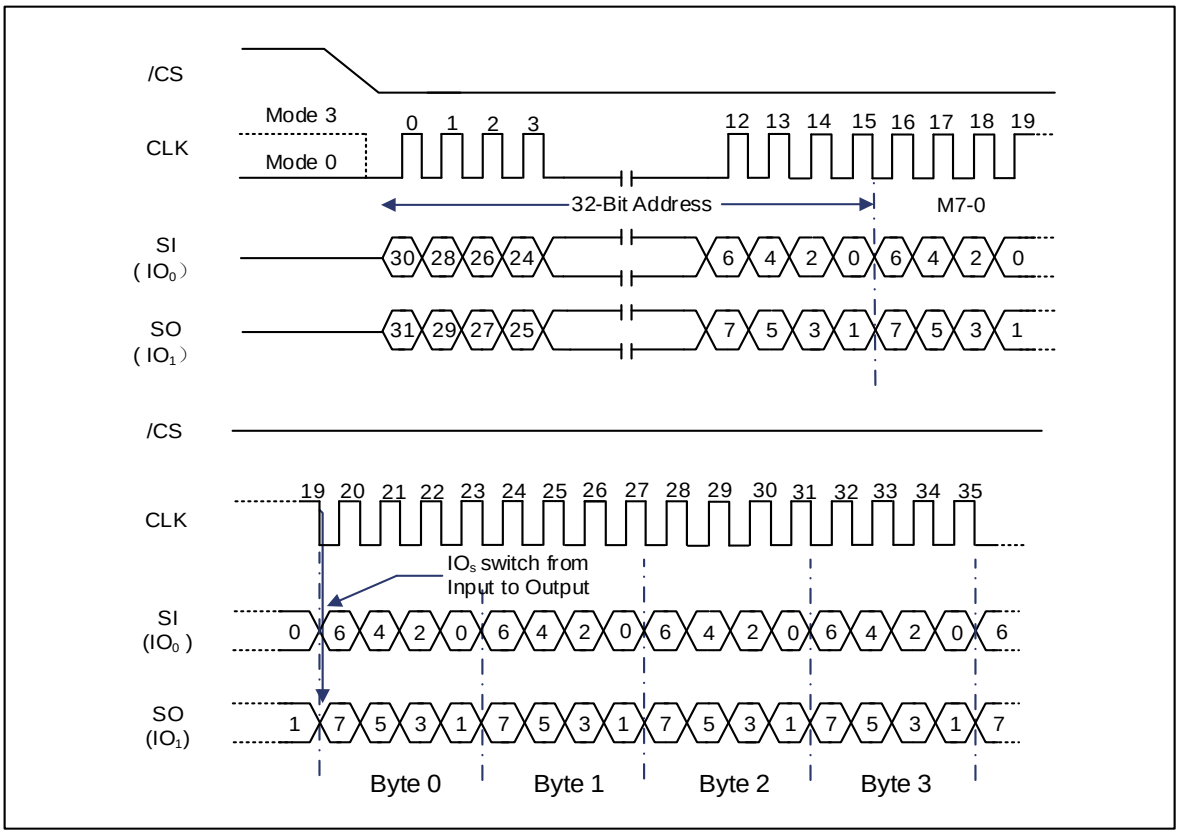


Figure 9-22 Fast Read Dual I/O w/ 4-Byte Addr. (Initial instruction or previous M5-4 = 10, SPI Mode only)

9.2.20 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

- **Fast Read Quad I/O with "Read Command Bypass Mode"**

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the Read Command Bypass Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 9-23. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Read Command Bypass Mode bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 9-24. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the Read Command Bypass Mode bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

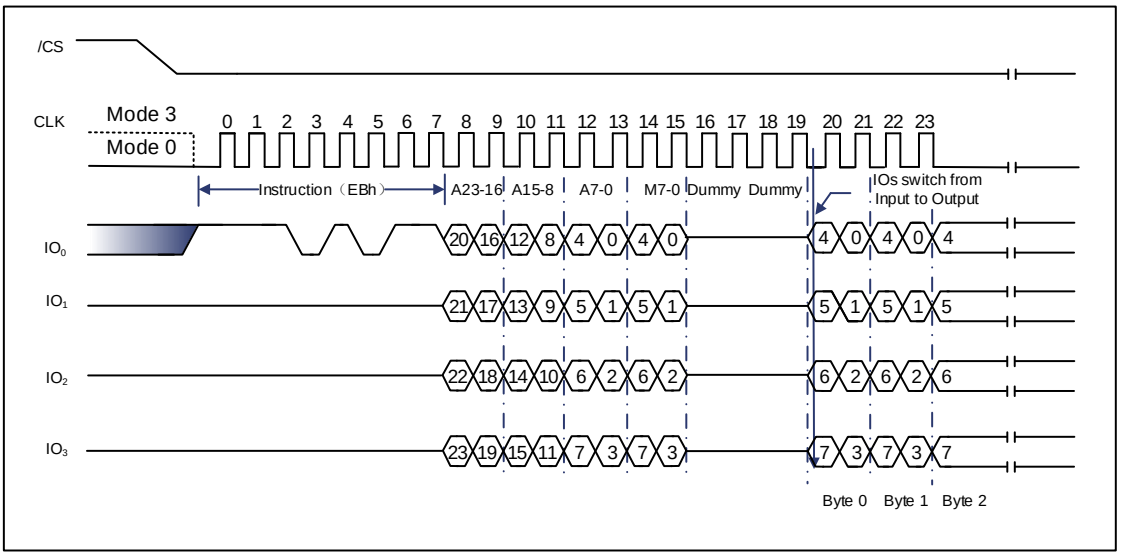


Figure 9-23 Fast Read Quad I/O (Initial instruction or previous M5-4 ≠ 10, SPI Mode)
32-Bit Address is required when the device is operating in 4-Byte Address Mode

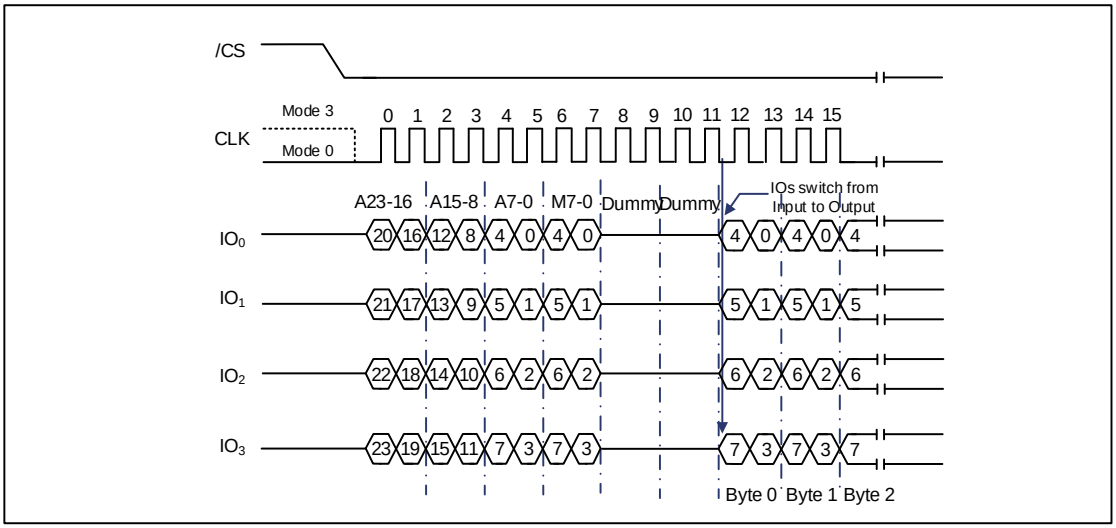


Figure 9-24 Fast Read Quad I/O Instruction (Previous instruction set M5-4 ≠ 10, SPI Mode)

- **Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode**

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64- byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

9.2.21 Fast Read Quad I/O with 4-Byte Address (ECh)

The Fast Read Quad I/O with 4-Byte Address instruction is similar to the Fast Read Quad I/O instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 512Mb memory.

The Fast Read Quad I/O with 4-Byte Address (ECh) instruction is only supported in Standard SPI mode.

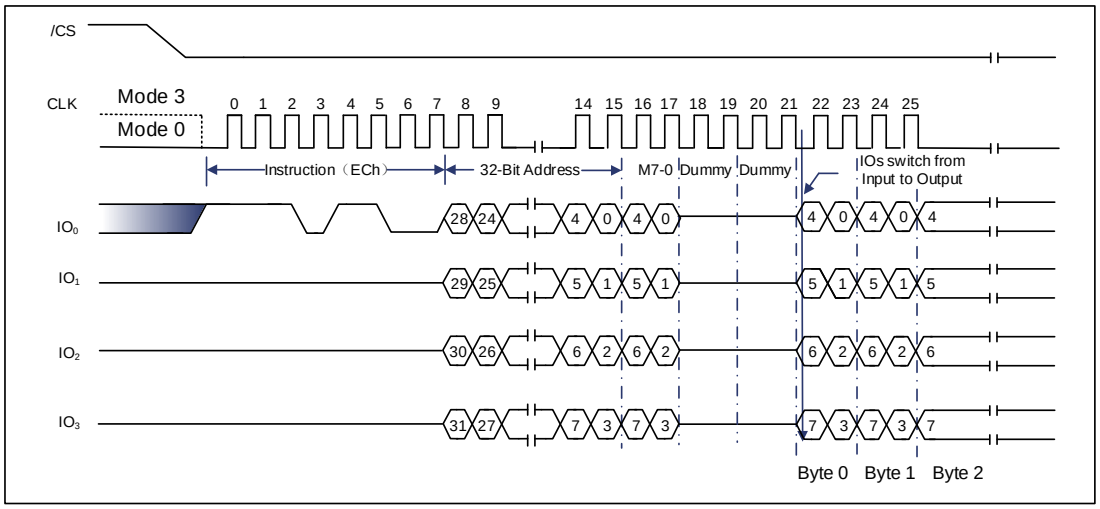


Figure 9-25 Fast Read Quad I/O w/ 4-Byte Addr. (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)

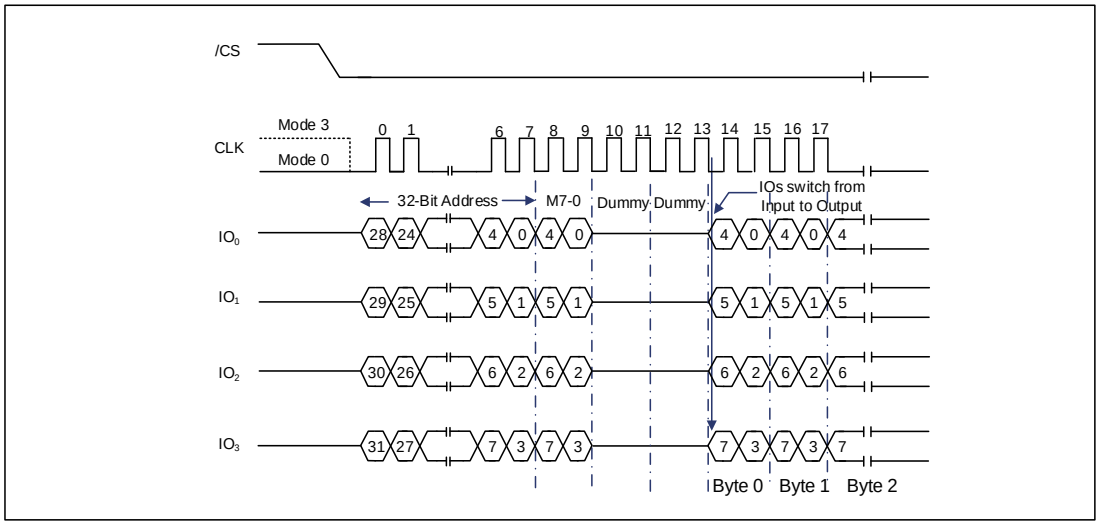


Figure 9-26 Fast Read Quad I/O w/ 4-Byte Addr. (Previous instruction set M5-4=10, SPI Mode only)

● **Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode**

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to Ech. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following Ech commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section 9.2.24 for detail descriptions.

9.2.22 Word Read Quad I/O (E7h)

The Word Read Quad I/O (E7h) instruction is similar to the Fast Read Quad I/O (EBh) instruction except that the lowest Address bit (A0) must equal 0 and only two Dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O Instruction.

● **Word Read Quad I/O with "Continuous Read Mode"**

The Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23/A31-0), as shown Figure 9-27. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the E7h instruction code, as shown in Figure 9-28. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

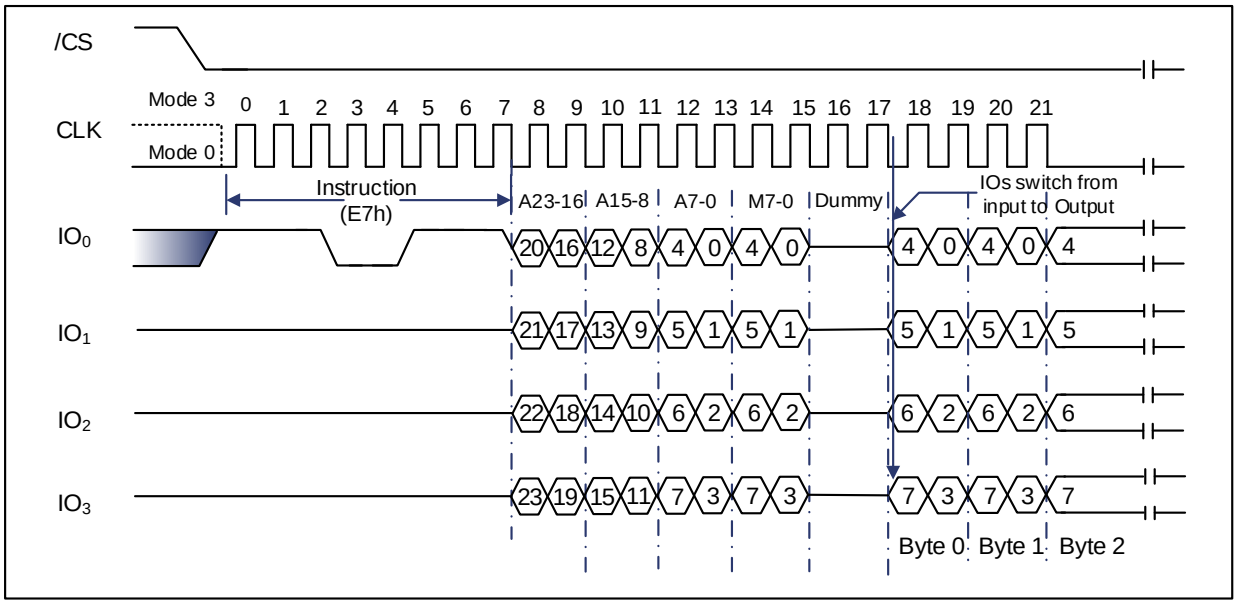


Figure 9-27 Word Read Quad I/O Instruction (Initial instruction or previous M5-4 10, SPI Mode only)
32-Bit Address is required when the device is operating in 4-Byte Address Mode

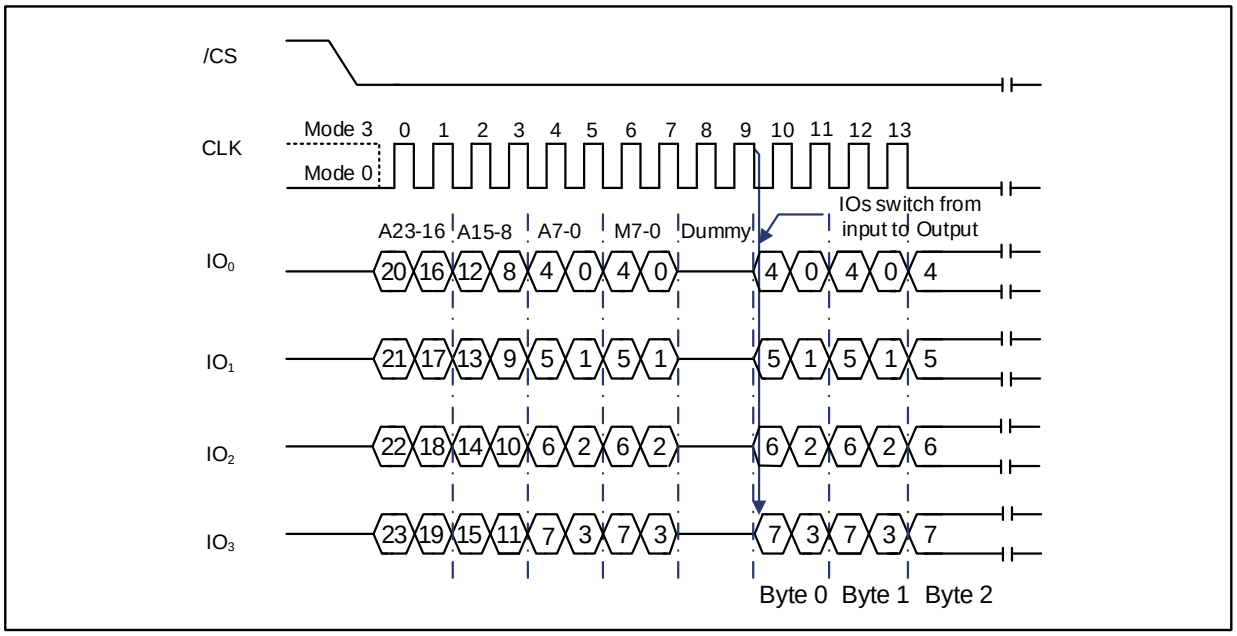


Figure 9-28 Word Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)
32-Bit Address is required when the device is operating in 4-Byte Address Mode

- **Word Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode**

The Word Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to E7h. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following E7h commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64- byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See 7.2.23 for detail descriptions.

9.2.23 Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) instruction is used in conjunction with “Fast Read Quad I/O” and “Word Read Quad I/O” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24/32 dummy bits and 8 “Wrap Bits”, W7-0. The instruction sequence is shown in Figure 9-29. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5		W4=0		W4 =1 (DEFAULT)	
		Wrap Around	Wrap Length	Wrap Around	Wrap Length
0	0	Yes	8-byte	No	N/A
0	1	Yes	16-byte	No	N/A
1	0	Yes	32-byte	No	N/A
1	1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following “Fast Read Quad I/O(EBh)” instruction will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

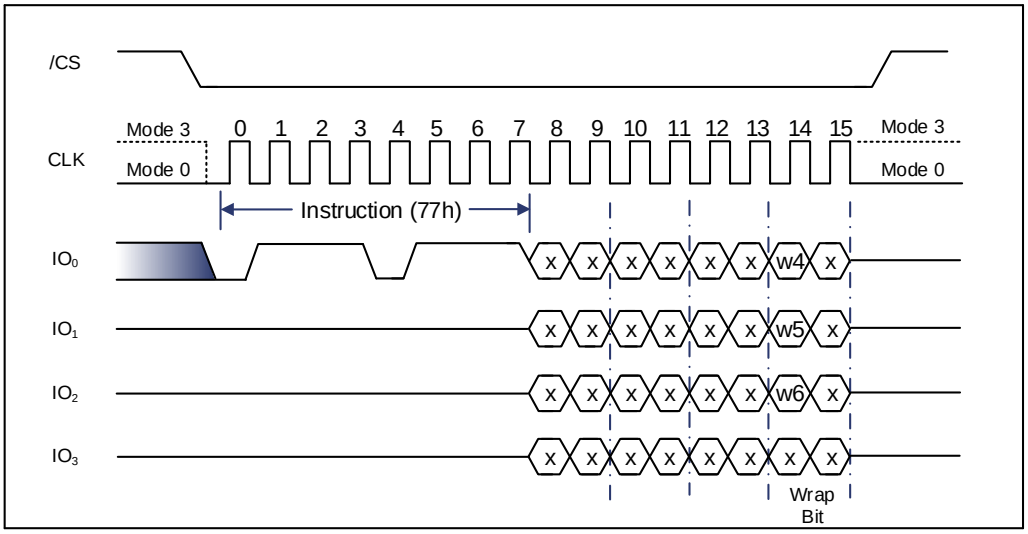


Figure 9-29 Set Burst with Wrap Instruction (SPI Mode only)

9.2.24 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24/32-bit address (A23/A31-A0) and at least one data byte, into the SI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in Figure 9-30.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3,BP2, BP1, and BP0) bits.

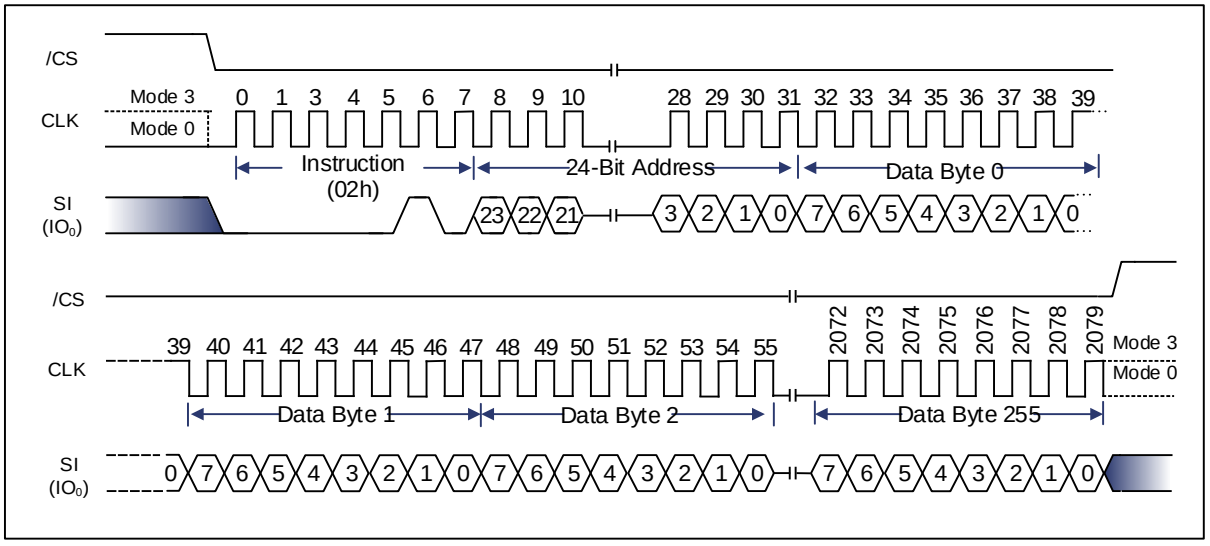


Figure 9-30 Page Program Instruction (SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.2.25 Page Program with 4-Byte Address (12h)

The Page Program with 4-Byte Address instruction is similar to the Page Program instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Page Program with 4-Byte Address instruction will always require 32-bit address to access the entire 512Mb memory.

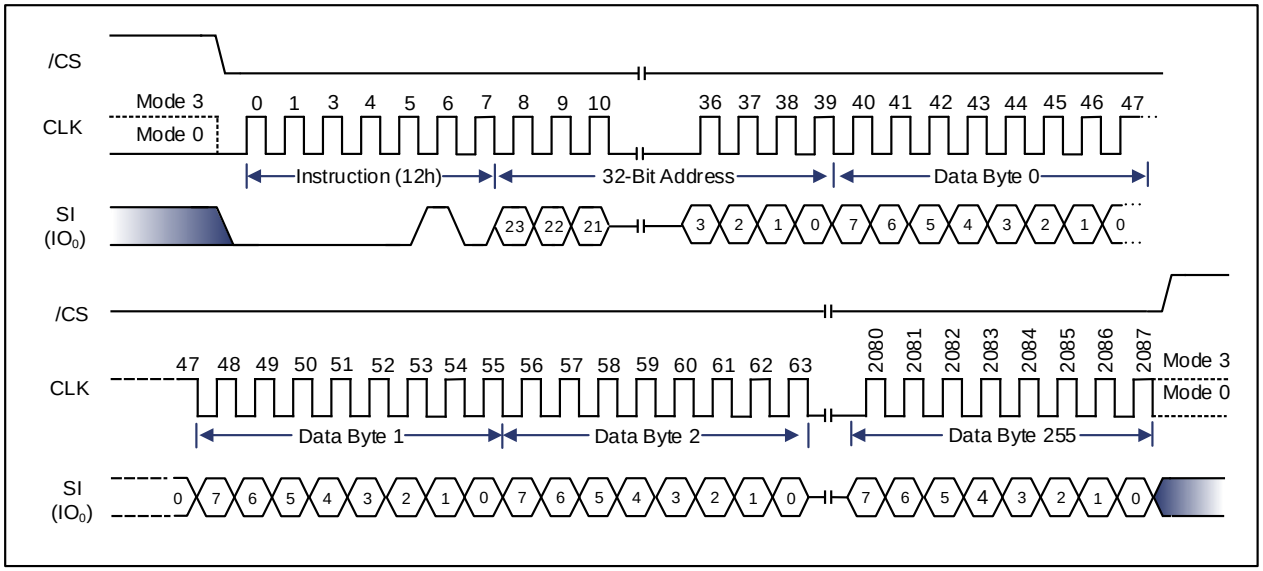


Figure 9-31 Page Program with 4-Byte Addr. (SPI Mode Only)

9.2.26 Quad Input Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO0, IO1, IO2, and IO3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “32h” followed by a 24/32-bit address (A23/A31-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 9-32.

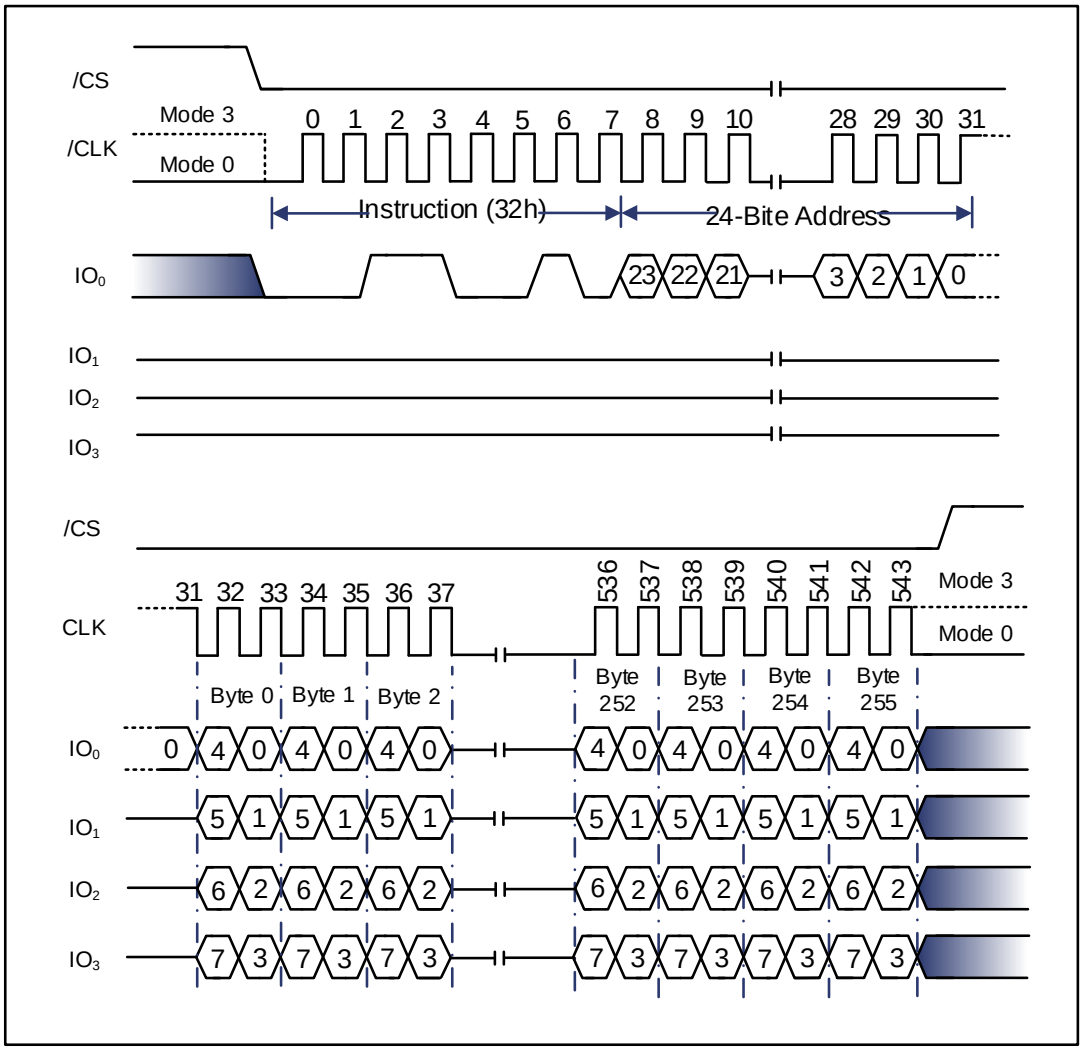


Figure 9-32 Quad Input Page Program Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.2.27 Quad Page Program (33h)

The Quad Page Program (33h) instruction is similar to the Quad Input Page Program (32h) instruction except that address and data bits are both input and output through four pins IO0, IO1, IO2 and IO3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data. To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. The Quad Page Program instruction sequence is shown in Figure 9-33.

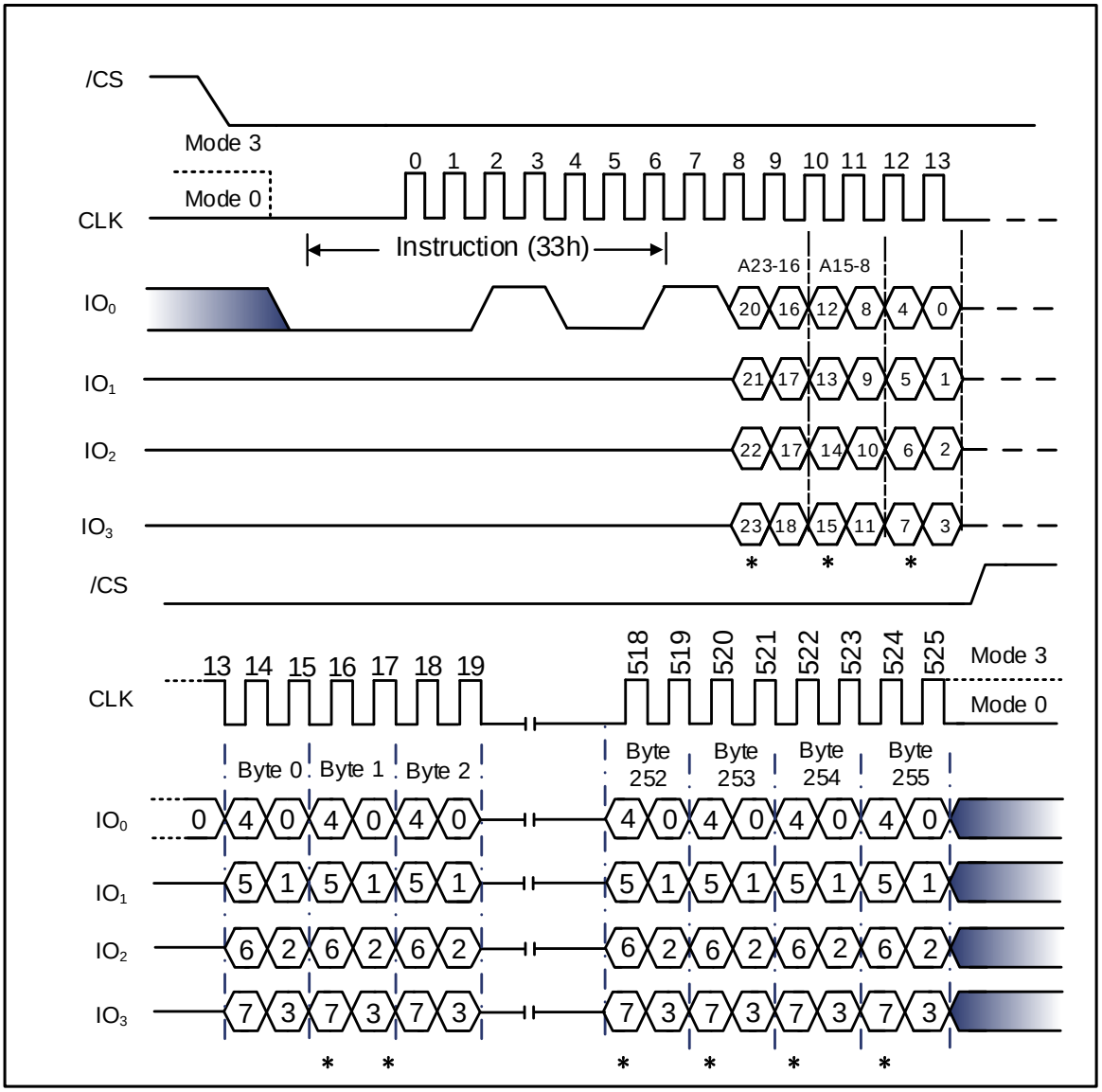


Figure 9-33 Quad Page Program Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.2.28 Quad Input Page Program with 4-Byte Address (34h)

The Quad Input Page Program with 4-Byte Address instruction is similar to the Quad Input Page Program instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Quad Input Page Program with 4-Byte Address instruction will always require 32-bit address to access the entire 512Mb memory.

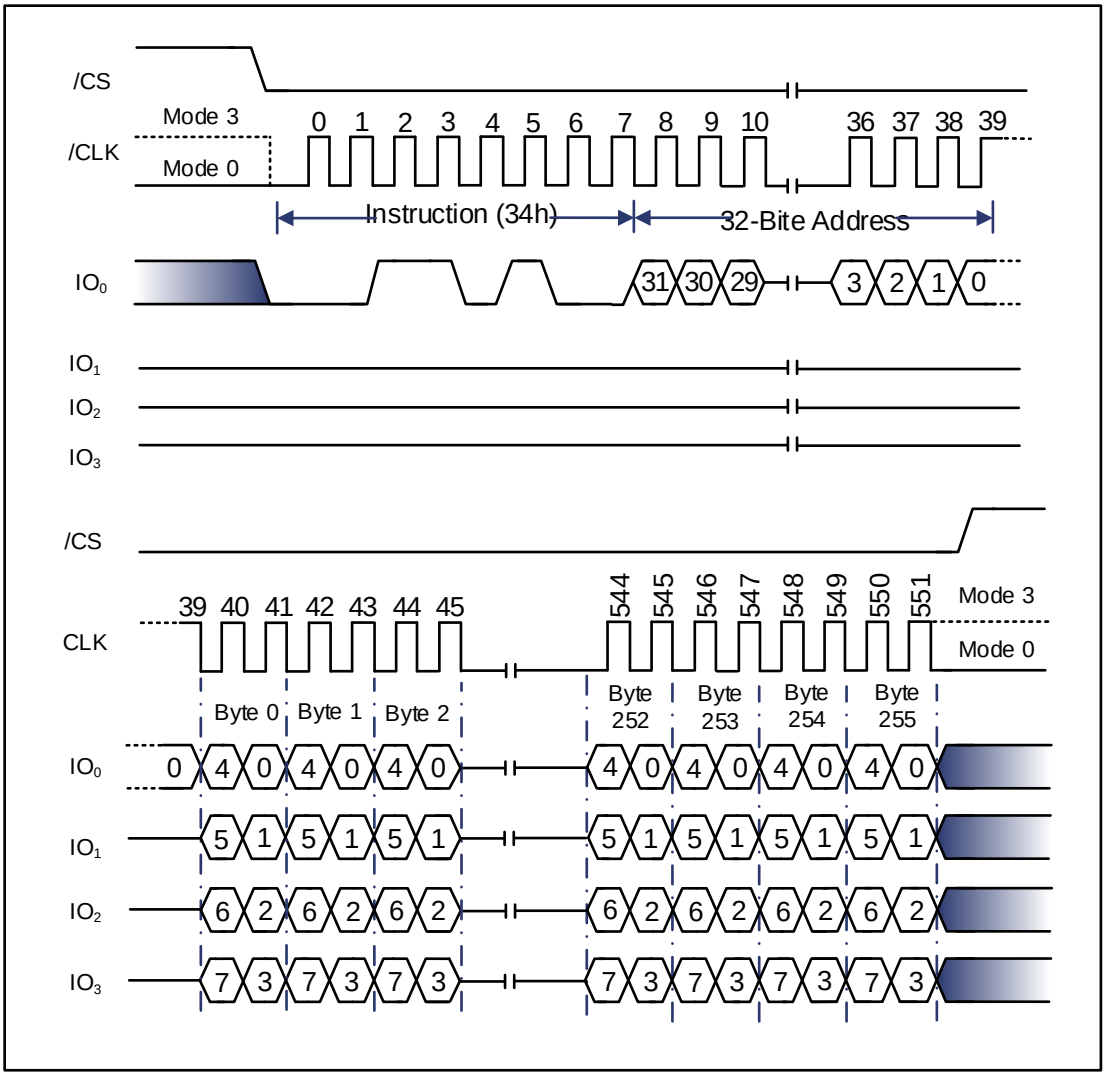


Figure 9-34 Quad Input Page Program with 4-Byte Addr. (SPI Mode only)

9.2.29 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23 -A0). The Sector Erase instruction sequence is shown in Figure 9-35.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits.

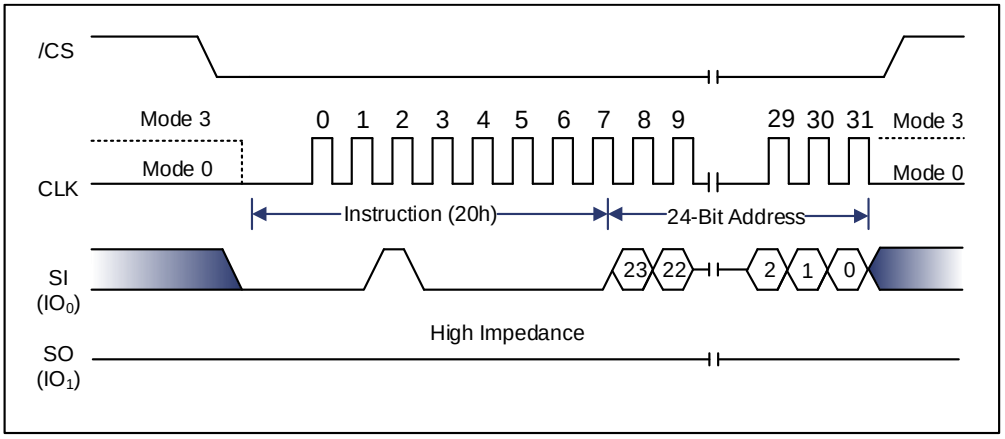


Figure 9-35 Sector Erase Instruction (SPI Mode)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.2.30 Sector Erase with 4-Byte Address (21h)

The Sector Erase with 4-Byte Address instruction is similar to the Sector Erase instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Sector Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 512Mb memory.

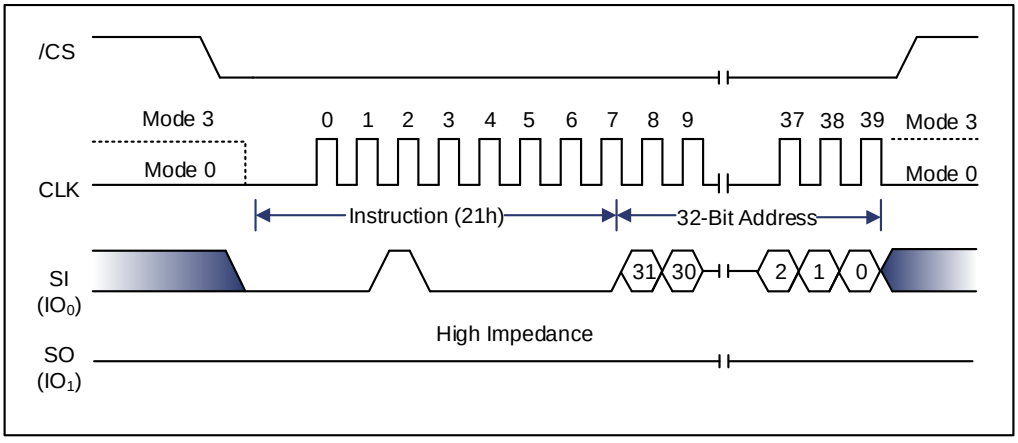


Figure 9-36 Sector Erase with 4-Byte Address Instruction (SPI Mode Only)

9.2.31 32KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” followed a 24/32-bit block address (A23/A31-A0). The Block Erase instruction sequence is shown in Figure 9-37.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE1 (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits.

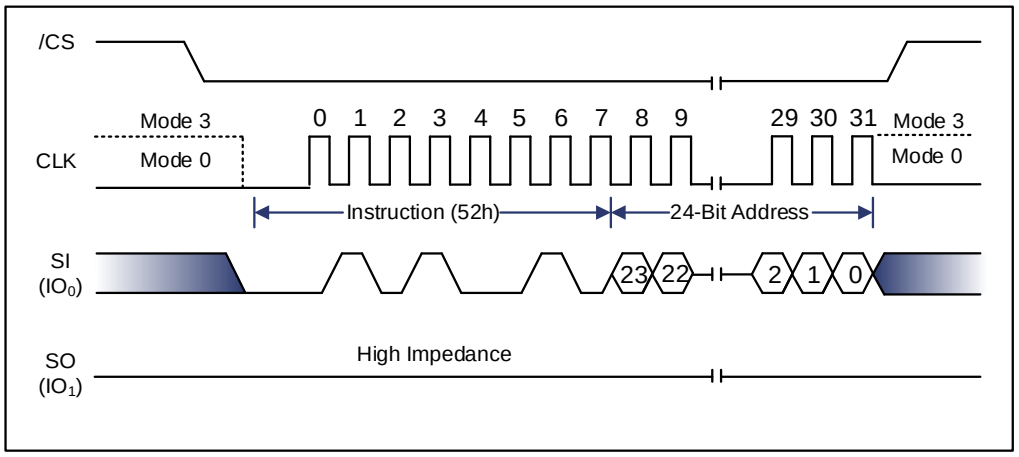


Figure 9-37 32KB Block Erase Instruction (SPI Mode)

9.2.32 32KB Block Erase with 4-Byte Address (5Ch)

The 32KB Block Erase with 4-Byte Address instruction (5Ch) is similar to the32KB Block Erase instruction (52h) except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 512Mb memory.

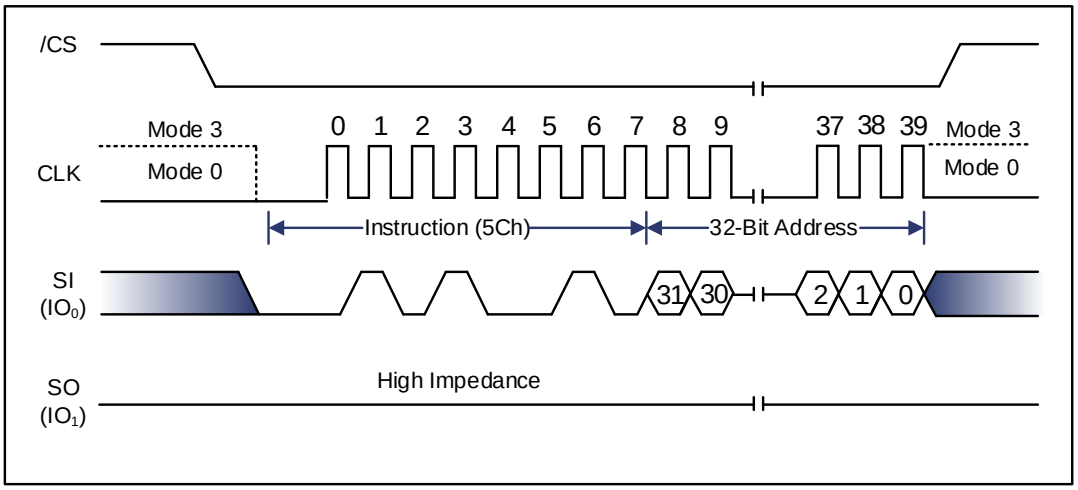


Figure 9-38 32KB Block Erase with 4-Byte Address Instruction (SPI Mode)

9.2.33 64KB Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24/32-bit block address (A23/A31-A0). The Block Erase instruction sequence is shown in Figure 9-39.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits.

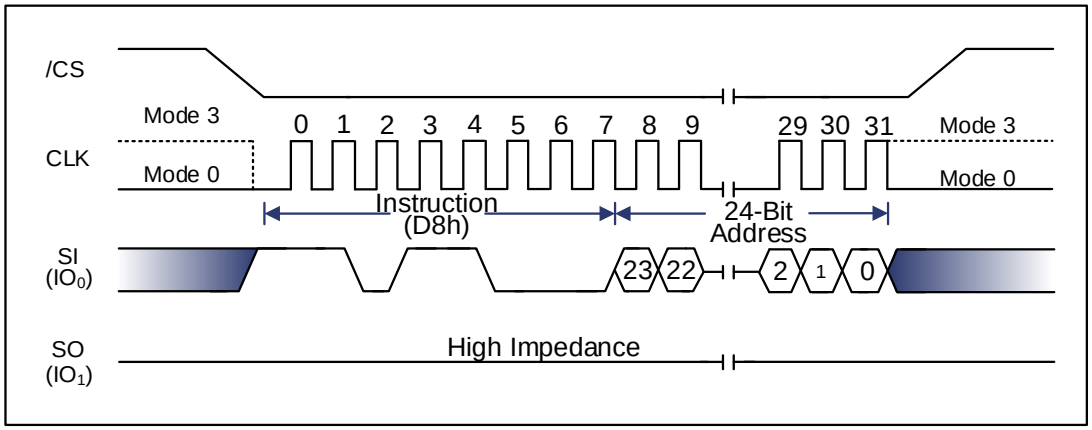


Figure 9-39 64KB Block Erase Instruction (SPI Mode)

9.2.34 64KB Block Erase with 4-Byte Address (DCh)

The 64KB Block Erase with 4-Byte Address instruction is similar to the 64KB Block Erase instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the 64KB Block Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 512Mb memory.

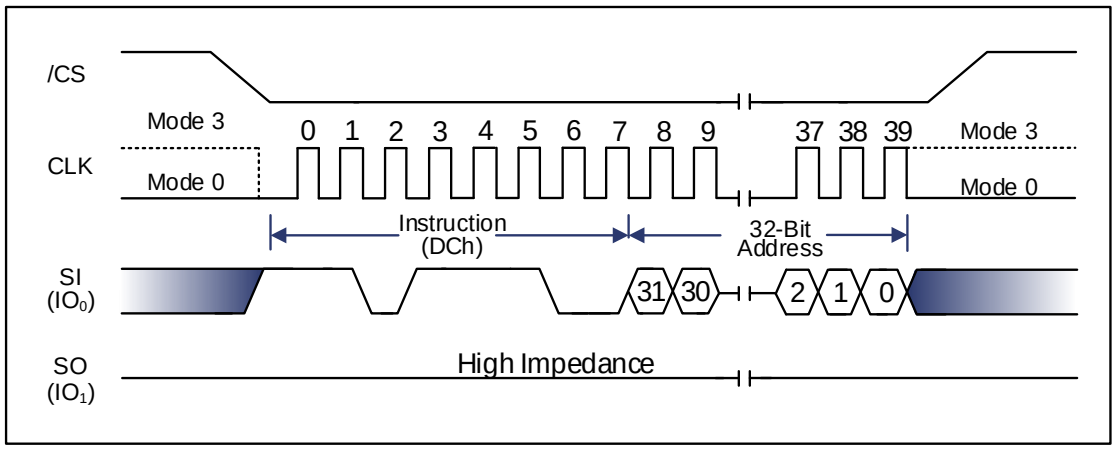


Figure 9-40 64KB Block Erase with 4-Byte Address Instruction (SPI Mode)

9.2.35 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown Figure 9-41.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (CMP, TB, BP3, BP2, BP1, and BP0) bits. Both active/non-active die are erased during internal Chip Erase operation. Chip Erase operations is detailed on the Two Die Stack Operations section.

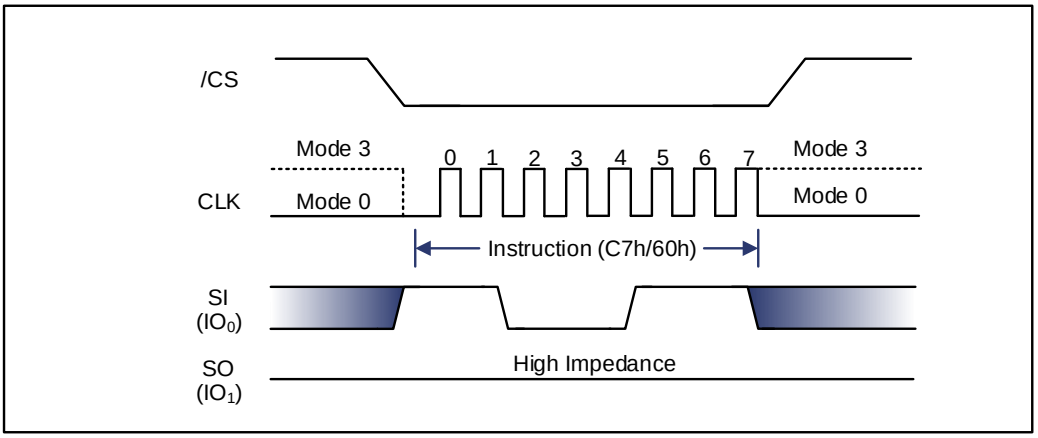


Figure 9-41 Chip Erase Instruction for SPI Mode

9.2.36 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in Figure 9-42.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h,42h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instructions (01h, 31h, 11h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h) and Program instructions (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “tSUS” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “tSUS” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “tSUS” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

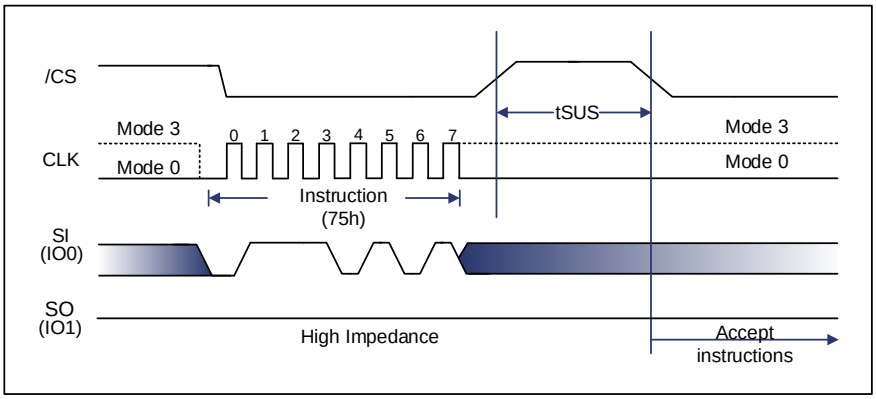


Figure 9-42 Erase/Program Suspend Instruction (SPI Mode)

9.2.37 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 9-43.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “tERS” following a previous Resume instruction.

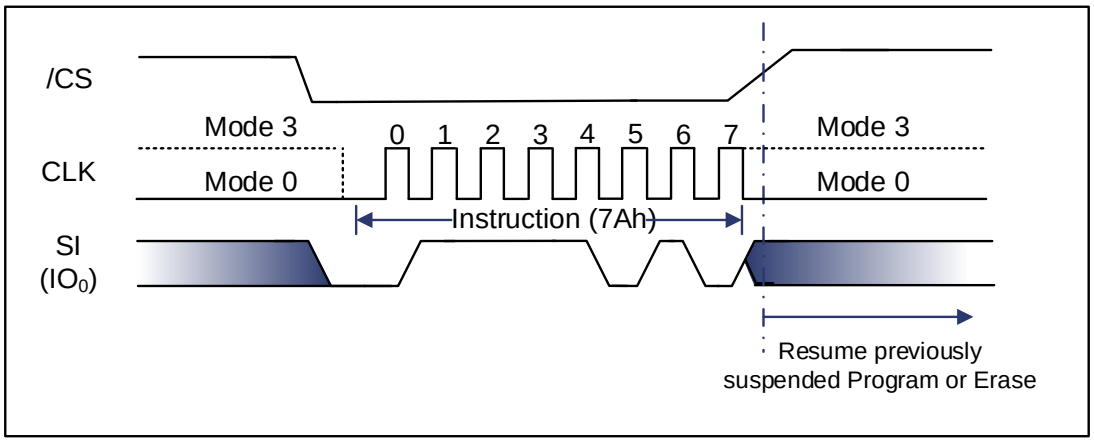


Figure 9-43 Erase/Program Resume Instruction (SPI Mode)

9.2.38 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in Figure 9-44.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP (See AC Characteristics). While in the power-down state only the Release Power-down (ABh) instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

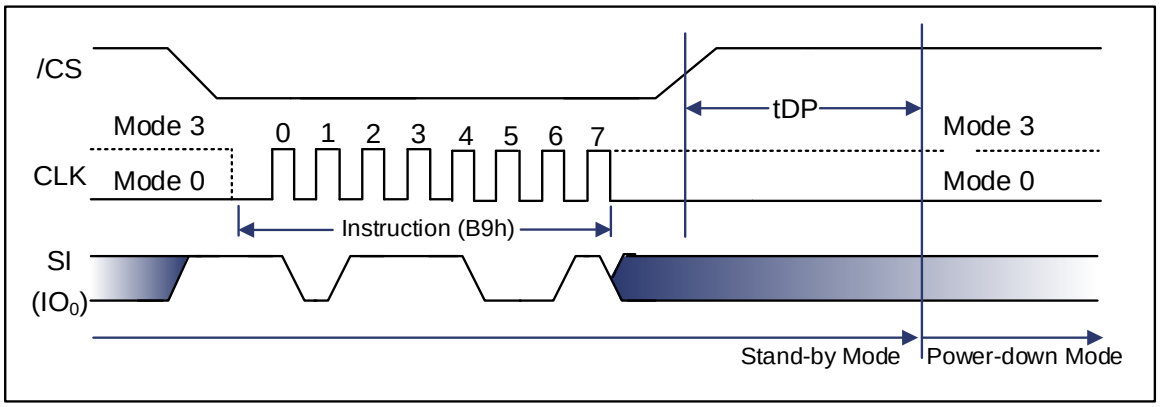


Figure 9-44 Deep Power-down Instruction (SPI Mode)

9.2.39 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in Figure 9-45. Release from power-down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first. The Device ID values for the XM25RU512Dis listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 9-46, except that after /CS is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

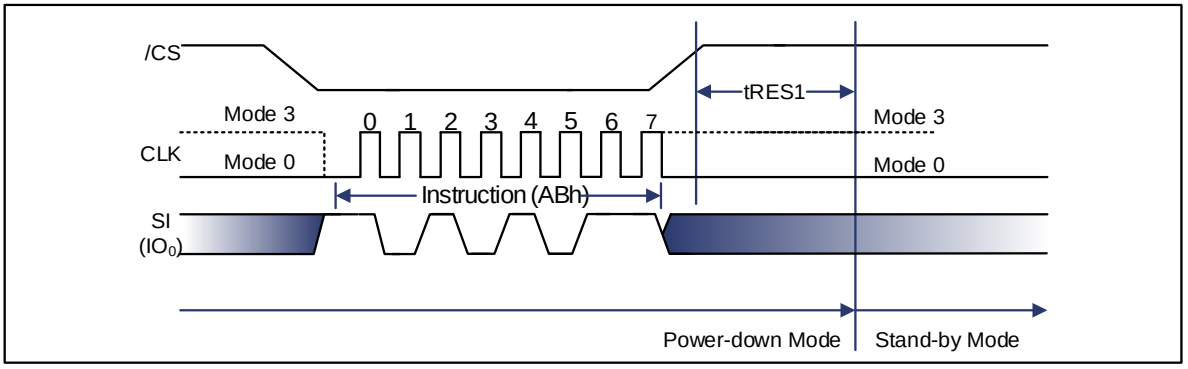


Figure 9-45 Release Power-down Instruction (SPI Mode)

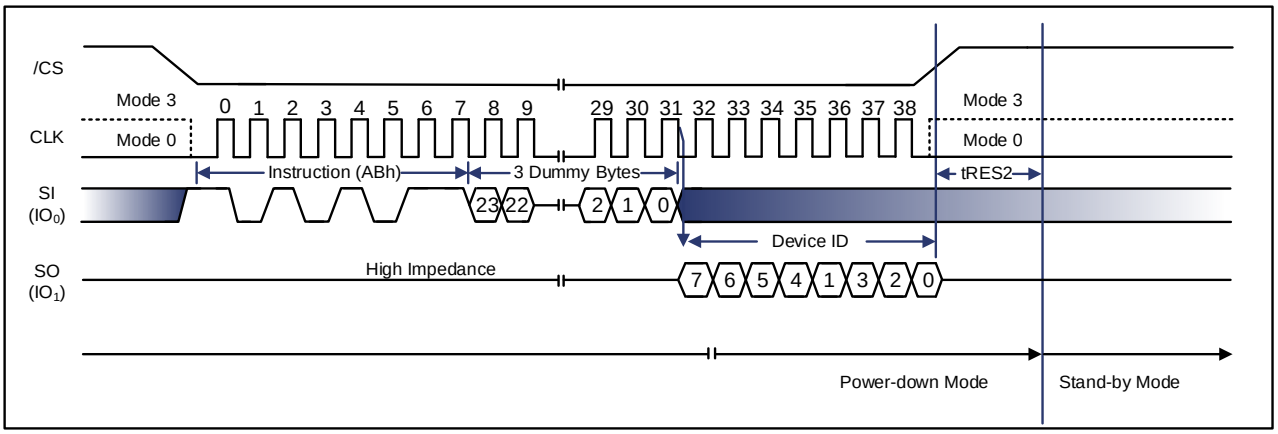


Figure 9-46 Release Power-down / Device ID Instruction (SPI Mode)

9.2.40 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for XMC(20h) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 9-47. The Device ID values for the XM25RU512Dare listed in Manufacturer and Device Identification table. The instruction is completed by driving /CS high.

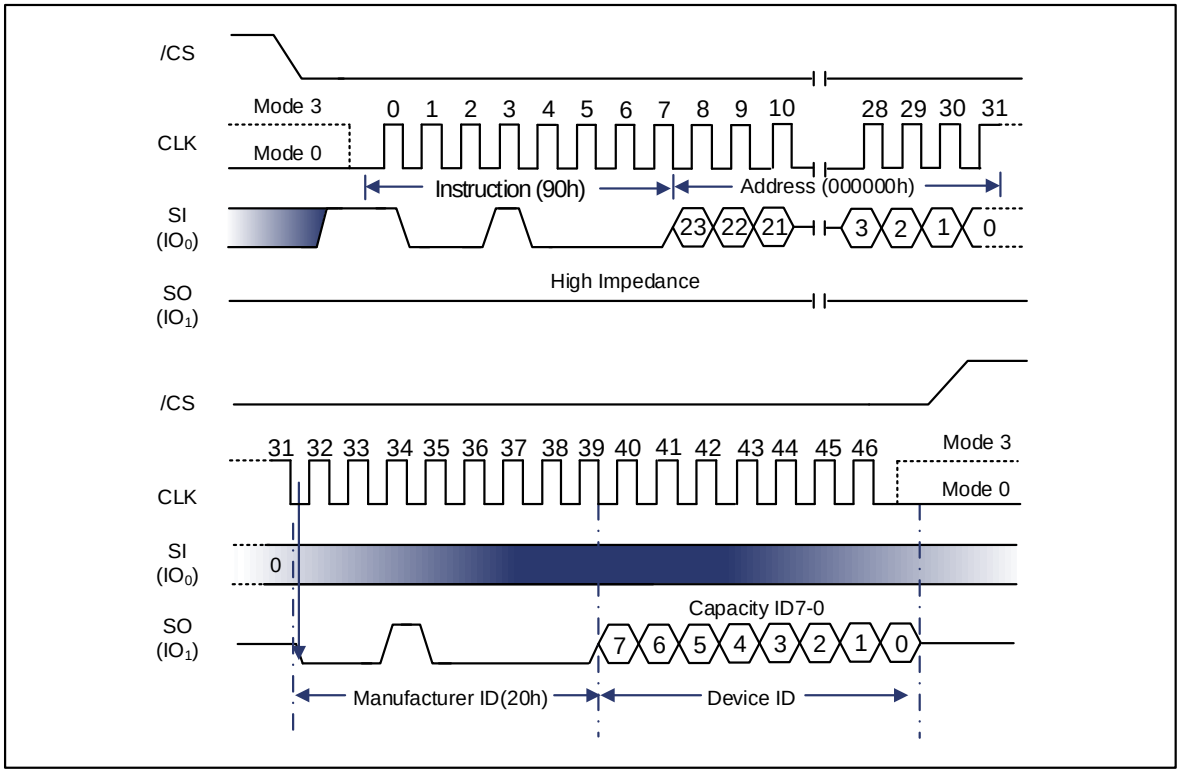


Figure 9-47 Read Manufacturer / Device ID Instruction (SPI Mode)

9.2.41 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “92h” followed by a 24/32-bit address (A23/A31-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for XMC (20h) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 9-48.

The Device ID values for the XM25RU512Dare listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

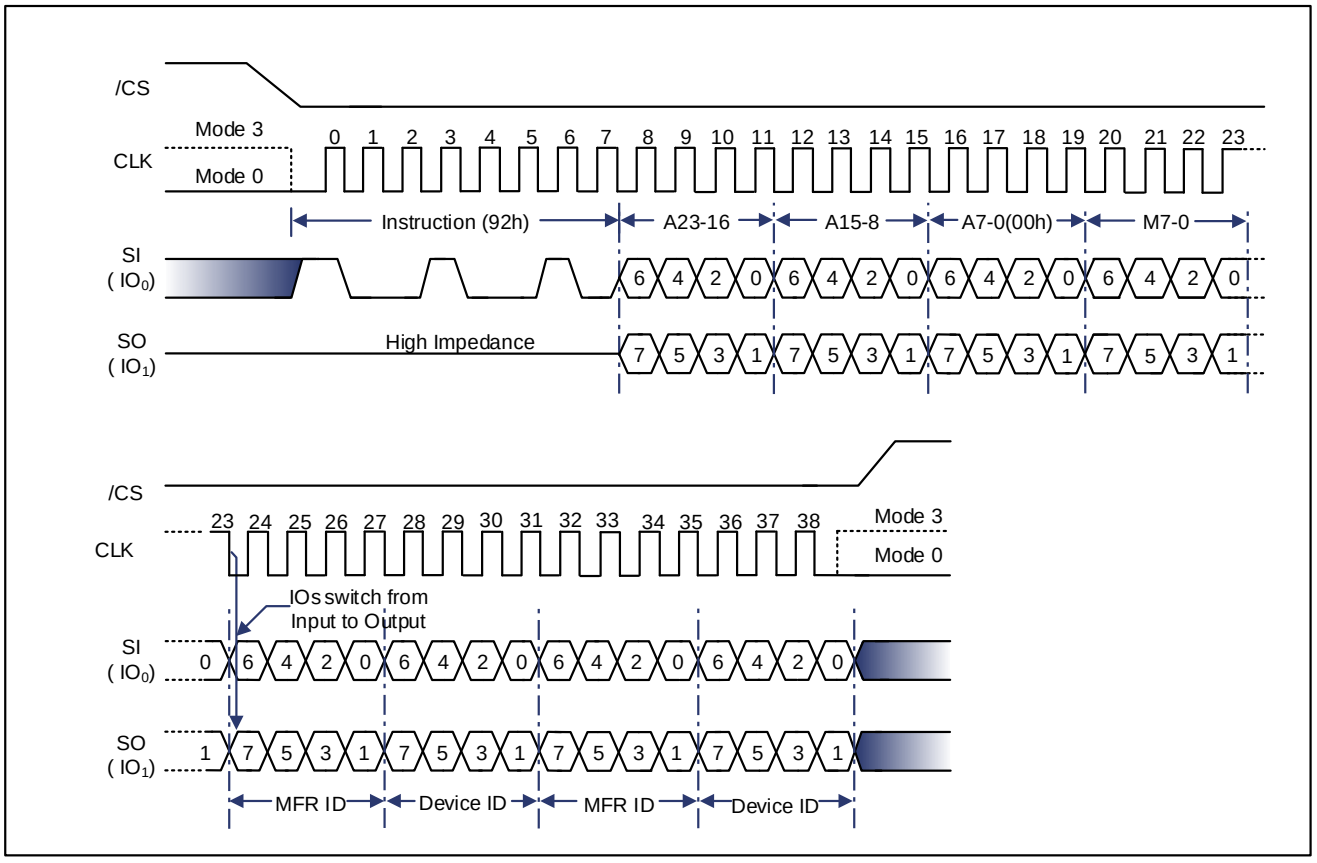


Figure 9-48 Read Manufacturer / Device ID Dual I/O Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

Note:

The Read Command Bypass Mode bits M(7-0) must be set to Fxh to be compatible with Fast Read Dual I/O instruction.

9.2.42 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “94h” followed by a four clock dummy cycles and then a 24/32-bit address (A23/A31-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for XMC (20h) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 9-49. The Device ID values for the XM25RU512Dare listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

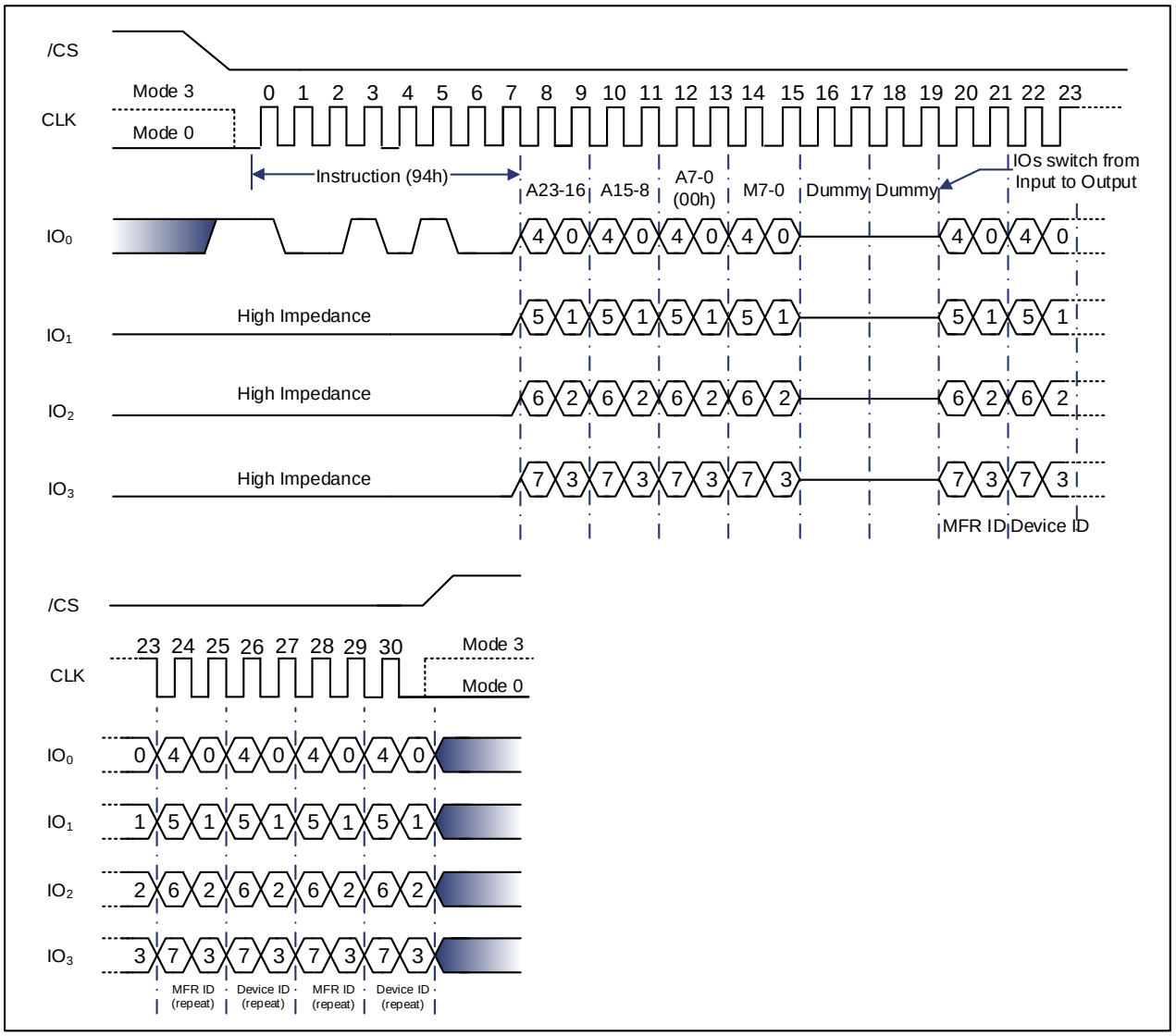


Figure 9-49 Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

Note:

The Read Command Bypass Mode bits M(7-0) must be set to Fxh to be compatible with Fast Read Quad I/O instruction.

9.2.43 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each XM25RU512Ddevice. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of CLK as shown in Figure 9-50.

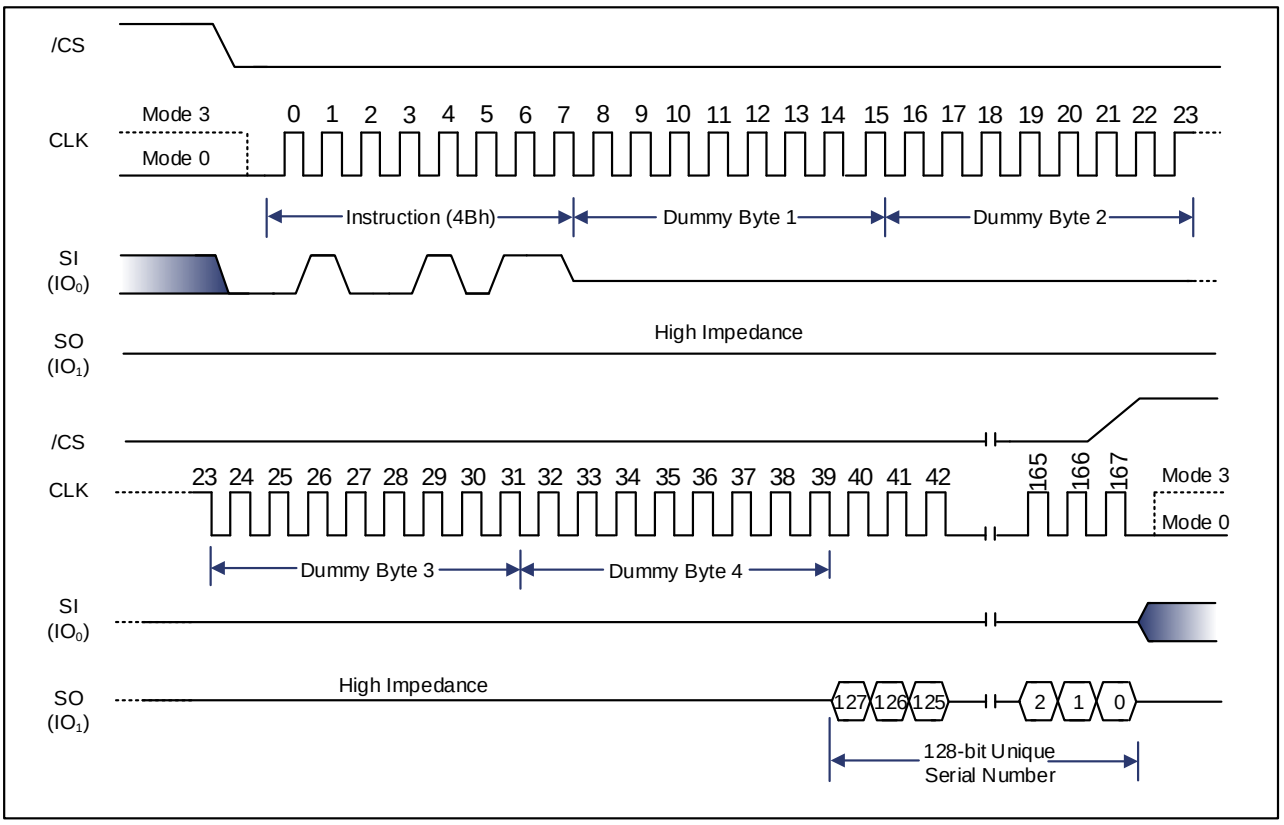


Figure 9-50 Read Unique ID Number Instruction (SPI Mode only)

5 Dummy Bytes are required when the device is operating in 4-Byte Address Mode

9.2.44 Read JEDEC ID (9Fh)

For compatibility reasons, the XM25RU512D provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for XMC (20h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 9-51. For memory type and capacity values refer to Manufacturer and Device Identification table.

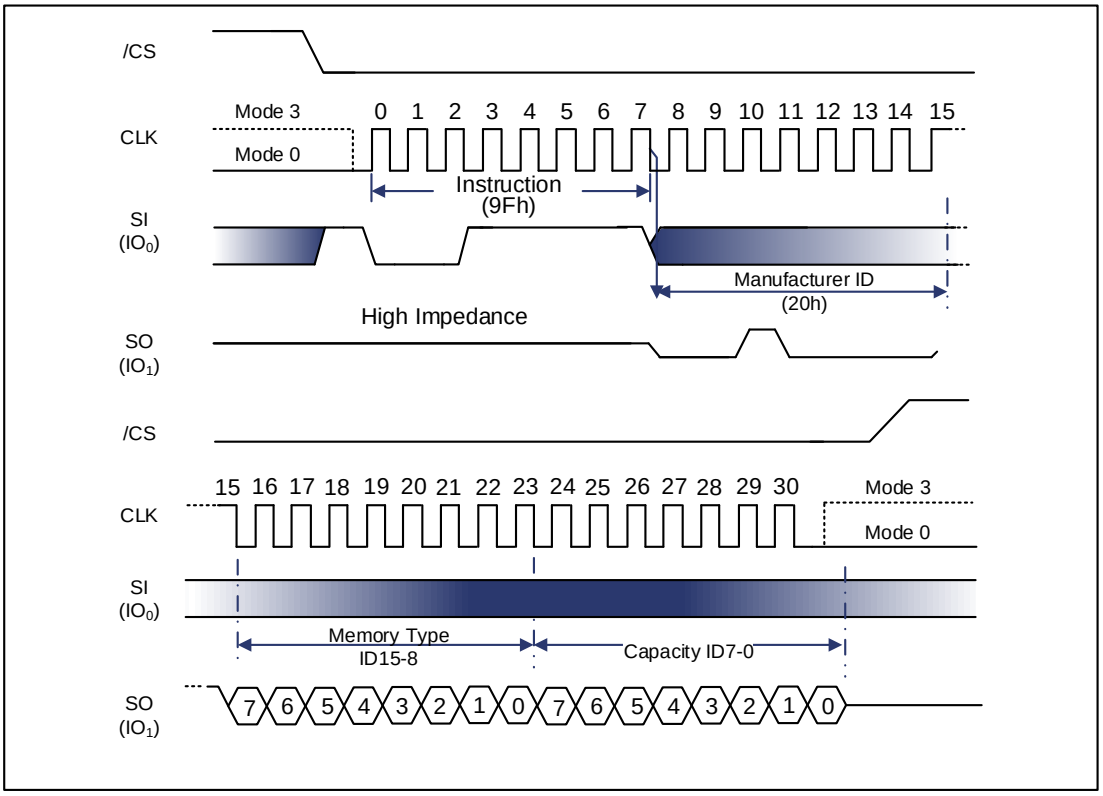


Figure 9-51 Read JEDEC ID Instruction (SPI Mode)

9.2.45 Read SFDP Register (5Ah)

The XM25RU512D features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard JESD216 that is published in 2011.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code “5Ah” followed by a 24-bit address (A23-A0)(1) into the SI pin. Eight “dummy” clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 9-52. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. The last byte address of the register is FFh (the data will always be FFh when read after the last address), For SFDP register values and descriptions, please refer to please refer to the following SFDP Definition Table.

Note: 1. A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

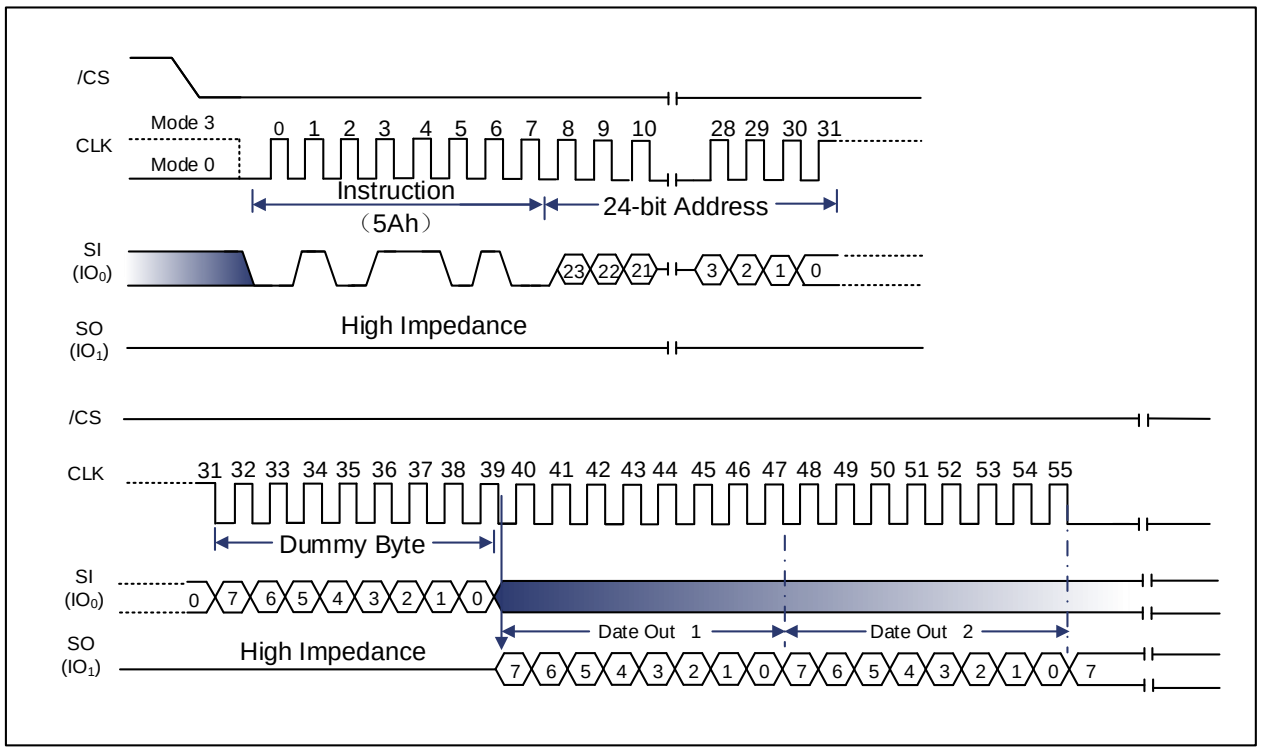


Figure 9-52 Read SFDP Register Instruction Sequence Diagram (Only SPI Mode)

Only 24-Bit Address is required when the device is operating in either 3-Byte or 4-Byte Address Mode

Serial Flash Discoverable Parameters (SFDP) Signature and Parameter Identification Data Value (Advanced Information)

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
SFDP Signature	00h	07 : 00	53h	Fixed: 50444653h
	01h	15 : 08	46h	
	02h	23 : 16	44h	
	03h	31 : 24	50h	
SFDP Minor Revision Number	04h	07 : 00	06h	Star from 0x00
SFDP Major Revision Number	05h	15 : 08	01h	Star from 0x01
Number of Parameter Headers (NPH)	06h	23 : 16	03h	This number is 0-based.Therefore,0 indicates 1 parameter header.
Unused	07h	31 : 24	FFh	Reserved
ID Number(JEDEC)	08h	07 : 00	00h	00h:it indicates a JEDEC specified header.
Parameter Table Minor Revision Number	09h	15 : 08	06h	Star from 0x00
Parameter Table Major Revision Number	0Ah	23 : 16	01h	Star from 0x01
Parameter Table Length (in double word)	0Bh	31 : 24	10h	How many DWORDs in the parameter table
Parameter Table Pointer (PTP)	0Ch	07 : 00	30h	First address of JEDEC Flash Parameter table
	0Dh	15 : 08	00h	
	0Eh	23 : 16	00h	
Unused	0Fh	31 : 24	FFh	
ID number(Manufacturer ID)	10h	07 : 00	20h	It indicates manufacture ID
Parameter Table Minor Revision Number	11h	15 : 08	00h	Start from 00h
Parameter Table Major Revision Number	12h	23 : 16	01h	Start from 01h
Parameter Table Length(in double word)	13h	31 : 24	04h	How many DWORDs in the parameter table
Parameter Table Pointer(PTP)	14h	07 : 00	D0h	First address of VENDOR Flash Parameter table
	15h	15 : 08	00h	
	16h	23 : 16	00h	
Unused	17h	31 : 24	FFh	
ID number (4-byte Address Instruction)	18h	07 : 00	84h	4-byte Address Instruction parameter ID
Parameter Table Minor Revision Number	19h	15 : 08	00h	Start from 00h
Parameter Table Major Revision Number	1Ah	23 : 16	01h	Start from 01h
Parameter Table Length (in double word)	1Bh	31 : 24	02h	How many DWORDs in the Parameter table
Parameter Table Pointer (PTP)	1Ch	07 : 00	C0h	First address of 4-byte Address Instruction table
	1Dh	15 : 08	00h	
	1Eh	23 : 16	00h	
Unused	1Fh	31 : 24	FFh	
ID Number (RPMC Manufacturer ID)	20h	07 : 00	03h	RPMC manufacturer ID
Parameter Table Minor Revision Number	21h	15 : 08	00h	Start from 00h
Parameter Table Major Revision Number	22h	23 : 16	01h	Start from 01h
Parameter Table Length(in double word)	23h	31 : 24	02h	How many DWORDs in the RPMC parameter table
Parameter Table Pointer (PTP)	24h	07 : 00	B0h	First address of RPMC parameter table
	25h	15 : 08	00h	
	26h	23 : 16	00h	
Unused	27h	31 : 24	FFh	

● Parameter ID (0) JEDEC Flash Parameter Tables 1/10

Description	Add(h) (Byte)	DW Add (Bit)	Data	Comment
Block / Sector Erase sizes	30h	01 : 00	01b	00:Reserved, 01:4KB erase, 10:Reserved, 11:not supported 4KB erase
Write Granularity		02	1b	0:1Byte,1:64Byte or larger
Volatile Status Register Block Protect bits		03	0b	0: Block Protect bits in device's status register are solely non-volatile or may be programmed either as volatile using the 50h instruction for write enable or non-volatile using the 06h instruction for write enable. 1: Block Protect bits in device's status register are solely volatile.
Write Enable Instruction Select for Writing to Volatile Status Registers		04	0b	0:use 50h instruction 1:use 06h instruction
Unused		07 : 05	111b	Contains 111b and can never be changed
4KB Erase Instruction	31h	15 : 08	20h	
(1-1-2) Fast Read(1)	32h	16	1b	0 = not supported 1 = supported
Address Bytes Number used in addressing flash array		18 : 17	01b	00:3Byte only, 01:3 or 4Byte 10:4Byte only, 11:Reserved
Double Transfer Rate (DTR) clocking		19	0b	0 = not supported 1 = supported
(1-2-2) Fast Read		20	1b	0 = not supported 1 = supported
(1-4-4) Fast Read		21	1b	0 = not supported 1 = supported
(1-1-4) Fast Read		22	1b	0 = not supported 1 = supported
Unused		23	1b	
Unused	33h	31 : 24	FFh	

● Parameter ID (0) JEDEC Flash Parameter Tables 2/10

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Flash Memory Density	37h : 34h	31 : 00	1FFFFFFFh	For densities 2 gigabits or less, bit-31 is set to 0b. The field 30:0 defines the size in bits. Example: 00FFFFFFh = 16 megabits For densities 4 gigabits and above, bit-31 is set to 1b. The field 30:0 defines 'N' where the density is computed as 2^N bits (N must be >= 32). Example: 80000021h = 2^33 = 8 gigabits

● Parameter ID (0) JEDEC Flash Parameter Tables 3/10

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
(1-4-4)Fast Read number of Wait states(2)	38h	04 : 00	00100b	00000b:Not supported; 00010b: 2; **00100b:4**; 00110b:6; 01000b:8
(1-4-4)Fast Read number of Mode Clocks(3)		07 : 05	010b	Mode clocks: 000b:Not supported; 010: 2 clocks
(1-4-4)Fast Read instruction	39h	15 : 08	EBh	
(1-1-4)Fast Read Number of Wait states	3Ah	20 : 16	01000b	00000b:Not suppoted; 00010b: 2; 00100b:4 00100b:6; **01000b:8**
(1-1-4)Fast Read Number of Mode Clocks		23 : 21	000b	Mode clocks: 000b:Not supported; 010b:2 clocks
(1-1-4)Fast Read Instruction	3Bh	31 : 24	6Bh	

● Parameter ID (0) JEDEC Flash Parameter Tables 4/10

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
(1-1-2)Fast Read Number of Wait states	3Ch	04 : 00	01000b	00000b:Not supported; 00010b: 2; 00100b:4; 00110b:6; **01000b:8**
(1-1-2)Fast Read Number of Mode Clocks		07 : 05	000b	Mode clocks: 000b:Not supported; 010:2 clocks
(1-1-2)Fast Read Instruction	3Dh	15 : 08	3Bh	
(1-2-2)Fast Read Number of Wait states	3Eh	20 : 16	00010b	00000b:Not supported; **00010b: 2**; 00100b:4; 00110b:6; 01000b:8
(1-2-2)Fast Read Number of Mode Clocks		23 : 21	010b	Mode clocks: 000b:Not supported;010:2 clocks
(1-2-2)Fast Read Instruction	3Fh	31 : 24	BBh	

● Parameter ID (0) JEDEC Flash Parameter Tables 5/10

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
(2-2-2)Fast Read	40h	00	0b	0 = not supported 1 = supported
Unused		03 : 01	111b	
(4-4-4)Fast Read		04	0b	0 = not supported 1 = supported
Unused		07 : 05	111b	
Unused	43h : 41h	31 : 08	FFFFFFh	

● **Parameter ID (0) JEDEC Flash Parameter Tables 6/10**

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Unused	45h : 44h	15 : 00	FFFFh	
(2-2-2)Fast Read Number of Wait states	46h	20 : 16	00000b	00000b:Not supported;00100b:4; 00110b:6; 01000b:8
(2-2-2) Fast Read Number of Mode Clocks		23 : 21	000b	Mode Clocks: 000b:Not supported; 010:2 clocks
(2-2-2)Fast Read Instruction	47h	31 : 24	FFh	

● **Parameter ID (0) JEDEC Flash Parameter Tables 7/10**

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Unused	49h : 48h	15 : 00	FFFFh	
(4-4-4)Fast Read Number of Wait states	4Ah	20 : 16	00000b	00000b:Not supported;00100b:4 00110b:6; 01000b:8
(4-4-4) Fast Read Number of Mode Clocks		23 : 21	000b	Mode Clocks: 000b:Not supported; 010:2 clocks
(4-4-4)Fast Read Instruction	4Bh	31 : 24	FFh	

● **Parameter ID (0) JEDEC Flash Parameter Tables 8/10**

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Erase Type 1 Size	4Ch	07 : 00	0Ch	Sector/block size=2N bytes(4) 0Ch:4KB; 0Fh:32KB; 10h:64KB
Erase Type 1 Erase Instruction	4Dh	15 : 08	20h	
Erase Type 2 Size	4Eh	23 : 16	0Fh	Sector/block size=2N bytes 00h:NA; 0Fh:32KB; 10h:64KB
Erase Type 2 Erase Instruction	4Fh	31 : 24	52h	

● **Parameter ID (0) JEDEC Flash Parameter Tables 9/10**

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Erase Type 3 Size	50h	07 : 00	10h	Sector/block size=2N bytes 00h:NA; 0Fh:32KB; 10h:64KB
Erase Type 3 Erase Instruction	51h	15 : 08	D8h	
Erase Type 4 Size	52h	23 : 16	00h	Sector/block size=2N bytes 00h:NA; 0Fh:32KB; 10h:64KB
Erase Type 4 Erase Instruction	53h	31 : 24	FFh	Not support

● **Parameter ID (0) JEDEC Flash Parameter Tables 10/10**

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Multiplier from typical erase time to maximum erase time	54h	03 : 00	0101b	Multiplier value: 0h~Fh (0~15) Max. time = 2 * (Multiplier + 1) * Typical Time
		07 : 04	00001b	
Erase Type 1 Erase Time (Typical)		08		Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units
	55h	10 : 09	01b	Units: 00: 1ms, 01: 16ms 10b: 128ms, 11b: 1s
Erase Type 2 Erase Time (Typical)		15 : 11	00100b	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units
	56h	17 : 16	01b	Units: 00: 1ms, 01: 16ms 10b: 128ms, 11b: 1s
Erase Type 3 Erase Time (Typical)		22 : 18	00111b	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units
		24 : 23	01b	Units: 00: 1 ms, 01: 16 ms 10b: 128ms, 11b: 1s
Erase Type 4 Erase Time (Typical)	57h	29 : 25	00000b	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units
		31 : 30	00b	Units: 00: 1ms, 01: 16ms 10b: 128 ms, 11b: 1 s
Multiplier from typical time to max time for Page or byte program	58h	03 : 00	0011b	Multiplier value: 0h~Fh (0~15) Max. time = 2 * (Multiplier + 1) *Typical Time
Page Program Size		07 : 04	1000b	Page size = 2^N bytes 2^8 = 256 bytes, 8h = 1000b
Page Program Time (Typical)	59h	12 : 08	00011b	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units
		13	1b	Units: 0: 8us, 1: 64us
Byte Program Time, First Byte (Typical)		15 : 14	1110b	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * Units
	5Ah	17 : 16		
		18	0b	Units: 0: 1us, 1: 8us
Byte Program Time, Additional Byte (Typical)		22 : 19	0010b	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * Units
		23	0b	Units: 0: 1us, 1: 8us
Chip Erase Time (Typical)	5Bh	28 : 24	01110b	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units
		30 : 29	10b	Units 00: 16ms, 01: 256ms 10: 4s, 11: 64s
Reserved		31	1b	Reserved
Prohibited Operations During Program Suspend	5Ch	03 : 00	1100b	xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) xxx1b: May not initiate a new erase in the program suspended page size xx0xb: May not initiate a new page program anywhere (program nesting not permitted) xx1xb: May not initiate a new page program in the program suspended page size x0xxb: Refer to vendor datasheet for read restrictions x1xxb: May not initiate a read in the program suspended page size 0xxxb: Additional erase or program restrictions apply 1xxxb: The erase and program restrictions in bits 1:0 are sufficient
Prohibited Operations During Erase Suspend		07 : 04	1100b	xxx0b: May not initiate a new erase anywhere (erase nesting not permitted)

				xxx1b: May not initiate a new erase in the erase suspended erase type size xx0xb: May not initiate a page program anywhere xx1xb: May not initiate a page program in the erase suspended erase type size x0xxb: Refer to vendor datasheet for read restrictions x1xxb: May not initiate a read in the erase suspended erase type size 0xxxb: Additional erase or program restrictions apply 1xxxb: The erase and program restrictions in bits 5:4 are sufficient
Reserved	5Dh	08	1b	Reserved
Program Resume to Suspend Interval (Typical)		12 : 09	0000b	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * 64us
Program Suspend Latency (Max.)		15: 13	10101b	Count value: 00h~1Fh (0~31) Maximum Time = (Count + 1) * Units
	5Eh	17 : 16		
		19 : 18	01b	Units: 00: 128ns, 01: 1us 10: 8us, 11: 64us
Erase Resume to Suspend Interval (Typical)		23 : 20	0111b	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * 64us
Erase Suspend Latency (Max.)	5Fh	28 : 24	10101b	Count value: 00h~1Fh (0~31) Maximum Time = (Count + 1) * Units
		30 : 29	01b	Units: 00: 128ns, 01: 1us 10: 8us, 11: 64us
Suspend / Resume supported		31	0b	0= Support 1= Not supported
Program Resume Instruction	60h	07 : 00	7Ah	Instruction to Resume a Program
Program Suspend Instruction	61h	15 : 08	75h	Instruction to Suspend a Program
Erase Resume Instruction	62h	23 : 16	7Ah	Instruction to Resume Write/Erase
Erase Suspend Instruction	63h	31 : 24	75h	Instruction to Suspend Write/Erase
Reserved	64h	01 : 00	11b	Reserved: 11b
Status Register Polling Device Busy		07 : 02	111101b	**Bit 2**: Read WIP bit [0] by 05h Read instruction **Bit 3:** Read bit 7 of Status Register by 70h Read instruction (0=not supported 1=support) **Bit 07:04**, Reserved: 1111b
Release from Deep Power-down (RDP) Delay (Max.)	65h	12 : 08	10011b	Count value: 00h~1Fh (0~31) Maximum Time = (Count + 1) * Units
		14 : 13	01b	Units: 00: 128ns, 01: 1us 10: 8us, 11: 64us
Release from Deep Power-down (RDP) Instruction	66h	15	10101011b	Instruction to Exit Deep Power Down FFh: Don't need command
		22 : 16		
Enter Deep Power Down Instruction	67h	23	10111001b	Instruction to Enter Deep Power Down
		30 : 24		
Deep Power Down Supported		31	0b	0: Supported 1: Not supported
4-4-4 Mode Disable Sequences	68h	03 : 00	1001b	Methods to exit 4-4-4 mode xxx1b: issue FFh instruction xx1xb: issue F5h instruction x1xxb: device uses a read-modify-write sequence of operations 1xxxb: issue the Soft Reset 66/99 sequence
4-4-4 Mode Enable Sequences	69h	07 : 04	00001b	Methods to enter 4-4-4 mode; x_xxx1b: set QE per QER description above, then issue instruction 38h x_xx1xb: issue instruction 38h x_x1xxb: issue instruction 35h
		08		
0-4-4 Mode Supported		09	1b	Performance Enhance Mode, Continuous Read, Execute in Place 0: Not supported 1: Supported

0-4-4 Mode Exit Method		15 : 10	111101b	xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation. xx_xx1xb: If 3-Byte address active, input Fh on DQ0-DQ3 for 8 clocks. If 4-Byte address active, input Fh on DQ0-DQ3 for 10 clocks. Xx_x1xxb: Reserved xx_1xxxb: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. x1_xxxxb: Mode Bit[7:0]≠Axh 1x_xxxxb: Reserved
0-4-4 Mode Entry Method	6Ah	19 : 16	1101h	xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode x1xxb: Mode Bit[7:0]=Axh 1xxxb: Reserved
Quad Enable (QE) bit Requirements		22 : 20	100b	000b: No QE bit. Detects 1-1-4/1-4- 4 reads based on instruction 100b: QE is bit 1 of status register 2. 010b: QE is bit 6 of Status Register. Where 1=Quad Enable or 0=not Quad Enable 111b: Not Supported
HOLD and RESET Disable by bit 4 of Ext. Configuration Register		23	0b	0: Not supported
Reserved	6Bh	31 : 24	FFh	Reserved
Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1	6Ch	06 : 00	1101001b	xxx_xxx1b: Non-Volatile Status Register 1, powers-up to last written value, use instruction 06h to enable write xxx_1xxxb: Non-Volatile/Volatile status register 1 powers-up to last written value in the nonvolatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register. xx1_xxxxb: Status Register 1 contains a mix of volatile and non-volatile bits. The 06h instruction is used to enable writing of the register. x1x_xxxxb: Reserved 1xx_xxxxb: Reserved
Reserved		07	1b	Reserved
Soft Reset and Rescue Sequence Support	6Dh	13 : 08	010000b	Return the device to its default power-on state Exit 4-Byte Addressing issue reset enable instruction 66h, then issue reset instruction 99h.
Exit 4-Byte Addressing		15 : 14	01b	xx_xxxx_xxx1b: issue instruction E9h to exit 4-Byte address mode (write enable instruction 06h is not required) xx_xxxx_x1xxb: 8-bit volatile extended address register used to define A[31:A24] bits. Read with instruction C8h. Write instruction is C5h, data length is 1 byte. Return to lowest memory segment by setting A[31:24] to 00h and use 3-Byte addressing. xx_xx1x_xxxxb: Hardware reset xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD) xx_1xxx_xxxxb: Power cycle x1_xxxx_xxxxb: Reserved 1x_xxxx_xxxxb: Reserved
	6Eh	23 : 16	11111001b	
Enter 4-Byte Addressing	6Fh	31 : 24	10000101b	xxxx_xxx1b: issue instruction B7h (preceding write enable not required) xxxx_x1xxb: 8-bit volatile extended address register used to define A[31:24] bits. Read with instruction C8h. Write instruction is C5h with 1 byte of data. Select the active 128 Mbit memory segment by setting the appropriate A[31:24] bits and use 3-Byte addressing. xx1x_xxxxb: Supports dedicated 4-Byte address instruction set. Consult vendor data sheet for the instruction set definition. 1xxx_xxxxb: Reserved

● Parameter Table(1) : 4-Byte Instruction Tables

Description	Add(h) (Byte)	DW Add (Bit)	Data	Comment
Support for (1-1-1) READ Command, Instruction=13h	C0h	00	1b	0=not supported 1=supported
Support for (1-1-1) FAST_READ Command, Instruction=0Ch		01	1b	0=not supported 1=supported
Support for (1-1-2) FAST_READ Command, Instruction=3Ch		02	1b	0=not supported 1=supported
Support for (1-2-2) FAST_READ Command, Instruction=BCh		03	1b	0=not supported 1=supported
Support for (1-1-4) FAST_READ Command, Instruction=6Ch		04	1b	0=not supported 1=supported
Support for (1-4-4) FAST_READ Command, Instruction=Ech		05	1b	0=not supported 1=supported
Support for (1-1-1) Page Program Command, Instruction=12h		06	1b	0=not supported 1=supported
Support for (1-1-4) Page Program Command, Instruction=34h		07	1b	0=not supported 1=supported
Support for (1-4-4) Page Program Command, Instruction=3Eh	C1h	08	0b	0=not supported 1=supported
Support for Erase Command – Type 1 size, Instruction lookup in next Dword		09	1b	0=not supported 1=supported
Support for Erase Command – Type 2 size, Instruction lookup in next Dword		10	1b	0=not supported 1=supported
Support for Erase Command – Type 3 size, Instruction lookup in next Dword		11	1b	0=not supported 1=supported
Support for Erase Command – Type 4 size, Instruction lookup in next Dword		12	0b	0=not supported 1=supported
Support for (1-1-1) DTR_Read Command, Instruction=0Eh		13	0b	0=not supported 1=supported
Support for (1-2-2) DTR_Read Command, Instruction=Beh		14	0b	0=not supported 1=supported
Support for (1-4-4) DTR_Read Command, Instruction=Eeh		15	0b	0=not supported 1=supported
Support for volatile individual sector lock Read command, Instruction=E0h	C2h	16	0b	0=not supported 1=supported
Support for volatile individual sector lock Write command, Instruction=E1h		17	0b	0=not supported 1=supported
Support for non-volatile individual sector lock read command, Instruction=E2h		18	0b	0=not supported 1=supported
Support for non-volatile individual sector lock write command, Instruction=E3h		19	0b	0=not supported 1=supported
Reserved		23 : 20	1111b	Reserved
Reserved	C3h	31 : 24	FFh	Reserved
Instruction for Erase Type 1	C4h	07 : 00	21h	FFh=not supported
Instruction for Erase Type 2	C5h	15 : 08	5Ch	FFh=not supported
Instruction for Erase Type 3	C6h	23 : 16	DCh	FFh=not supported
Instruction for Erase Type 4	C7h	31 : 24	FFh	FFh=not supported

● Parameter Table(2) : XMC Flash Parameter Tables

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
VCC supply maximum voltage	D1h:D0h	07:00	00h	2000h=2.000V 2700h=2.700V 3600h=3.600V
		15:08	20h	
VCC supply minimum voltage	D3h:D2h	23:16	50h	1650h=1.65V; 1750h=1.75V 2250h=2.25V 2300h=2.3V 2350h=2.35V 2650h=2.65V 2700h=2.7V
		31:24	16h	
H/W /Reset pin	D5h:D4h	0	F99Fh	0 = not supported 1 = supported
H/W /Hold pin		1		0 = not supported 1 = supported
Deep Power Down Mode		2		0 = not supported 1 = supported
S/W Reset		3		0 = not supported 1 = supported
S/W Reset Instruction		11:04		Reset Enable(66h)should be issued before Reset instruction
Program suspend/resume		12		0 = not supported 1 = supported
Erase suspend/resume		13		0 = not supported 1 = supported
Unused		14		
Wrap-Around Read mode		15		0 = not supported 1 = supported
Wrap-Around Read mode instruction	D6h	23:16	77h	
Wrap-Around Read data length	D7h	31:24	64h	08h:support 8B wrap-around read 16h:8B&16B 32h:8B&16B&32B 64h:8B&16B&32B&64B
Individual block lock	DBh:D8h	0	E800h	0 = not supported 1 = supported
Individual block lock bit(Volatile/Nonvolatile)		1		0:Volatile 1:Nonvolatile
Individual block lock Instruction		09:02		0 = not supported 1 = supported
Individual block lock Volatile protect bit default protect status		10		0:Protect 1:Unprotect
Secured OTP		11		0 = not supported 1 = supported
Read Lock		12		0 = not supported 1 = supported
Permanent Lock		13		0 = not supported 1 = supported
Unused		15:14		
Unused		31:16	FFFFh	
Unused	DFh:DCh	31:00	FFFFFFFFh	

● **Parameter Table (3): RPMC Parameter Tables**

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Flash_Hardening	B3h: B0h	00	0b	0= supported 1= not upported
MC_Size		01	0b	0=Monotonic counter size is 32bit 1=Reserved
Busy_Polling_Method		02	0b	0=Poll for OP1 busy using OP2 Extended Status[0] 1=Poll for OP1 busy using Status
Reserved		03	1b	Must be 1
Num_counter-1		07:04	3h	Number of supported counters-1
OP1 Opcode		15:08	9Bh	Suggested value 9Bh
OP2 Opcode		23:16	96h	Suggested value 96h
Update_Rate		27:24	0h	Rate of Update=5*(2**Update_Rate) seconds
Reserved		31:28	fh	Must be 0FH
Read Counter Polling Delay	B7h:B4h	04:00	00001b	Polling delay_read counter
		06:05	10b	Units(00=1us, 01=16us, 10=128us, 11=1ms)
		07	1b	Reserved
Write Counter Polling Short Delay		12:08	00001b	Polling_short_delay_write_counter
		14:13	10b	Units(00=1us, 01=16us, 10=128us, 11=1ms)
		15	1b	Reserved
Write Counter Polling Long Delay		20:16	00011b	Polling_long_delay_write_counter
		22:21	10b	Units(00=1ms, 01=16ms, 10=128ms, 11=1s)
		23	1b	Reserved
Reserved		31:24	FFh	Must be FFH

Note 1:

1. (x-y-z) means I/O mode nomenclature used to indicate the number of active pins used for the instruction (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4);

2: Wait States is required dummy clock cycles after the address bits or optional mode clocks;

3: Mode clocks is optional control bits that follow the address bits. These bits are driven by the system controller if they are specified. (eg,read performance enhance toggling bits);

4: 4KB=2^0Ch,32KB=2^0Fh,64KB=2^10h;;

5: All unused and undefined area data is blank FFh.

9.2.46 Erase Security Registers (44h)

The XM25RU512Doffers three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “44h” followed by a 24/32-bit address (A23/A31-A0) to erase one of the three security registers.

ADDRESS	A23/A31-16	A15-12	A11-8	A7-0
Security Register #1	00h	0001b	0b	Do not Care
Security Register #2	00h	0010b	0b	Do not Care
Security Register #3	00h	0011b	0b	Do not Care

The Erase Security Register instruction sequence is shown Figure 9-53. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of tSE (See AC Characteristics). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB[3:1]) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored (Refer to section 9.1.8 for detail descriptions).

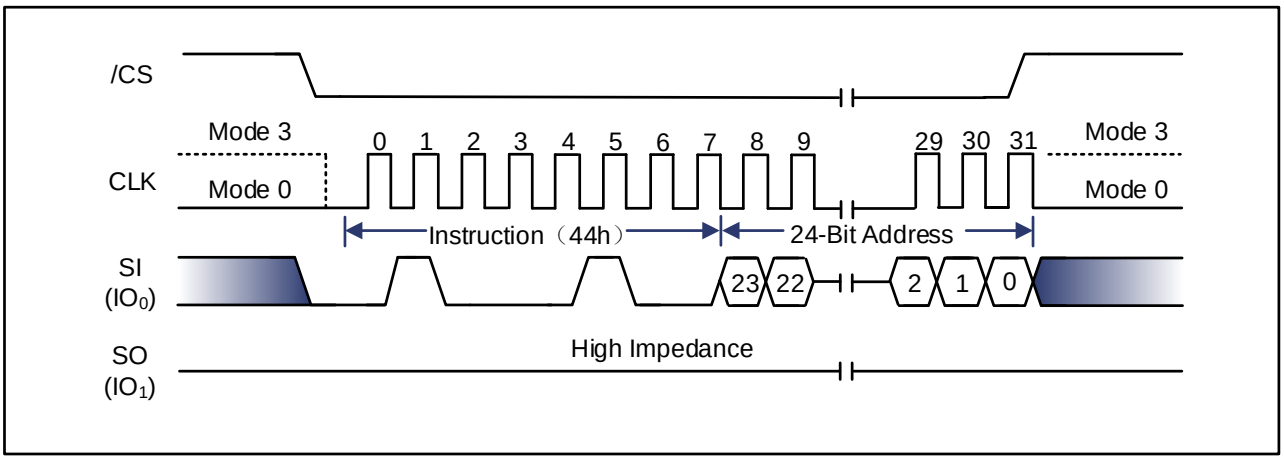


Figure 9-53 Erase Security Registers Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.2.47 Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows from one byte to 256 bytes of security register data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “42h” followed by a 24/32-bit address (A23/A31-A0) and at least one data byte, into the SI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23/A31-16	A15-12	A11-8	A7-0
Security Register #1	00h	0001b	0b	Byte Address
Security Register #2	00h	0010b	0b	Byte Address
Security Register #3	00h	0011b	0b	Byte Address

The Program Security Register instruction sequence is shown in Figure 9-54. The Security Register Lock Bits (LB[3:1]) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored (See 7.1.8 for detail descriptions).

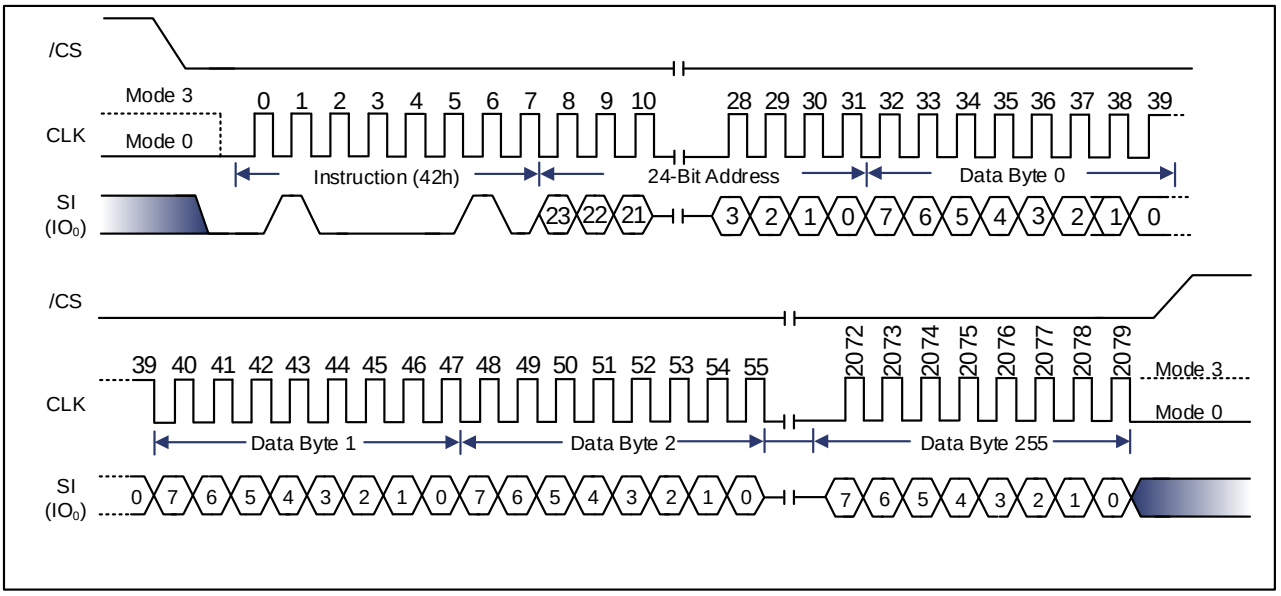


Figure 9-54 Program Security Registers Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.2.48 Read Security Registers (48h)

The Read Security Register instruction is similar to the Fast Read instruction and allows one or more data bytes to be sequentially read from one of the three security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “48h” followed by a 24/32-bit address (A23/A31-A0) and eight “dummy” clocks into the SI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in Figure 9-55. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates from D.C. to a maximum of FR (see AC Electrical Characteristics).

ADDRESS	A23/A31-16	A15-12	A11-8	A7-0
Security Register #1	00h	0001b	0b	Byte Address
Security Register #2	00h	0010b	0b	Byte Address
Security Register #3	00h	0011b	0b	Byte Address

Note: If the 24-bit address (A23-A0) out of the table, the data of the addressed memory location will always be FFh.

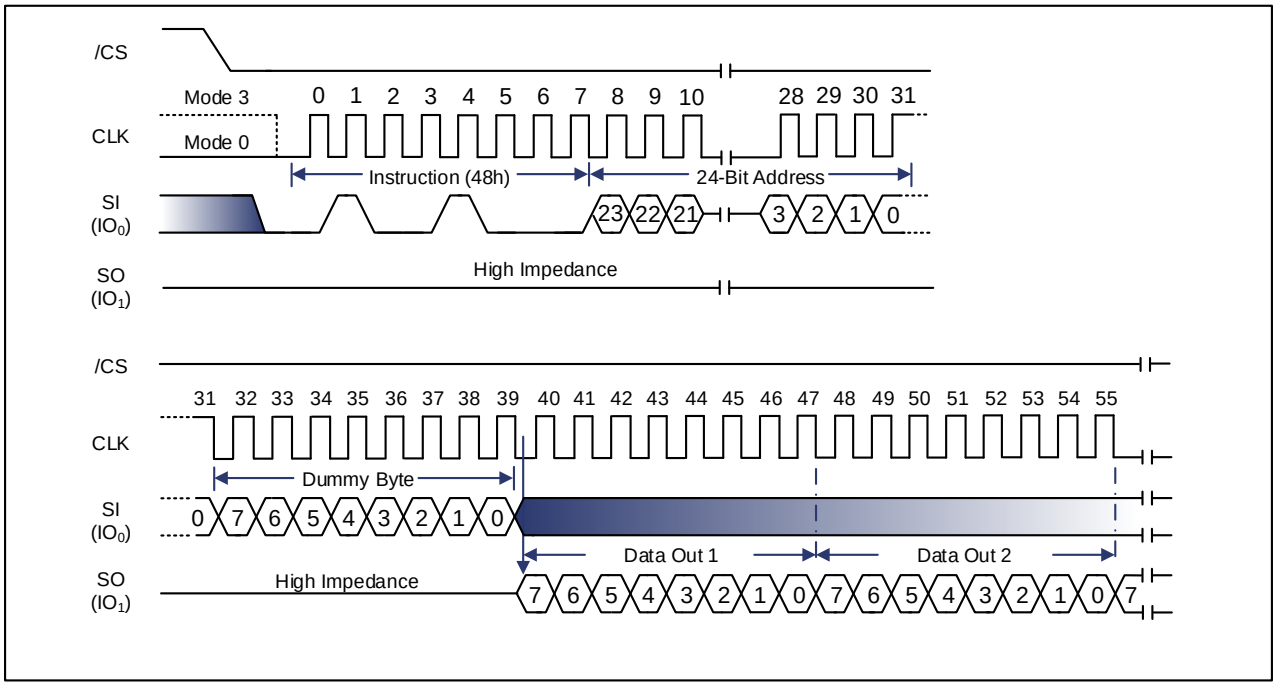


Figure 9-55 Read Security Registers Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode

9.2.49 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the XM25RU512Dprovide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0) and Wrap Bit setting (W6-W4).

“Enable Reset (66h)” and “Reset (99h)” instructions can be issued in either SPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than “Reset (99h)” after the “Enable Reset (66h)” command will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

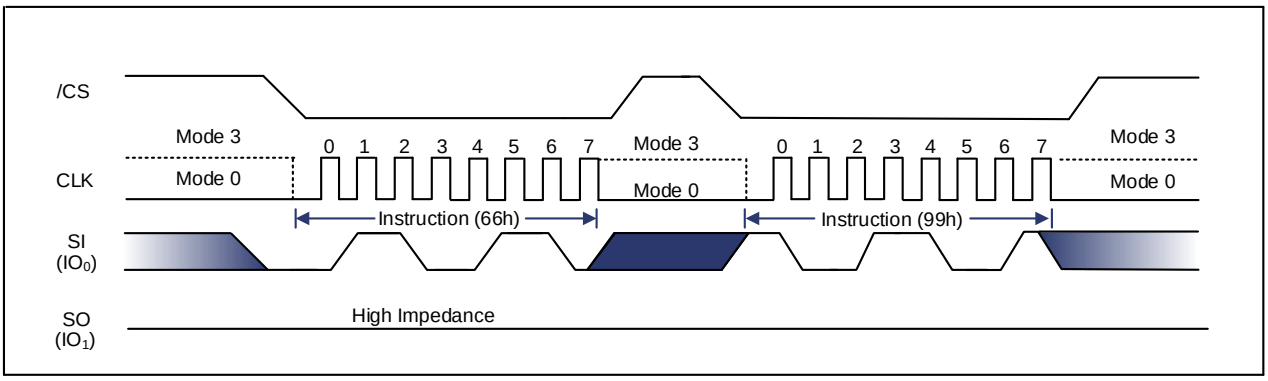


Figure 9-56 Enable Reset and Reset Instruction Sequence (SPI Mode)

9.2.50 Ultra-Deep Power-Down (79H)

The Ultra-Deep Power-Down mode allows the device to consume far less power compared to the standby and Deep Power-Down modes by shutting down additional internal circuitry.

When the device is in the Ultra-Deep Power-Down mode, all commands including the Status Register Read and Resume from Deep Power-Down commands will be ignored. Since all commands will be ignored, the mode can be used as an extra protection mechanism against program and erase operations.

Entering the Ultra-Deep Power-Down mode is accomplished by simply driving /CS low in Deep Power-Down mode, shifting the instruction code “79h” into the Data Input (SI) pin on the rising edge of CLK, and then driving /CS high. Any additional data clocked into the device after the instruction will be ignored. When the /CS pin is high, the device will enter the Ultra-Deep Power-Down mode within the maximum time of tEUDPD(See AC Characteristics).

The complete instruction code must be clocked in before the /CS pin is driving high, and the /CS pin must be driving high on an even byte boundary (multiples of eight bits); otherwise, the device will abort the operation and return to the standby mode once the /CS pin is driving high. In addition, the device will default to the standby mode after a power cycle.

The Ultra-Deep Power-Down command will be ignored if an internally self-timed operation such as a program or erase cycle is in progress. The Ultra-Deep Power-Down command must be reissued after the internally self-timed operation has been completed in order for the device to enter the Ultra-Deep Power-Down mode.

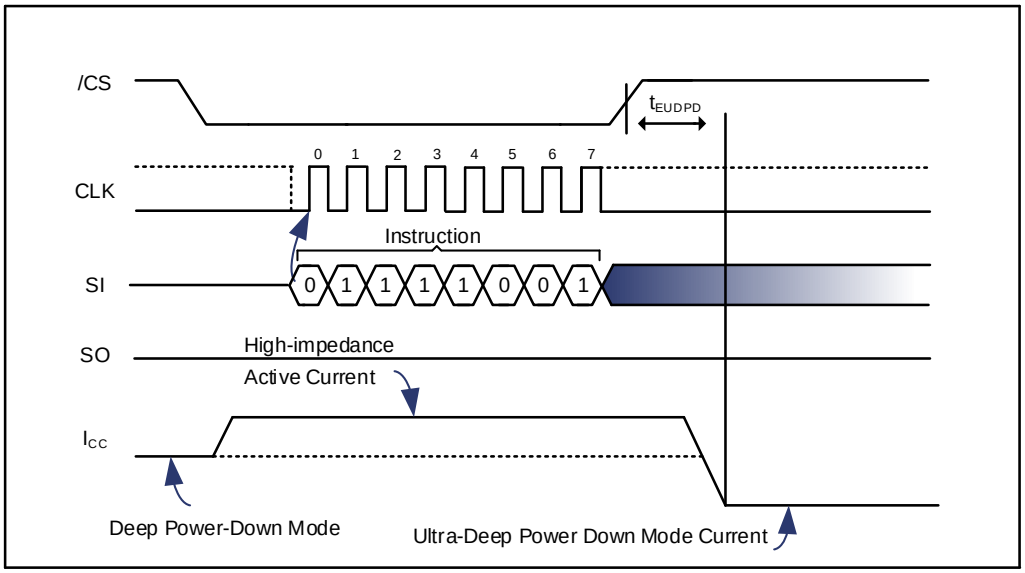


Figure 9-57 Ultra-Deep Power-Down

9.2.51 Exit Ultra-Deep Power-Down

To exit from the Ultra-Deep Power-Down mode, the /CS pin must simply be driving low, waiting the minimum necessary tCSLU (See AC Characteristics) time, and then driving /CS high. To facilitate simple software development, a dummy byte can also be entered while the /CS pin is being pulsed just as in a normal operation like the Program Suspend operation; the dummy byte is simply ignored by the device in this case. After the /CS pin has been driving high, the device will exit from the Ultra-Deep Power-Down mode and return to the standby mode within a maximum time of tXUDPD (See AC Characteristics). If the /CS pin is driving low again before the tXUDPD (See AC Characteristics) time has elapsed in an attempt to start a new operation, then that operation will be ignored and nothing will be performed. The system must wait for the device to return to the standby mode before normal command operations such as Continuous Array Read can be resumed.

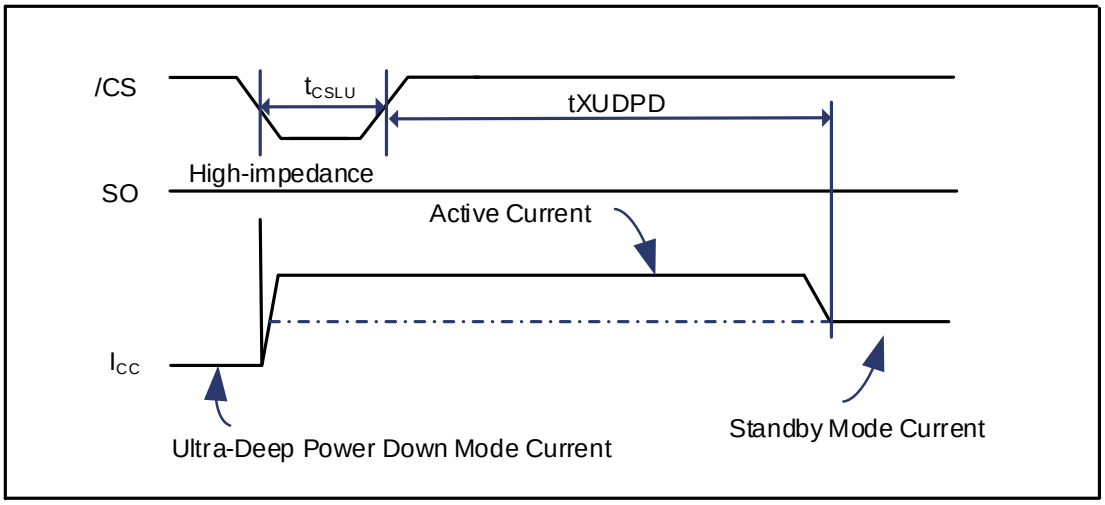


Figure 9-58 Exit Ultra-Deep Power-Down

9.2.52 Write Root Key Register (9Bh + 00h)

This command is used by the SPI Flash Controller to initialize the Root Key Register corresponding to the received Counter Address with the received Root Key. It is expected to be used in an OEM manufacturing environment when the SPI Flash Controller and SPI Flash are powered together for the first time.

After the command is issued on the interface the SPI Flash device must ensure that the received transaction is error free. This includes checking following conditions:

- Payload size is correct. (including OP1 is 64 bytes)
- Counter Address falls within the range of supported counters.
- The Root Key Register corresponding to the requested Counter Address was previously uninitialized. [Root_Key_Reg_Init_State[Counter_Address] = 0xFFh]
- Truncated signature field is the same as least significant 224 bits of HMAC-SHA-256 based signature computed based on received input parameters.

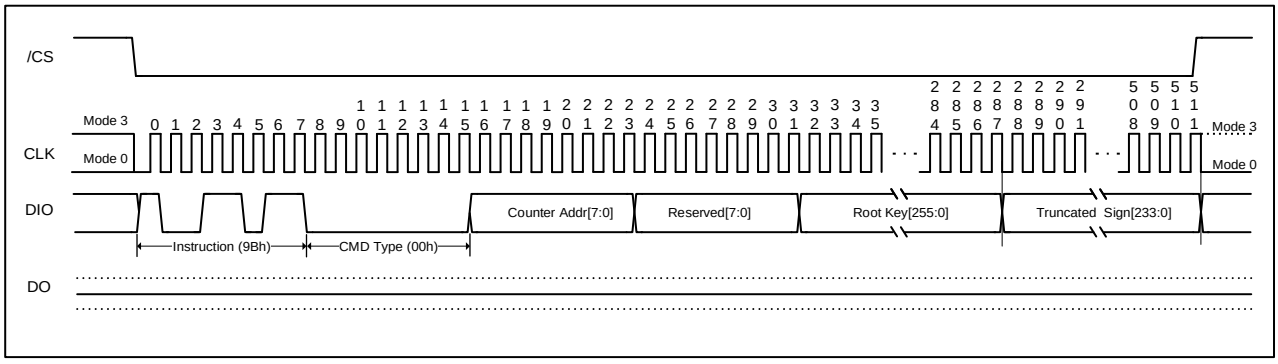
If the received transaction is error free SPI Flash device successfully executes the command and posts “successful completion” in the RPMC Status Register. This command must be executed to ensure that power cycling in the middle of command execution is properly handled. This requires that the internal state tracking the root key register initialization is written as the last operation of the command execution.

(Root_Key_Reg_Init_State[Counter_Address] = 0].

Root Key Register Write with root key is = 256’hFF…FF is used as a temporary key. When this request is received error-free Root_Key_Reg_Init_State[Counter_Address] is not affected. Instead only the corresponding Monotonic counters is initialized to 0 if previously uninitialized. This state is tracked as separate state using MC_Init_State[Counter_Address]. This state is used to leave the Monotonic counters at the current value when an error free Root Key Register Write operation is received. (Both 256’hFF..FF and non 256’hFF..FF).

Once this command is successfully executed with a non 256’hFF..FF Root Key, the device will not accept the “Write Root Key Register” command any more, and the Root Key value cannot be read out by any instructions.

Figure 9-59 Write Root Key Register Instruction



9.2.53 Update HMAC Key (9Bh + 01h)

This command is used by the SPI Flash Controller to update the HMAC-Key register corresponding to the received Counter Address with a new HMAC key calculated based on received input. This command must be issued once only on every power cycle event on the interface. This allows the HMAC key storage to be implemented using volatile memory. Status register busy indication is expected to indicate busy for double the amount of Read_Counter_Polling_Delay specified in SFDP table since this command performs two distinct HMAC-SHA-256 computations (RPMC SFDP table please refer to the RMPC application note).

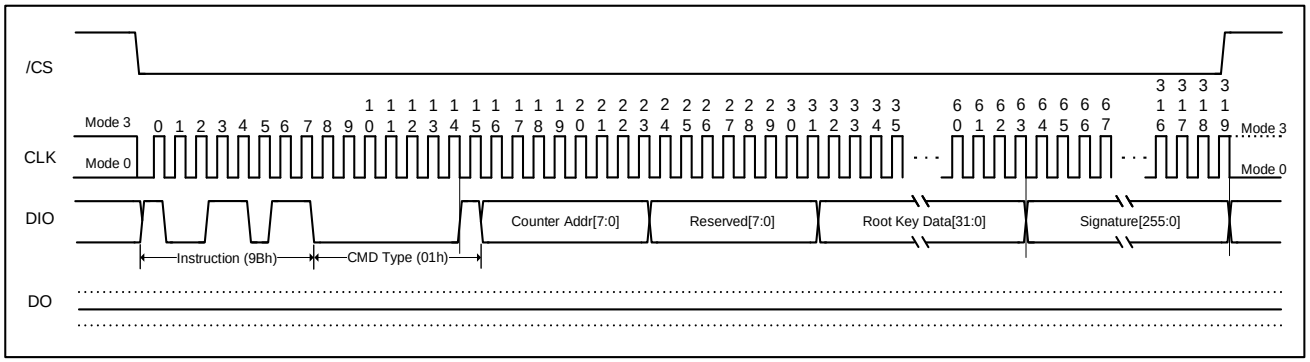
After the command is issued on the interface the SPI Flash device must ensure that the received transaction is error free. This includes checking following conditions:

- Payload size is correct. (including OP1 = 40 bytes)
- Counter Address falls within the range of supported counters.
- The Monotonic counters corresponding to the requested Counter Address was previously initialized.
- Signature matches the HMAC-SHA-256 based signature computed based on received input parameters. This command performs two HMAC-SHA-256 operations.

If the received transaction is error free, the SPI Flash device successfully executes the command and posts “successful completion” in the RPMC Status Register.

If the received transaction has errors, the SPI Flash device does not execute the transaction and posts the corresponding error in the RPMC Status Register.

Figure 9-60 Update HMAC Key Register Instruction



9.2.54 Increment Monotonic counters (9Bh + 02h)

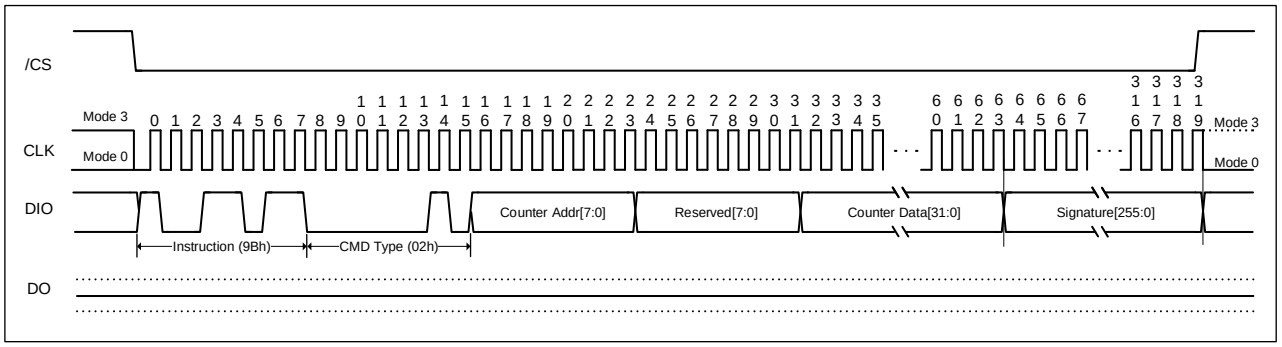
This command is used by the SPI Flash Controller to increment the Monotonic counters by 1 inside the SPI Flash Device.

After the command is issued on the interface the SPI Flash device must ensure that the received transaction is error free. This includes checking following conditions:

- Payload size is correct. (including OP1 = 40 bytes)
- Counter Address falls within the range of supported counters.
- The Monotonic counters corresponding to the requested Counter Address was previously initialized.
- The HMAC Key Register corresponding to the requested Counter Address was previously initialized.
- The requested Signature matches the HMAC-SHA-256 based signature computed based on received input parameters.
- The received Counter_Addressmatches the current value of the counter read from the SPI Flash.

If the received transaction is error free, the SPI Flash device successfully executes the command and posts “successful completion” in the RPMC Status Register. The increment counter implementation should make sure that the counter increment operation is performed in a power glitch aware manner.

Figure 9-61 Increment Monotonic counters Instruction



9.2.55 Request Monotonic counters (9Bh + 03h)

This command is used by the SPI Flash Controller to request the Monotonic counters value inside the SPI Flash Device.

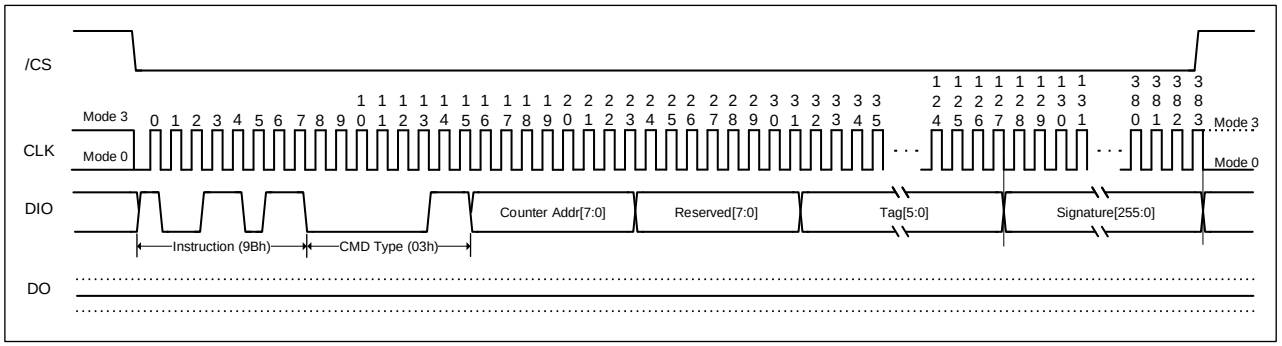
After the command is issued on the interface the SPI Flash device must ensure that the received transaction is error free. This includes checking following conditions:

- Payload size is correct. (including OP1 = 48 bytes)
- Counter Address falls within the range of supported counters.
- The Monotonic counters corresponding to the requested Counter Address was previously initialized.
- The HMAC Key Register corresponding to the requested Counter Address was previously initialized.
- The requested Signature matches the HMAC-SHA-256 based signature computed based on received input parameters.

If the received transaction is error free, the SPI Flash device successfully executes the command and posts “successful completion” in the RPMC Status Register. In response to this command, the SPI flash reads the Monotonic counters addressed by counter address. It calculates HMAC-SHA-256 signatures the second time, based on following parameters.

- HMAC Message[127:0] = Tag [95:0], Counter_Data_Read[31:0]
- HMAC Key[255:0] = HMAC_Key_Register[Counter_Address][255:0]

Figure 9-62 Request Monotonic counters Instruction



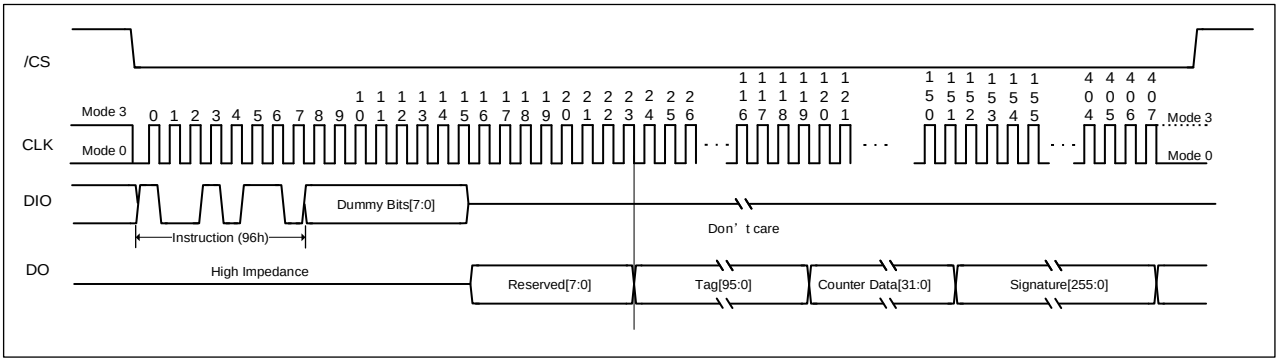
9.2.56 Reserved RPMC Commands (9Bh + 04h~FFh)

If the SPI Flash Controller issues any of the reserved command-types, the SPI Flash Device must return Error status in the RPMC Status Register. It asserts bit 2 to indicate that a reserved command-type was issued.

9.2.57 Read RPMC Status / Data (96h)

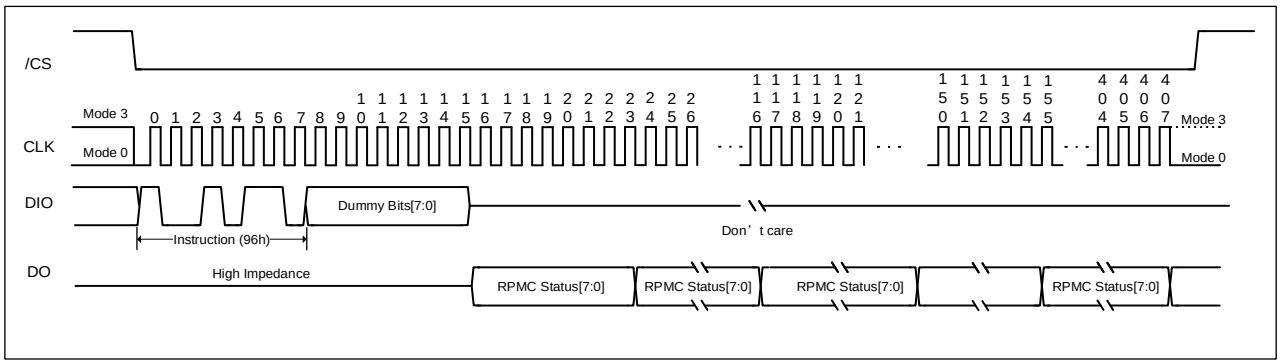
This command is used by the SPI Flash Controller to read the RPMC status from any previously issued OP1 command. In addition, if previous OP1 command is Request Monotonic counters and if SPI Flash returns successful completion (BUSY=0) in the RPMC Status Register, then it must also return valid values in the Tag, Counter_Address and Signature field. If there're other error flags, the values returned in Tag, Counter and Signature field are invalid. The controller may abort the read prematurely prior to completely reading the entire payload. This may occur when the controller wants to simply read the RPMC status or when it observes an error being returned in the RPMC status field. The controller may also continue reading past the defined payload size of 49 bytes. Since this is an error condition, the SPI Flash may return any data past the defined payload size. The controller must ignore the data.

Figure 9-63 Read RPMC Data Instruction (BUSY=0)



When BUSY=1, from Byte-3 and beyond, the device will output the RPMC Status[7:0] value continuously until /CS terminates the instruction. The device will not output Tag, CounterData & Signature fields when BUSY=1. Once BUSY becomes 0, another OP2 command must be issued to read out the correct Tag, CounterData & Signature fields.

Figure 9-64 Read RPMC Data Instruction (BUSY=1)



10 ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Ratings (1)(2)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to 4.6V	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD(3)		See Note (3)	°C
Electrostatic Discharge Voltage	VESD(2)	Human Body Model	–2000 to +2000	V

Notes:

1 This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

2 JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

3. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU

10.2 Operating Ranges

PARAMETER	SYMB OL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC (1)	fc = 133MHz, fR = 80MHz	1.65	2.0	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C
		Industrial Plus	–40	+105	°C

Note:

VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage

10.3 Power-Up Power-Down Timing and Requirements (1)

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min.) to device operation	2		ms
VWI	Write Inhibit Voltage	1.0	1.4	V
tPUW	Time Delay Before Write Instruction	2.5		ms
tPWD	The minimum duration for ensuring initialization will occur	100		µs
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		1	V

Note:These parameters are characterized only.

Figure 10-1 Power-up Timing and Voltage Levels

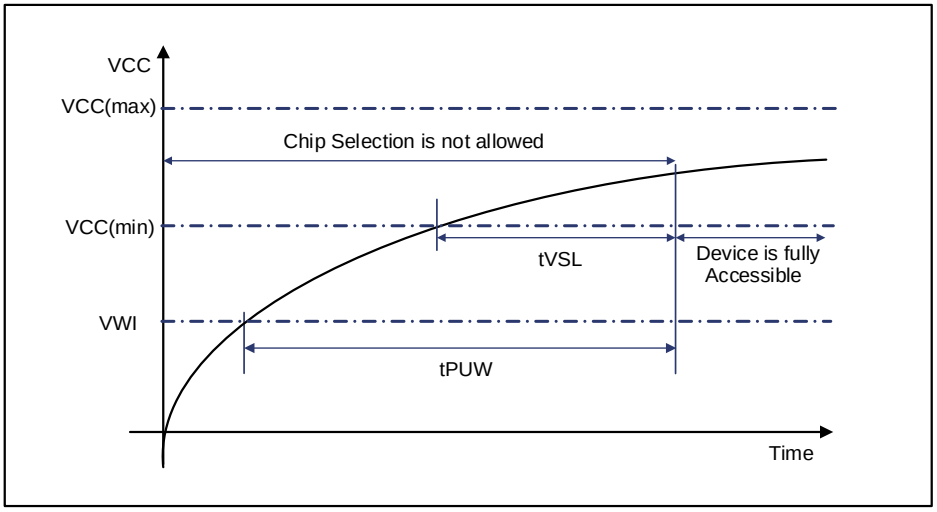


Figure 10-2 Power-up, Power-Down Requirement

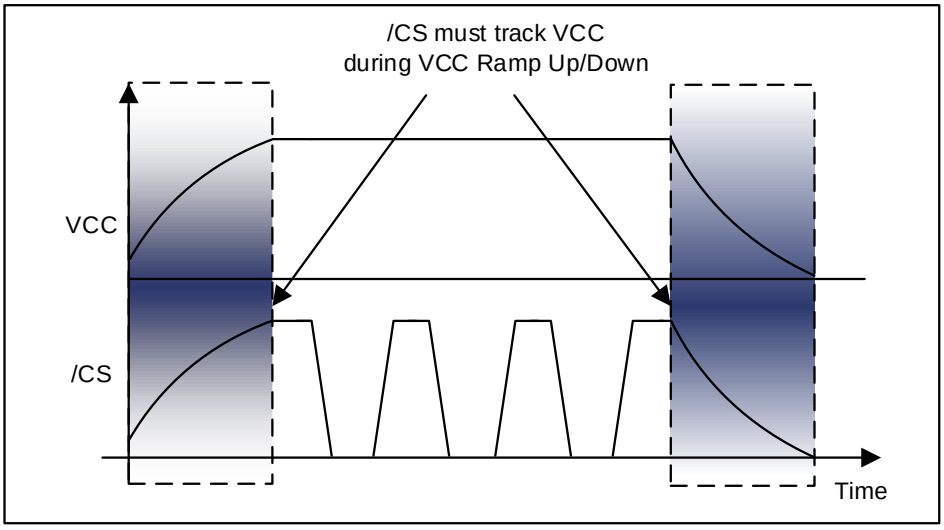
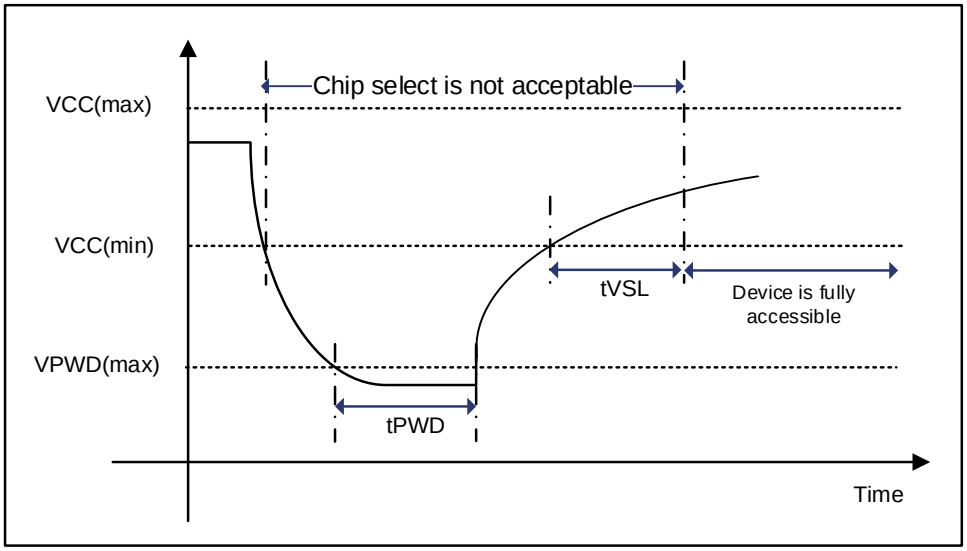


Figure 10-3 Power-Down Requirement



10.4 DC Characteristics

(T_A = -40℃~85℃, VCC=1.65~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
ILI	Input Leakage Current				±2	μA
ILO	Output Leakage Current				±2	μA
ICC1	Standby Current	/CS=VCC, VIN=VCC or VSS		20	160	μA
ICC2	Deep Power-Down Current	/CS=VCC, VIN=VCC or VSS		5	60	μA
ICC3	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 133MHz, Q=Open(x4 I/O)		12	30	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(x4 I/O)		10	25	mA
ICC5	Operating Current (PP)	/CS=VCC		12	20	mA
ICC6	Operating Current (WRSR)	/CS=VCC		8	20	mA
ICC7	Operating Current (SE)	/CS=VCC		8	20	mA
ICC7	Operating Current (BE)	/CS=VCC		8	20	mA
ICC7	Operating Current (CE)	/CS=VCC		10	20	mA
ICC8	RPMC OP1 Write Only	/CS = VCC		15	20	mA
ICC9	RPMC OP1 & Array Read	CLK = 0.1 VCC / 0.9 VCC DO=Open		19	40	mA
ICC10	RPMC OP1 & Array Program/Erase	/CS = VCC		35	45	mA
ICC11	RPMC OP2 Read Only	CLK = 0.1VCC / 0.9VCC			30	mA
ICC12	RPMC OP2 & Array Program/Erase	CLK = 0.1VCC / 0.9VCC		30	45	mA
VIL	Input Low Voltage				0.3VCC	V
VIH	Input High Voltage		0.7VCC			V
VOL	Output Low Voltage	IOL = 100μA			0.2	V
VOH	Output High Voltage	IOH = -100μA	VCC – 0.2			V

Note:

1. *Typical value at T_A = 25℃, VCC = 1.8V.*
2. *Value guaranteed by design and/or characterization, not 100% tested in production.*

10.5 AC Measurement Conditions(1)

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	CL		30	pF
Input Rise and Fall Times	TR, TF		5	ns
Input Pulse Voltages	VIN	0.1 VCC to 0. 8VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note: Output Hi-Z is defined as the point where data out is no longer driven.

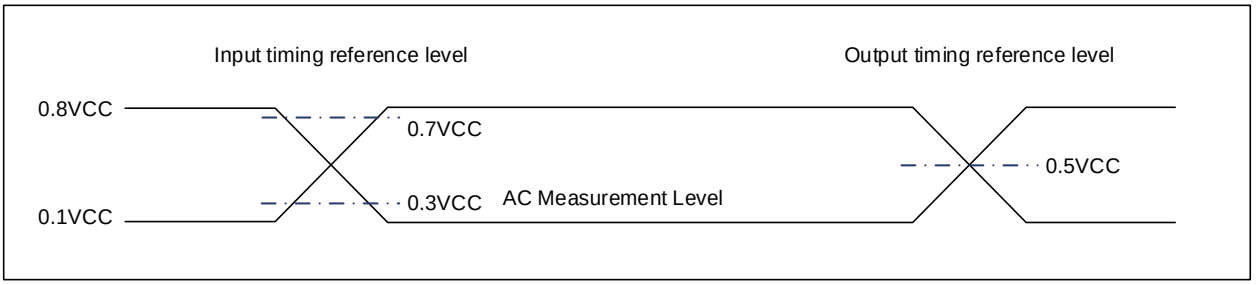


Figure 10-4 AC Measurement I/O Waveform

10.6 AC Characteristics(5)

(TA = -40℃~85℃)

Parameter	Symbol	ALT	Min.	Typ.	Max.	Unit.
Serial Clock Frequency For: all commands except Read (03H,13H)	fc	fC1	D.C.		133	MHz
Serial Clock Frequency For: RPMC Instructions	Fr		D.C.		80	MHz
Serial Clock Frequency For: Read (03H, 13H)	fR		D.C.		80	MHz
Serial Clock High Time	tCLH(1)		45% PC			ns
Serial Clock Low Time	tCLL(1)					ns
Serial Clock Rise Time (Slew Rate)	tCLCH		0.1			V/ns
Serial Clock Fall Time (Slew Rate)	tCHCL		0.1			V/ns
/CS Active Setup Time relative to CLK	tSLCH	tCSS	5			ns
/CS Active Hold Time relative to CLK	tCHSH		5			ns
/CS Not Active Setup Time relative to CLK	tSHCH	tDH	5			ns
/CS Not Active Hold Time relative to CLK	tCHSL		5			ns
/CS Deselect Time (for Read)	tSHSL1	tCSH	7			ns
/CS Deselect Time (for Erase or Program or write)	tSHSL2		30			ns
Output Disable Time	tSHQZ(2)	tDIS			6	ns
Clock Low to Output Valid for 30pf	tCLQV	tV			7	ns
Clock Low to Output Valid for 15pf	tCLQV	tV			6	ns
Output Hold Time	tCLQX	tHO	1			ns
Data In Setup Time	tDVCH	tDSU	2			ns
Data In Hold Time	tCHDX	tDH	3			ns
/HOLD Active Setup Time relative to CLK	tHLCH		5			ns
/HOLD Active Hold Time relative to CLK	tCHHH		5			ns
/HOLD Not Active Setup Time relative to CLK	tHHCH		5			ns
/HOLD Not Active Hold Time relative to CLK	tCHHL		5			ns

Continued – next page AC Electrical Characteristics (cont'd)

AC Electrical Characteristics (cont'd)

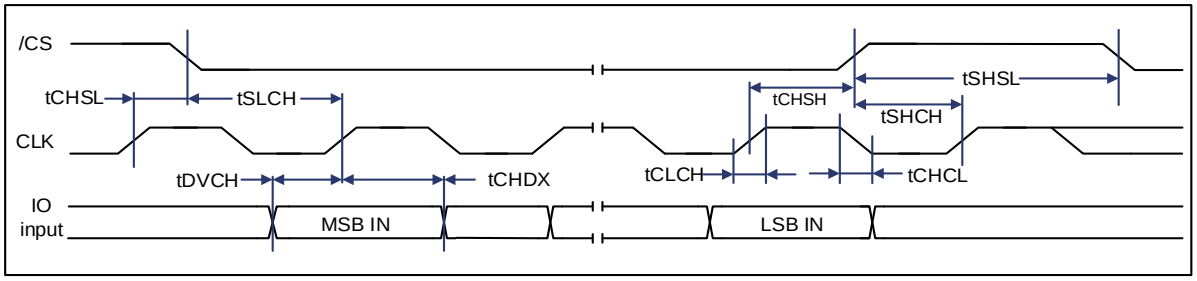
(TA = -40℃~85℃)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD to Output Low-Z	tHHQX(2)	tLZ			6	ns
/HOLD to Output High-Z	tHLQZ(2)	tHZ			6	ns
Write Protect Setup Time Before /CS Low	tWHSL(3)		20			ns
Write Protect Hold Time After /CS High	tSHWL(3)		100			ns
/CS High to Power-down Mode	tDP(2)				3	µs
/CS High to Standby Mode without ID Read	tRES1(2)				10	µs
/CS High to Standby Mode with ID Read	tRES2(2)				8.8	µs
/CS High to next Instruction after Suspend	tSUS(2)				22	µs
Latency Between Resume And Next Suspend	tERS(2)		50			µs
/RESET pin Low period to reset the device	tRESET(2)(4)		1			µs
RPMC Write Root Key Register	tKEY			170	450	µs
RPMC Update HMAC Key Register	tHMAC			50	150	µs
RPMC Increment Monotonic Counter	tINC1			40	200	us
RPMC Increment Monotonic Counter (Counter Switching)	tINC2			50	400	ms
RPMC Request Monotonic Counter	tREQ			40	120	µs
Write Status Register Time	tW			1	50	ms
Page Program Time	tPP			0.25	2	ms
Sector Erase Time (4KB)	tSE			25	300	ms
Block Erase Time (32KB)	tBE1			80	800	ms
Block Erase Time (64KB)	tBE2			120	1000	ms
Chip Erase Time	tCE			60	300	s
Software Reset Latency (WIP = write operation)	tSR				28	µs
Software Reset Latency (WIP = not in write operation)	tSR				0.3	µs
the maximum time to enter the Ultra-Deep Power-Down mode	tEUDPD				12	µs
/CS low to /CS high time (Exit Ultra-Deep Power-Down mode)	tCSLU		100			ns
/CS high to exit (Exit Ultra-Deep Power-Down mode)	tXUDPD		1			ms

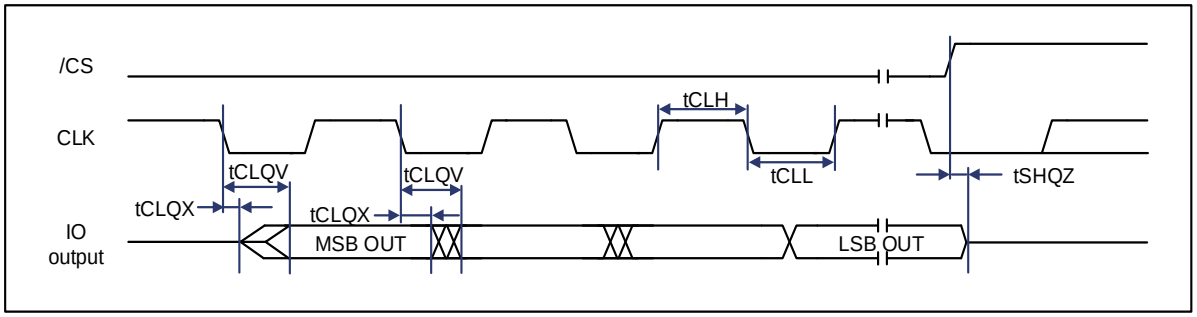
Notes:

1. *Clock high or Clock low must be more than or equal to 45%Pc. Pc=1/fc(max).*
2. *Value guaranteed by design and/or characterization, not 100% tested in production.*
3. *Only applicable as a constraint for a Write Status Register instruction when SRP[1:0]=(0,1).*
4. *It's possible to reset the device with shorter tRESET (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation.*

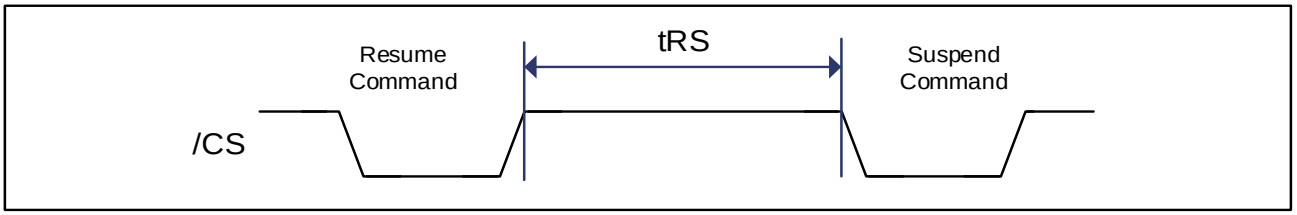
10.7 Serial Input Timing



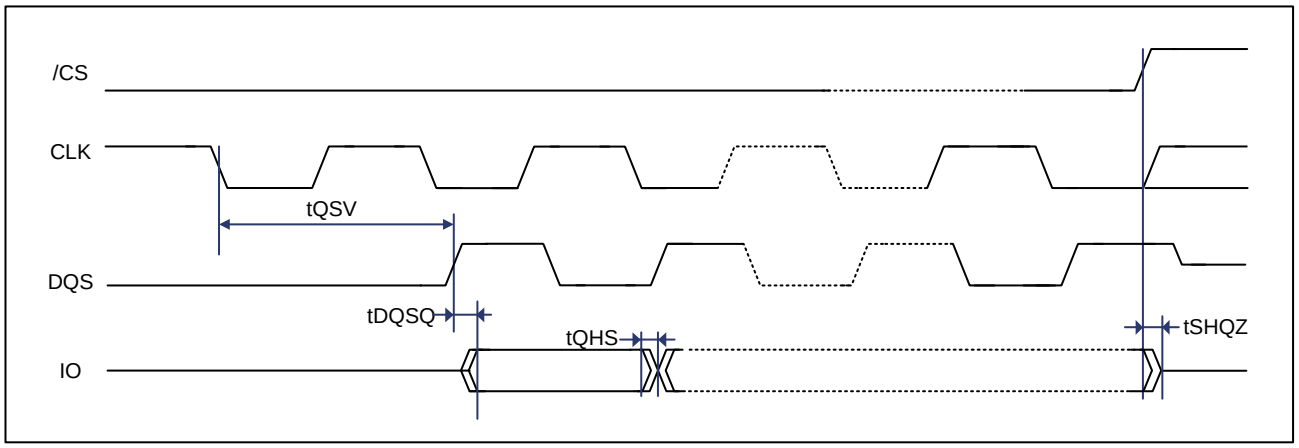
10.8 Serial Output Timing



10.9 Resume to Suspend Timing Diagram

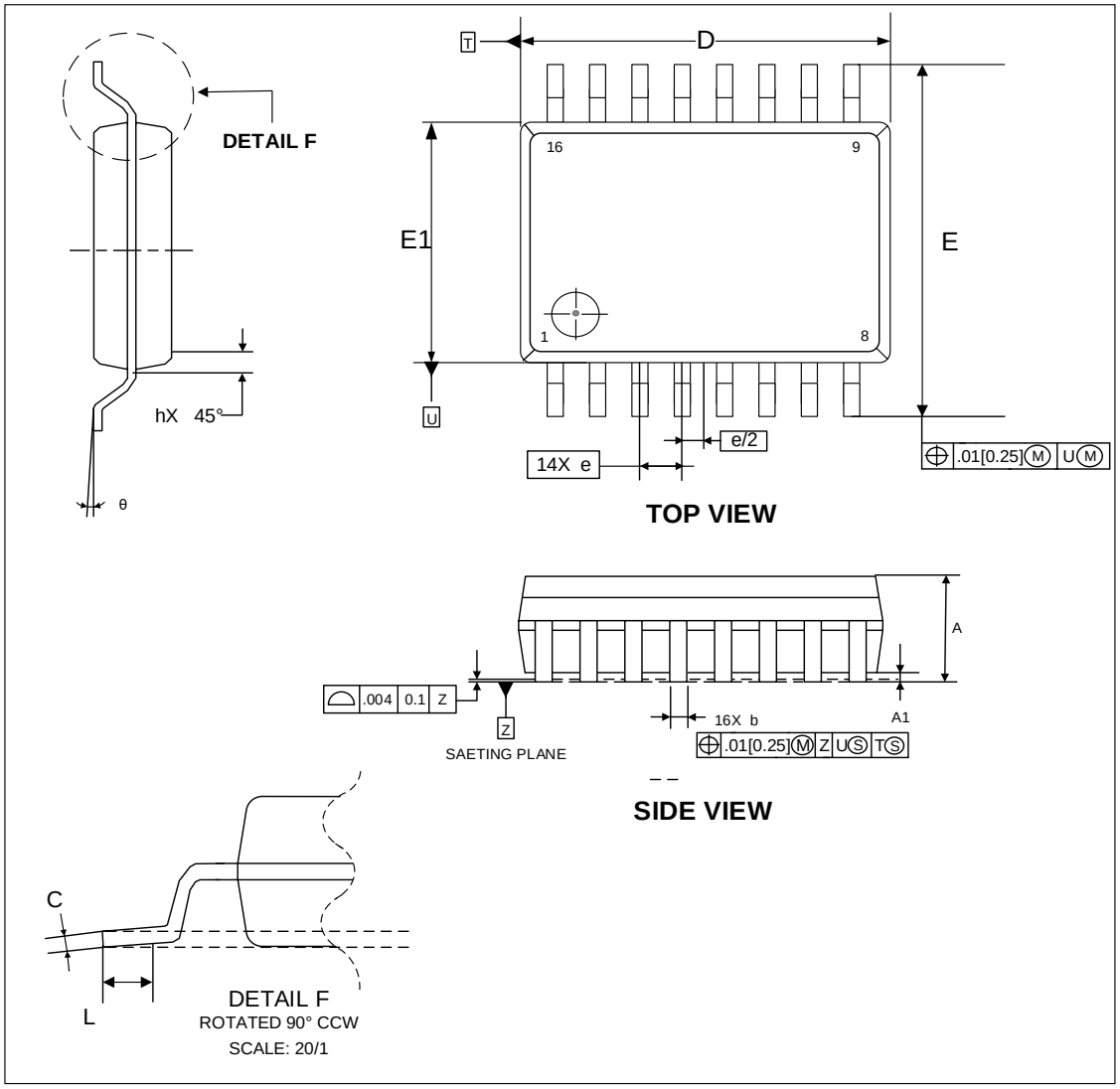


10.10 DQS Output Timing (STR)



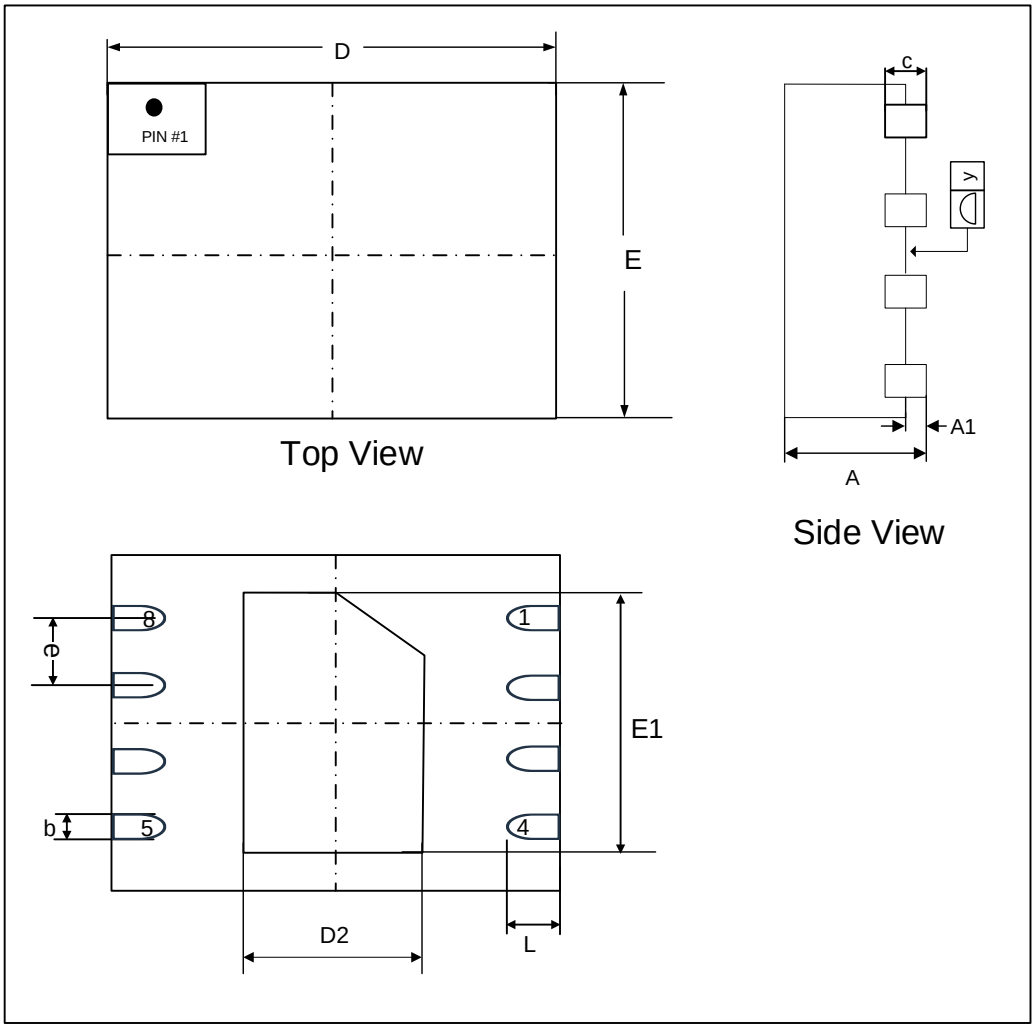
11 PACKAGE INFORMATION

11.1 SOP 300 16L (Package K)



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
b	0.31		0.51	0.013		0.020
c	0.23		0.32	0.009		0.013
D	10.10		10.50	0.398		0.413
E1	7.40		7.60	0.291		0.299
E	10.00		10.63	0.394		0.419
e	1.27 BSC			0.050 BSC		
L	0.40		1.27	0.016		0.050
h	0.25		0.75	0.010		0.030
θ	0°		8°	0°		8°

11.2 WSON 6×8 8L (Package X)



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
C	---	0.20 REF	---	---	0.008 REF	---
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	3.30	3.40	3.50	0.130	0.134	0.138
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.20	4.30	4.40	0.165	0.169	0.173
e	---	1.27	---	---	0.050	---
L	0.40	0.50	0.60	0.016	0.020	0.024
y	0.00	---	0.050	0.000	---	0.002

12 REVISION HISTORY

Version No	Description	Page	Date
0.1	Initial release	All	2024-01-28
0.2	Update preliminary version	All	2024-06-11
0.3	Update package information	All	2024-11-05
1.0	1. Change ICC1 max spec from 180uA to 160uA. 2. Update WSON 6x8 package diagram.	P99 P105	2025-07-14



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