3V 16M-BIT

SERIAL FLASH MEMORY WITH

DUAL/QUAD SPI & QPI/DTR

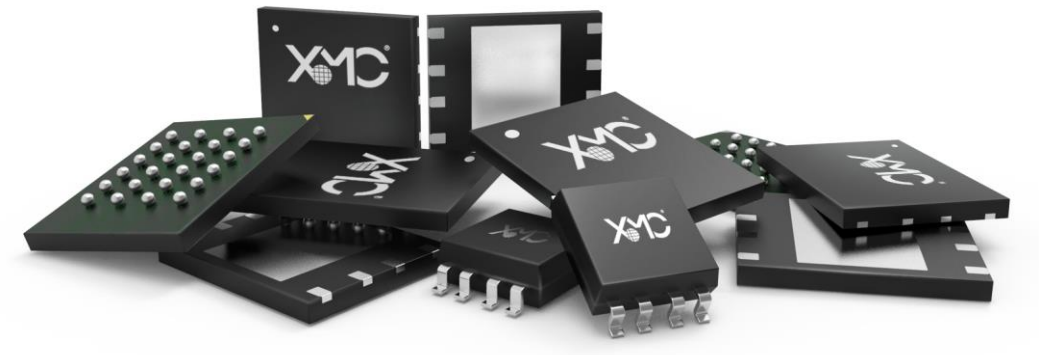


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1 FEATURES

- **New Family of SpiFlash Memories**
  - XM25QH16D: 16M-bit / 2M-Byte
  - Standard SPI: CLK, /CS, SI, SO, /WP, /Hold
  - Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - QPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - SPI/QPI DTR (Double Transfer Rate) Read
- **Highest Performance Serial Flash**
  - 166MHz Single, Dual/Quad SPI Fast Read
  - 108MHz Normal Read
  - 166MHz DTR Read
  - Configurable dummy cycle number for fast read operation
  - More than 100,000 erase/program cycles
  - More than 20-year data retention
- **Efficient "Continuous Read" and QPI Mode**
  - Continuous Read with 8/16/32/64-Byte Wrap
  - Quad Peripheral Interface (QPI) reduces instruction overhead
  - Allows true XIP (execute in place) operation
- **High performance program/erase speed**
  - Page program time: 0.2 ms typical
  - Sector erase time: 25 ms typical
  - 32KB Block erase time 50 ms typical
  - 64KB Block erase time 90 ms typical
  - Chip erase time: 2 seconds typical
- **Single Power Supply Voltage**
  - Full voltage range: 2.3-3.6V
- **Low Power Consumption，**
  - 10 μA typical standby current
  - 0.2 μA typical deep power down current
  - 3 mA typical active read current (80MHz Quad I/O)
- **Flexible Architecture**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 Byte per programmable page
  - Erase/Program Suspend & Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Top/Bottom, Complement array protection
  - 128-Bit Unique ID for each device
  - Support Serial Flash Discoverable Parameters (SFDP) signature
  - 3x1024-Byte Security Registers with OTP Locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
  - SOP 208mil 8L
  - SOP 150mil 8L
  - USON 2x3 8L
  - Contact XMC for KGD and other options

2 GENERAL DESCRIPTIONS

The XM25QH16D (16M-bit) is a serial interface Flash memory device designed for operating on a single power supply from 2.3-3.6V with current consumption as low as 0.2μA at deep power-down in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the device with its page erase granularity is ideal for data storage as well, eliminating the need for additional data storage devices.

There are 8192 programmable pages (256-Bytes each) configured in the device and up to 256 Bytes can be programmed at a time. The groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase) allow Pages to be erased. The device has 512 erasable sectors and 32 erasable blocks respectively. The small 4KB sectors afford greater flexibility for applications requiring data and parameter to be stored.

The device support standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Peripheral Interface (QPI), including Serial Clock, Chip Select, Serial Data I/O_0 (SI), I/O1 (SO), I/O_2 (/WP) and I/O_3 (/HOLD). It also supports SPI clock frequencies up to 166MHz, allowing equivalent clock rates of 332MHz for Dual I/O and 664MHz for Quad I/O when running Fast Read Dual/Quad I/O and QPI instructions. device also adds support for DTR (Double Transfer Rate) instructions, which can exceed the transfer rates of standard Asynchronous 8 and 16-bit Parallel Flash memories. with a 24-bit address being read in just 8-clocks of instruction overhead, the Continuous Read Mode enables efficient memory access, allowing true XIP (execute in place) operation.

Moreover, there are a Hold pin, Write Protect pin and programmable write protection with top or bottom array control to provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device ID and SFDP Register, a 128-bit Unique Serial Number and three 1024-Bytes Security Registers.

Read performance Comparison Table

(STR Mode)[1][2]

Numbers of Dummy Cycles	Fast Read （0BH） (MHZ)	Fast Read Dual Output (3BH) (MHZ)	Fast Read Quad Output （6BH) (MHZ)	Fast Read Dual I/O (BBH) (MHZ)	Word Read Quad I/O (E7H) (MHZ)	Fast Read Quad I/O (EBH) (MHZ)
4	-	-	-	80*	80*	80
6	-	-	-	-	-	108*
8	166*	166*	166*	166	166	133
10	-	-	-	-	-	166

(DTR Mode)[1][2]

Numbers of Dummy Cycles	DTR Fast Read (0DH) (MHZ)	DTR Fast Read Dual I/O (BDH) (MHZ)	DTR Fast Read Quad I/O (EDH) (MHZ)
4	80	80	80
6	108*	108*	108
8	133	133	133*
10	166	166	166

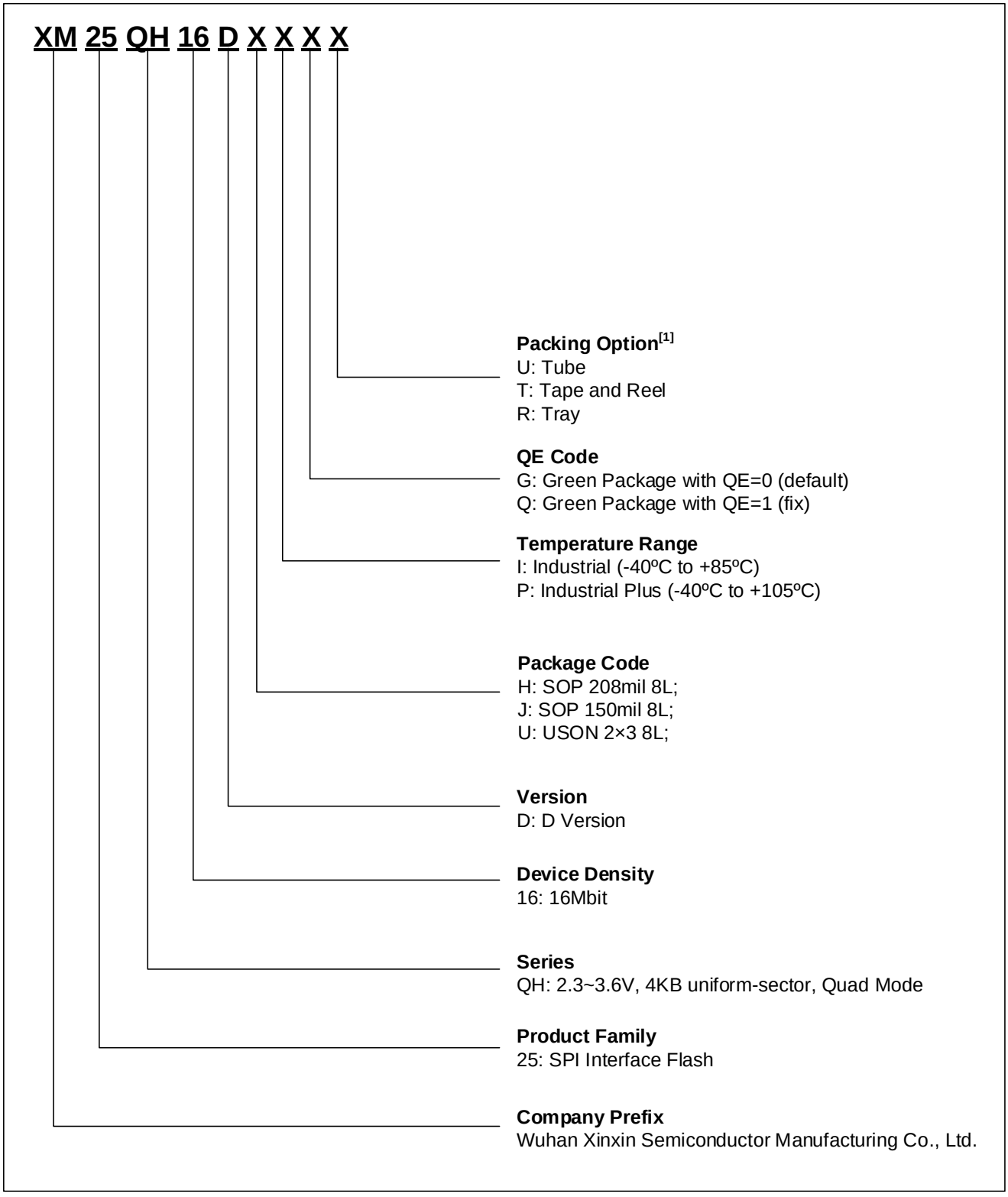
Note:

*[1] * Mean default status;*

[2]: For 4 I/O command, the start alignment address should keep [A1, A0] = (0,0)

3 ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following:

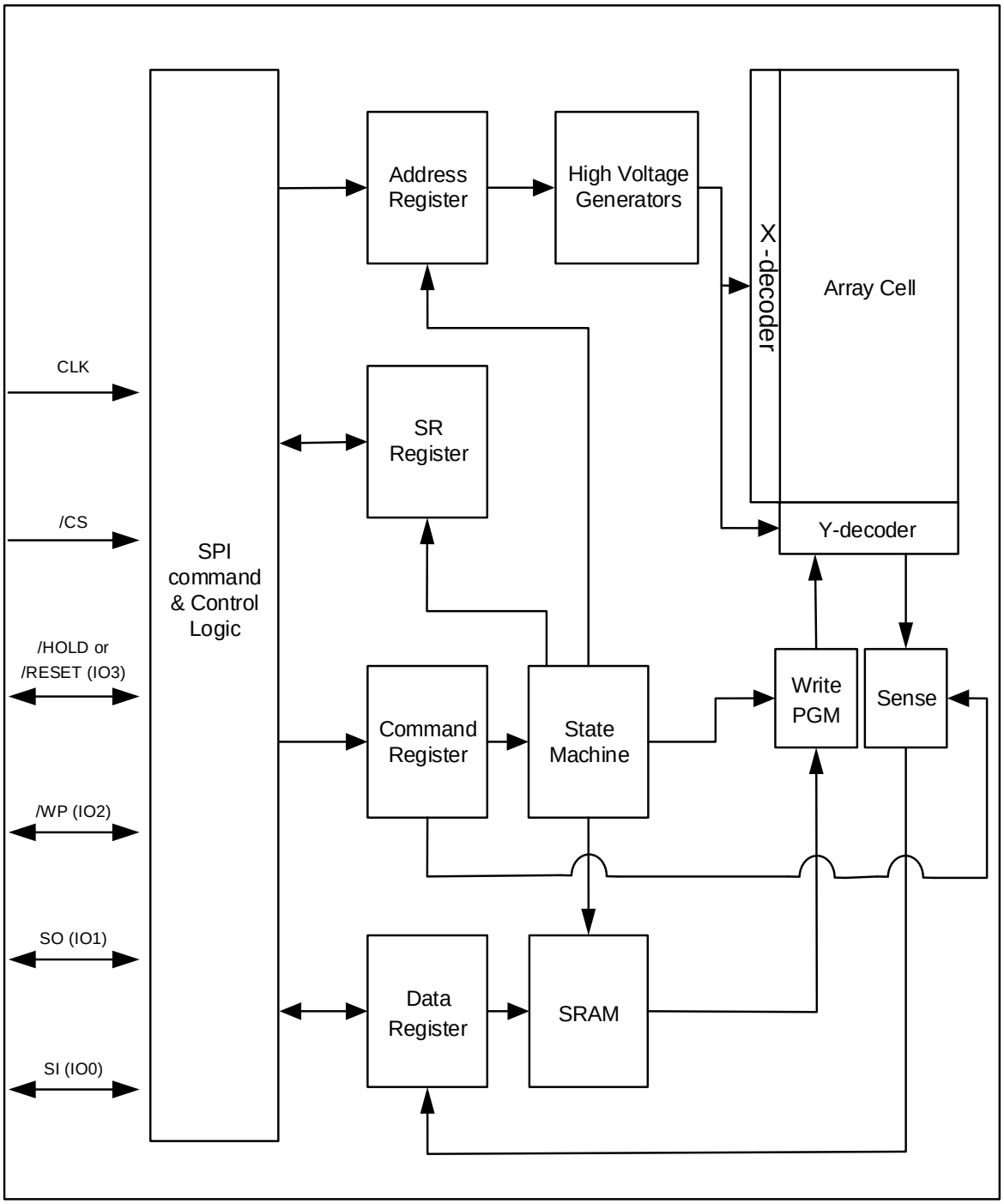


Note:

[1] This option code is not included on the part marking;

4 BLOCK DIAGRAM

Figure 4-1 XM25QH16D Serial Flash Memory Block Diagram



5 CONNECTION DIAGRAMS

Figure 5-1 8-pin SOP 208-mil & 150-mil (Package Code H and J)

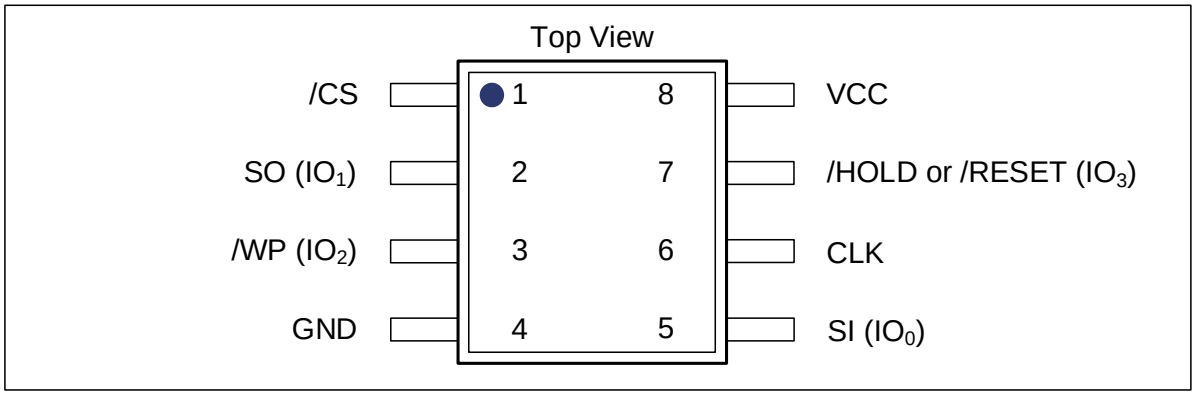
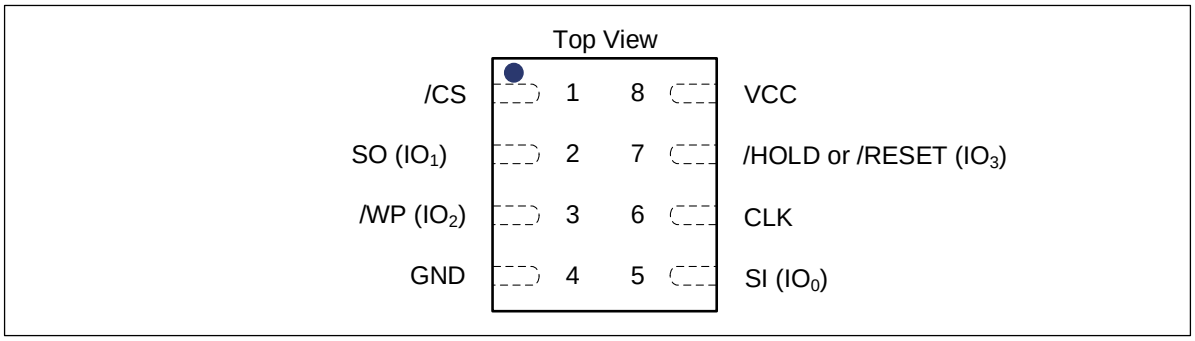


Figure 5-2 8-pad USON (Package Code U)



Pin description

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	SO (IO_1)	I/O	Data Output (Data Input Output 1)[1]
3	/WP (IO_2)	I/O	Write Protect Input (Data Input Output 2)[2]
4	GND		Ground
5	SI (IO_0)	I/O	Data Input (Data Input Output 0)[1]
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO_3)	I/O	Hold or Reset Input (Data Input Output 3)[2]
8	VCC		Power Supply

Notes:

[1] IO_0 and IO_1 are used for Standard and Dual SPI instructions;

[2] IO_0 – IO_3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.

6 SIGNAL DESCRIPTIONS

6.1 Chip Select (/CS)

The SPI Chip Select (/CS) pin is used to operate the device. The device is deselected when /CS is high and the serial data output (SO, or IO_0, IO_1, IO_2, IO_3) pins are under high impedance. When deselected, the devices power consumption will be at standby levels except when there is an internal erase, program or write status register cycle in progress. When /CS is low the device will be selected, power consumption will increase to the active levels and instructions can be written to and data read from the device. After power-up, /CS must change from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down (as indicated in “Write Protection” and Figure 10-2). Note that there was an internal pull-up resistor on the /CS pin to achieve this.

6.2 Serial Data Input, Output and IOs (SI, SO and IO_0, IO_1, IO_2, IO_3)

The device supports standard SPI, Dual SPI and Quad SPI operation.

The Standard SPI instructions write instructions, addresses or data to the device serially on the rising edge of the serial clock (CLK) input pin with the use of the unidirectional SI (input) pin. Standard SPI also uses the unidirectional SO (output) to read data or status from the device on the falling edge of CLK. The Dual and Quad SPI instructions use bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. The Quad SPI instructions demands that the non-volatile Quad Enable bit (QE) in Status Register-2 be set. When QE=1, the /WP pin turns into IO_2 and /HOLD pin becomes IO_3.

6.3 Write Protect (/WP)

To prevent the Status Register from being written, the Write Protect (/WP) pin can be configured. When the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits work together with the Status Register Protect (SRP) bits, anything from a small 4KB sector to an entire memory array can be protected by hardware. The /WP pin is active low. When the QE bit of Status Register-2 is set to Quad I/O, the /WP pin function is not available as this pin is used for IO_2. Figure 5-1/2/3 reveals the pin configuration of Quad I/O operation. Note that there was an internal pull-up resistor on the /WP pin to avoid accidentally trigging WP function by pin floating.

6.4 HOLD (/HOLD)

The /HOLD pin allows the device to be suspended while it is actively selected. When /HOLD is set low, the SO pin will be under high impedance as /CS is low and the signals on the DI and CLK pins will be ignored (of no concern) When /HOLD is set high, device operation can be resumed. The /HOLD function can be helpful when multiple devices share the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set to Quad I/O, the /HOLD pin function is not available since this pin is being used for IO_3. Figure 5-1/2/3 shows the pin configuration of Quad I/O operation. Note that there was an internal pull-up resistor on the /HOLD pin to avoid accidentally trigging HOLD function by pin floating.

6.5 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides timing for serial input and output operations. ("See SPI Operations").

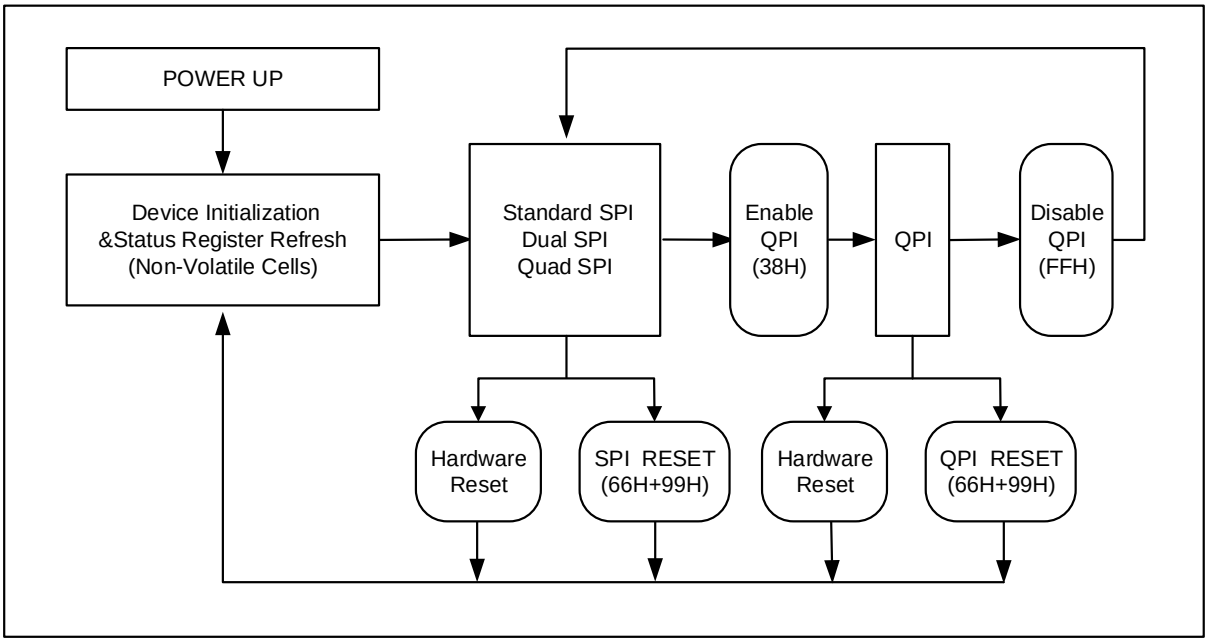
6.6 Reset (/RESET)

The /RESET pin enables the controller to reset the device. For 8-pin packages, when QE=0, the IO_3 pin can be configured as either the /HOLD pin or the /RESET pin, depending on Status Register setting. When QE=1, the /HOLD or /RESET function is not available for the 8-pin configuration. Note that there was an internal pull-up resistor on the /RESET pin to avoid accidentally trigging /RESET function by pin floating.

7 FUNCTIONAL DESCRIPTIONS

7.1 SPI / QPI Operations

Figure 7-1 XM25QH16D Serial Flash Memory Operation Diagram



7.1.1 Standard SPI Instructions

The device of XM25QH16D features a serial peripheral interface on four signals bus, namely, Serial Clock (CLK), Chip Select (/CS), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. The Input data is latched on the rising edge of CLK and data shifts out on the falling edge of CLK. For Mode 0, the CLK signal is typically low on the falling and rising edges of /CS. For Mode 3, the CLK signal is typically high on the falling and rising edges of /CS.

7.1.2 Dual SPI Instructions

When using instructions such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”, the Dual SPI operation is supported in the device. These instructions allow data to be transferred to or from the device at twice the rate of the standard SPI. When working in the Dual SPI instructions, the SI and SO pins act as bidirectional I/O pins: IO_0 and IO_1.

7.1.3 Quad SPI Instructions

When using the “Quad Output Fast Read” and “Quad I/O Fast Read” (6BH, EBH) instructions, the Quad SPI operation is supported in the device. These instructions allow data to be transferred to or from the device at four times the rate of the standard SPI. When working in the Quad SPI instructions, the SI and SO pins act as bidirectional I/O pins: IO_0 and IO_1, and the /WP and /HOLD pins act as bidirectional I/O pins: IO_2 and IO_3. The Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register set to 1

7.1.4 SPI / QPI DTR Read Instructions

Throughput of read operations can be effectively improved without increasing the serial clock frequency by device introducing multiple DTR (Double Transfer Rate) Read instructions that support Standard/Dual/Quad SPI and QPI modes. Similar to all other SPI/QPI instructions, the Byte-long instruction code is still latched into the device on the rising edge of the serial clock. When the device uses the DTR instruction code, the address input and data output will be latched on the rising as well as falling edges of the serial clock.

7.1.5 QPI Instructions

The device supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enable the QPI (38H)” instruction. The QPI mode utilizes all four IO pins to input the command code with less serial clocks to improve system performance in an XIP environment.

Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given times. The “Enter QPI (38h)” and “Exit QPI (FFh)” instructions are applied to switch the device between these two modes.

Upon power-up or after a software reset with “Reset (99h)” instruction, the default state of the device is Standard/Dual/Quad SPI mode. The QPI commands require the non-volatile Quad Enable bit (QE) in Status Register set to 1. When the QPI instruction is under function, the SI and SO pins become bidirectional IO_0 and IO_1, and the /WP and /HOLD pins become $_{IO2}$ and IO_3 respectively. The device's operation modes are shown in Figure 7-1.

7.1.6 Hold Function

The /HOLD signal is designed to give the device permission to suspend operation when actively selected (when /CS is low) in Standard / Dual SPI operations. The HOLD function is available when QE=0. If QE=1, The HOLD function is disabled, and the /HOLD pin acts as dedicated data I/O pin. The /HOLD signal goes low to stop any serial communications with the device, except the operation of write status register, programming, or erasing in progress.

The operation of HOLD needs /CS keep low, and starts on falling edge of the /HOLD signal, with CLK signal being low. If not, HOLD operation will not start until CLK is low. The HOLD condition ends on rising edge of /HOLD signal with CLK being low. If not, HOLD operation will not end until CLK is low. The SO is high impedance, both SI and CLK don’t care during the HOLD operation. When /CS is driven high during HOLD operation, the internal logic of the device will be reset. To re-start communication with the chip, the /HOLD must be at high and then /CS must be at low.

7.1.7 Software Reset & Hardware / RESET pin

The software Reset sequence allows the device to reset to the initial power on state (SPI/QPI mode) which must consist of two consecutive command: Enable Reset (66h) & Reset (99h). The device can also be configured under the hardware /RESET pin for the WSON-8 and TFBGA package types. The HOLD/RESET bit in the Status Register-3 is set for either /HOLD pin or RESET pin function. When the HOLD/RESET=0 (default) and HOLD/RESET=1, the pin acts as the /HOLD pin and /RESET pin respectively. When the QE bit is set to 1, the /HOLD or /RESET function will be disabled and the pin will act as one of the four data I/O pins. Of all the input signals, the hardware /RESET pin has the highest priority.

It will take approximately tSR for the device to restore if the command sequence is successfully received, and no commands will be accepted during reset. Any on-going external/internal operations will be interrupted by driving /RESET low for a minimum period of ~1us (tRESET*), regardless the status of other SPI signals (/CS, CLK, IOs, /WP and/or /HOLD).

Note:

While a faster /RESET pulse (as short as a few hundred nanoseconds) generally resets the device, a minimum of 1us is recommended to ensure reliable operation.

7.2 Write Protection

The possibility of noise and other adverse system conditions that may compromise data integrity must be taken into account in Applications working with non-volatile memory. There are several means to protect the data from being inadvertently written.

7.2.1 Write Protect Features

- *Reset of the device will be triggered when VCC falls below threshold*
- *Time delay write disable after Power-up*
- *Write enable/disable instructions and automatic write disable after erase or program*
- *Software and Hardware (/WP pin) write protection using Status Registers*
- *Write Protection with Power-down instruction*
- *Lock Down write protection for Status Register until the next power-up*
- *One Time Program (OTP) write protection for array and Security Registers using Status Register**

** Note: This feature requires special order. Please contact XMC for further details.*

As indicated in Figure 10-2, upon power-up or at power-down, the VCC voltage determines the status of device. While VCC is below the threshold value of V_{WI}. all operations are deactivated and no instructions are recognized. After the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of tPUW, including Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register. The /CS pin must track the VCC supply level at power-up status until the VCC-min level and tVSL time delay are met, and it must also keep track of the VCC supply level at power-down status to prevent adverse command sequence as indicated in Figure 10-3. Note that there was an internal pull-up resistor on the /CS pin to achieve this.

After power-up, the device is automatically rendered write-disabled and the Write Enable Latch (WEL) in the Status Register is set to a 0. Before a Page/Erase/Write Status Register instruction can be accepted, a Write Enable instruction must be issued. After the instruction finished, the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is achieved by issuing the Write Status Register instruction and setting the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, SEC, TB, BP[2:0]) bits. These settings can set parts or the entire memory array as read-only. Used together with the Write Protect (/WP) pin, changes to the Status Register can be activated or deactivated under hardware control.

Further information on the above instructions can be referred to the Status Register section. Moreover, the Power-down instruction provides an extra level of write protection, as all instructions are omitted except for the Release Power-down instruction.

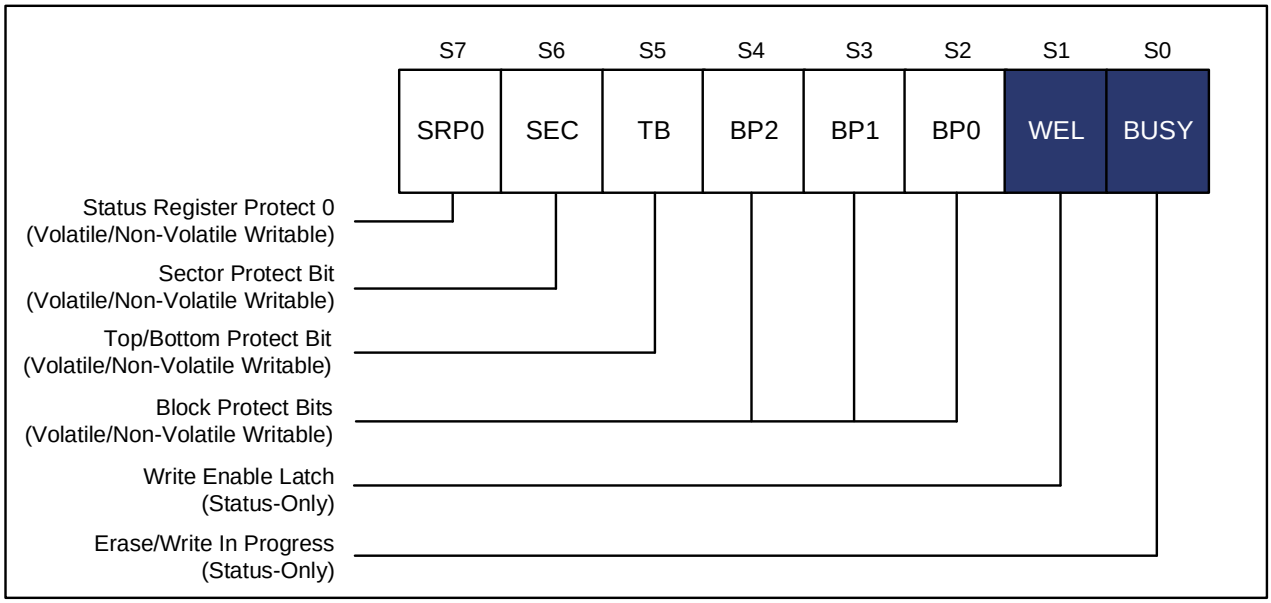
8 STATUS AND CONFIGURATION REGISTERS

The device supports three Status and Configuration Registers, including the Read Status Register-1/2/3 instructions. These instructions can be adopted to provide the availability status of the flash memory array, whether the device is write enabled or disabled, the state of write protection, the Quad SPI setting, the Security Register lock status, the Erase/Program Suspend status and the output driver strength.

While the Write Status Register instruction can be applied to configure the device write protection features, the Quad SPI setting, the Security Register OTP locks, Hold/Reset functions, output driver strength. Write access to the Status Register is determined by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and the /WP pin during Standard/Dual SPI operations.

8.1 Status Registers

Figure 8-1 Status Register-1



8.1.1 Erase/Write in Progress (BUSY) – Status Only

The BUSY bit will be reset to the state of 0, demonstrating the readiness of the device to accept further instructions when the instructions of program, erase or write status/security register instruction are executed.

When the device is performing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction, the BUSY bit is a read-only bit in the status register (S0) that is set to the state of 1. During this time, the device will ignore further instructions except the Read Status Register and Erase/Program Suspend instructions (as indicated by tW, tPP, tSE, tBE, and tCE in AC Characteristics).

8.1.2 Write Enable Latch (WEL) – Status Only

After the Write Enable Instruction is executed, the Write Enable Latch (WEL) is a read-only bit in the status register (S1) that is set to 1. The WEL status bit is cleared to 0 when the device is write disabled. At power-up or after the execution of any of the following instructions, namely, Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register, the write disable state is achieved.

8.1.3 Block Protect Bits (BP2, BP1, BP0) – Volatile/Non-Volatile Writable

As indicated by tW in AC characteristics, the Block Protect Bits (BP2, BP1 and BP0) are read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set with the Write Status Register Instruction. It is possible for all, none or part of a memory array to be protected from Program and Erase instructions (The Status Register Memory Protection table can be referred to for more detailed). The factory default setting for the Block Protection Bits is 0, meaning that none of the arrays are protected.

8.1.4 Top/Bottom Block Protect (TB) – Volatile/Non-Volatile Writable

As shown in the Status Register Memory Protection table, the non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect the Top (TB=0) or Bottom (TB=1) of the array, and its factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

8.1.5 Sector/Block Protect Bit (SEC) – Volatile/Non-Volatile Writable

As shown in the Status Register Memory Protection table, its default setting is SEC=0. The Sector/Block Protect bit (SEC) controls whether the Block Protect Bits (BP2, BP1, BP0) protect 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) at the Top (TB=0) or Bottom (TB=1) of the array.

8.1.6 Complement Protect (CMP) – Volatile/Non-Volatile Writable

The Complement Protect bit (CMP) which functions together with the SEC, TB, BP2, BP1 and BP0 bits to provide greater flexibility for array protection is a read/write bit in the status register (S14). The default setting is CMP=0. It. Once CMP is set to 1, the array protection previously set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, the top 64KB block can be protected while the rest of the array is unprotected; when CMP=1, the top 64KB block will become unprotected while the rest of the array become read-only. For more details, please refer to the Status Register Memory Protection table.

8.1.7 Status Register Protect (SRP1, SRP0) – Volatile/Non-Volatile Writable

The Status Register Protect bits (SRP1 and SRP0) control the method of write protection, that is, software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection. And the SRP bits are read/write bits in the status register (S8 and S7).

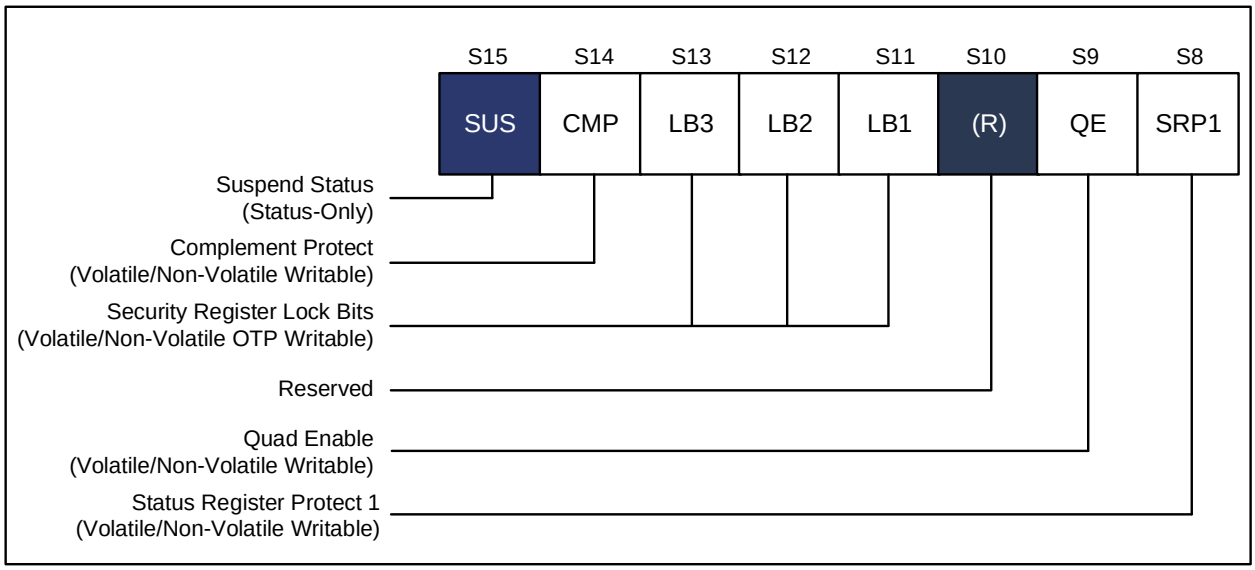
SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin has no control. The Status Register can be written to after a Write Enable instruction, WEL=1. [Factory default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle.(1)
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written to.

Note:

[1] When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state;

[2] This feature is available upon special order. Please contact XMC for details.

Figure 8-2 Status Register-2



8.1.8 Erase/Program Suspend Status (SUS) – Status Only

After running a Erase/Program Suspend (75h) instruction the Suspend Status bit is a read-only bit in the status register (S15) that is set to 1. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction and after power-down and power-up cycles.

8.1.9 Security Register Lock Bits (LB3, LB2, LB1) – Volatile/Non-Volatile OTP Writable

The Security Register Lock Bits (LB3, LB2, LB1) are non-volatile One Time Program (OTP) bits in the Status Register (S13, S12 and S11) that provide the write protect control and status to the Security Registers. The default state of LB3-1 is 0 and the Security Registers are unlocked. LB3-1 can be individually set to 1 using the Write Status Register instruction. LB3-1 is One Time Programmable (OTP), and once it is set to 1, the corresponding 1024-Byte Security Register will become permanently read-only.

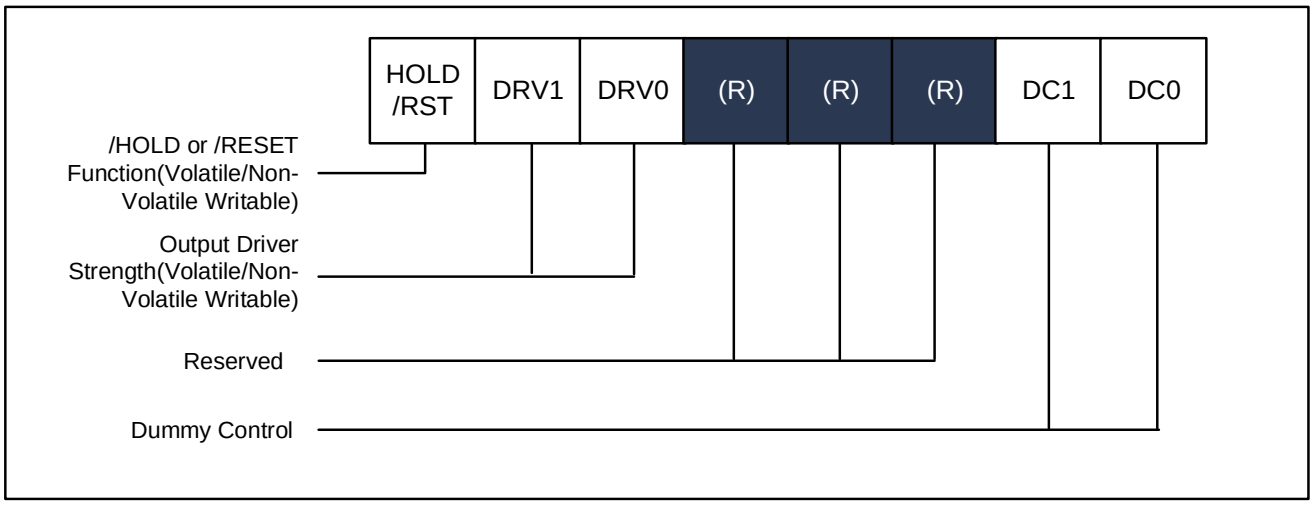
8.1.10 Quad Enable (QE) – Volatile/Non-Volatile Writable

The Quad Enable (QE) bit that allows Quad SPI and QPI operation is a read/write bit in the status register (S9). When the QE bit is set to the state of 0, the /WP and /HOLD pin are enabled. When the QE bit is set to the state of 1, the Quad IO_2 and IO_3 pins are activated, and /WP and /HOLD pin functions are deactivated.

Before issuing an “Enter QPI (38h)” to switch the device from Standard/Dual/Quad SPI to QPI, the QE bit should be set to 1, otherwise the command will be ignored. When the device is in QPI mode, the QE bit will remain at 1. The “Write Status Register” command in QPI mode cannot change the QE bit from “1” to “0”.

WARNING: The QE bit should never be set to 1 in the case where the /WP or /HOLD pin is directly connected to the power supply or ground during standard SPI or Dual SPI operation.

Figure 8-3 Status Register-3



8.1.11 Output Driver Strength (DRV1, DRV0) – Volatile/Non-Volatile Writable

The DRV1 & DRV0 bits are applied to determine the output driver strength for Read operations.

DRV1, DRV0	Driver Strength
0, 0	100%
0, 1	75% (default)
1, 0	50%
1, 1	25%

8.1.12 /HOLD or /RESET Pin Function (HOLD/RST) – Volatile/Non-Volatile Writable

Setting the HOLD/RST bit can determine whether the /HOLD or /RESET function will be implemented on the hardware pin for 8-pin packages. When HOLD/RESET=0, that is factory default, the pin acts as /HOLD; when HOLD/RESET=1, the pin acts as /RESET; however, /HOLD or /RESET functions are only available when QE=0. If QE equals to 1, the /HOLD and /RESET functions are disabled, and the pin acts as a dedicated data I/O pin.

8.1.13 Dummy Cycle Bits

The Dummy Cycle Bits (DC1&DC0) are used to determine the Max Frequency for Read operations.

（STR Mode）

DC[1:0]	Numbers of Dummy clock cycles	Fast Read	Fast Read Dual Output	Fast Read Quad Output
00(default)	8	166MHz	166MHz	166MHz
01	8	166MHz	166MHz	166MHz
10	8	166MHz	166MHz	166MHz
11	8	166MHz	166MHz	166MHz

DC[1:0]	Numbers of Dummy clock cycles	Fast Read Dual I/O	Word Read Quad I/O
00(default)	4	80MHz	80MHz
01	8	166MHz	166MHz
10	4	80MHz	80MHz
11	8	166MHz	166MHz

DC[1:0]	Numbers of Dummy clock cycles	Fast Read Quad I/O
00(default)	6	108MHz
01	4	80MHz
10	8	133MHz
11	10	166MHz

（DTR Mode）

DC[1:0]	Numbers of Dummy clock cycles	DTR Fast Read	DTR Fast Read Dual I/O
00(default)	6	108MHz	108MHz
01	4	80MHz	80MHz
10	8	133MHz	133MHz
11	10	166MHz	166MHz

DC[1:0]	Numbers of Dummy clock cycles	DTR Fast Read Quad I/O
00(default)	8	133MHz
01	4	80MHz
10	6	108MHz
11	10	166MHz

Note 1: For 4 I/O command, the start alignment address should keep [A1, A0] = (0,0)

8.1.14 Reserved Bits – Non Functional

There are several reserved Status Register bits that may be read out as “0” or “1” and it is recommended that the value of these bits be ignored. During the “Write Status Register” instruction, the Reserved Bits can be written as “0” without any implications.

XM25QH16D Status Register Memory Protection (CMP = 0)

STATUS REGISTER[1]					XM25QH16D (16M-BIT) MEMORY PROTECTION[3]			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION[2]
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	31	1F0000h – 1FFFFFh	64KB	Upper 1/32
0	0	0	1	0	30 and 31	1E0000h – 1FFFFFh	128KB	Upper 1/16
0	0	0	1	1	28 thru 31	1C0000h – 1FFFFFh	256KB	Upper 1/8
0	0	1	0	0	24 thru 31	180000h – 1FFFFFh	512KB	Upper 1/4
0	0	1	0	1	16 thru 31	100000h – 1FFFFFh	1MB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/32
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/16
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/8
0	1	1	0	0	0 thru 7	000000h – 07FFFFh	512KB	Lower 1/4
0	1	1	0	1	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/2
X	X	1	1	X	0 thru 31	000000h – 1FFFFFh	2MB	ALL
1	0	0	0	1	31	1FF000h – 1FFFFFh	4KB	U - 1/512
1	0	0	1	0	31	1FE000h – 1FFFFFh	8KB	U - 1/256
1	0	0	1	1	31	1FC000h – 1FFFFFh	16KB	U - 1/128
1	0	1	0	X	31	1F8000h – 1FFFFFh	32KB	U - 1/64
1	1	0	0	1	0	000000h – 000FFFh	4KB	L - 1/512
1	1	0	1	0	0	000000h – 001FFFh	8KB	L - 1/256
1	1	0	1	1	0	000000h – 003FFFh	16KB	L - 1/128
1	1	1	0	X	0	000000h – 007FFFh	32KB	L - 1/64

Note:

[1] X = don't care;

[2] L = Lower; U = Upper;

[3] If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored

XM25QH16D Status Register Memory Protection (CMP = 1).

STATUS REGISTER[1]					XM25QH16D (16M-BIT) MEMORY PROTECTION[3]			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION[2]
X	X	0	0	0	0 thru 31	000000h – 1FFFFFh	2MB	ALL
0	0	0	0	1	0 thru 30	000000h – 1EFFFFh	1,984KB	Lower 31/32
0	0	0	1	0	0 thru 29	000000h – 1DFFFFh	1,920KB	Lower 15/16
0	0	0	1	1	0 thru 27	000000h – 1BFFFFh	1,792KB	Lower 7/8
0	0	1	0	0	0 thru 23	000000h – 17FFFFh	1,536KB	Lower 3/4
0	0	1	0	1	0 thru 15	000000h – 0FFFFFh	1MB	Lower 1/2
0	1	0	0	1	1 thru 31	010000h – 1FFFFFh	1,984KB	Upper 31/32
0	1	0	1	0	2 thru 31	020000h – 1FFFFFh	1,920KB	Upper 15/16
0	1	0	1	1	4 thru 31	040000h – 1FFFFFh	1,792KB	Upper 7/8
0	1	1	0	0	8 thru 31	080000h – 1FFFFFh	1,536KB	Upper 3/4
0	1	1	0	1	16 thru 31	100000h – 1FFFFFh	1MB	Upper 1/2
X	X	1	1	X	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 31	000000h – 1FEFFFh	2,044KB	L - 511/512
1	0	0	1	0	0 thru 31	000000h – 1FDFFFh	2,040KB	L - 255/256
1	0	0	1	1	0 thru 31	000000h – 1FBFFFh	2,032KB	L - 127/128
1	0	1	0	X	0 thru 31	000000h – 1F7FFFh	2,016KB	L - 63/64
1	1	0	0	1	0 thru 31	001000h – 1FFFFFh	2,044KB	U - 511/512
1	1	0	1	0	0 thru 31	002000h – 1FFFFFh	2,040KB	U - 255/256
1	1	0	1	1	0 thru 31	004000h – 1FFFFFh	2,032KB	U - 127/128
1	1	1	0	X	0 thru 31	008000h – 1FFFFFh	2,016KB	U - 63/64

Note:

[1] X = don't care;

[2] L = Lower; U = Upper;

[3] If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

9 INSTRUCTIONS

As can be seen in the Instruction Set Table1&2, The Standard/Dual/Quad SPI instruction set of the device consists of 41 basic instructions that are fully controlled through the SPI bus. Instructions are initiated with the falling edge of Chip Select (/CS). The first Byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock, with the most significant bit (MSB) preceding it.

As indicated in the Instruction Set Table 3, the QPI instruction set of the device consists of 27 basic instructions that are fully controlled via the SPI bus. Instructions are initiated with the falling edge of Chip Select (/CS). The first Byte of data clocked through IO [3:0] pins provides the instruction code. Data on all four IO pins are sampled on the rising edge of clock, with MSB preceding it. All QPI instructions, addresses, data and dummy Bytes are using all four IO pins to transfer every Byte of data at every two serial clocks (CLK).

The instructions vary in length from one to several Bytes and may be followed by address Bytes, data Bytes, dummy Bytes (do not care), and, possibly, in some cases, there will be combinations of them. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in Figure 9-1 to Figure 9-66. All read instructions can be completed after any clocked bit. However, all Write, Program or Erase instructions must be completed on a Byte boundary (/CS is driven high after a full 8-bits clocked) or the instruction will be ignored, protecting the device from inadvertent writes. Additionally, when a memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register and Erase/Program Suspend instructions will be ignored until the program or erase cycle has completed.

9.1 Device ID and Instruction Set Tables

9.1.1 Manufacturer and Device Identification

MANUFACTURER ID	(MF7 - MF0)	
XMC Serial Flash	**20h**	
Device ID	**(ID7 - ID0)**	**(ID15 - ID0)**
Instruction	**ABh, 90h, 92h, 94h**	**9Fh**
XM25QH16D	14h	4015h

9.1.2 Instruction Set Table 1 (Standard/Dual/Quad SPI Instructions)[1]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-47)**	**(48-55)**
Write Enable	**06h**						
Volatile SR Write Enable	**50h**						
Write Disable	**04h**						
Read Status Register-1	**05h**	(S7-S0)(2)					
Write Status Register-1(4)	**01h**	(S7-S0)(4)					
Read Status Register-2	**35h**	(S15-S8)(2)					
Write Status Register-2	**31h**	(S15-S8)					
Read Status Register-3	**15h**	(S23-S16)(2)					
Write Status Register-3	**11h**	(S23-S16)					
Chip Erase	**C7h/60h**						
Erase / Program Suspend	**75h**						
Erase / Program Resume	**7Ah**						
Power-down	**B9h**						
Release Power-down / ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)	
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)			
Enter QPI Mode	**38h**						
Enable Reset	**66h**						
Reset Device	**99h**						

9.1.3 Instruction Set Table 2 (Standard/Dual/Quad SPI Instructions)[1]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Clock Number	**(0–7)**	**(8–15)**	**(16–23)**	**(24–31)**	**(32–39)**	**(40–47)**
Read Unique ID	**4Bh**	Dummy	Dummy	Dummy	Dummy	(UID7-UID0)…
Page Program	**02h**	A23-A16	A15-A8	A7-A0	(D7-D0) [3]	…
Quad Input Page Program	**32h**	A23-A16	A15-A8	A7-A0	(D7-D0)[3] [9]	…
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)	…
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	Dummy*	(D7-D0)…
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	Dummy*	(D7-D0) [7]…
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	Dummy*	(D7-D0) [9]…
Read SFDP Register	**5Ah**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)…
Erase Security Register[5]	**44h**	A23-A16	A15-A8	A7-A0		
Program Security Register[5]	**42h**	A23-A16	A15-A8	A7-A0	(D7-D0)(3)	…
Read Security Register[5]	**48h**	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)…

Data Input Output	Byte 1	Byte 2[6]	Byte 3[6]	Byte 4[6]	Byte 5	Byte 6[7]	Byte 7[7]
Clock Number	**(0–7)**	**(8–11)**	**(12–15)**	**(16–19)**	**(20–23)**	**(24–27)**	**(28–31)**
Fast Read Dual I/O	**BBh**	A23-A16	A15-A8	A7-A0	Dummy*	(D7-D0)	…
Mftr./Device ID Dual I/O	**92h**	A23-A16	A15-A8	A7-A0	Dummy	(MF7-MF0)	(ID7-ID0)…

Data Input Output	Byte 1	Byte 2[8]	Byte3[8]	Byte4[8]	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Clock Number	**(0–7)**	**(8, 9)**	**(10, 11)**	**(12, 13)**	**(14, 15)**	**(16, 17)**	**(18,19)**	**(20, 21)**	**(22, 23)**
Set Burst with Wrap	**77h**	Dummy	Dummy	Dummy	W7-W0				
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy*	Dummy*	(D7-D0)	…
Word Read Quad I/O[9]	**E7h**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)	(D7-D0)	…
Mftr./Device ID Quad I/O	**94h**	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)

9.1.4 Instruction Set Table 3 (QPI Instructions)[10]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Clock Number	**(0, 1)**	**(2, 3)**	**(4, 5)**	**(6, 7)**	**(8, 9)**	**(10, 11)**
Write Enable	**06h**					
Volatile SR Write Enable	**50h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(S7-S0)[2]				
Write Status Register-1[4]	**01h**	(S7-S0)[4]				
Read Status Register-2	**35h**	(S15-S8)[2]				
Write Status Register-2	**31h**	(S15-S8)				
Read Status Register-3	**15h**	(S23-S16)[2]				
Write Status Register-3	**11h**	(S23-S16)				
Chip Erase	**C7h/60h**					
Erase / Program Suspend	**75h**					
Erase / Program Resume	**7Ah**					
Power-down	**B9h**					
Set Read Parameters	**C0h**	P7-P0				
Release Power-down / ID	**ABh**	Dummy	Dummy	Dummy	(ID7-ID0)[2]	
Manufacturer/Device ID	**90h**	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)
JEDEC ID	**9Fh**	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)		
Exit QPI Mode	**FFh**					
Enable Reset	**66h**					
Reset Device	**99h**					
Page Program	**02h**	A23-A16	A15-A8	A7-A0	(D7-D0)[9]	…
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	Dummy[11]	(D7-D0)…
Burst Read with Wrap[12]	**0Ch**	A23-A16	A15-A8	A7-A0	Dummy[11]	(D7-D0)…
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0[11]	(D7-D0)…

9.1.5 Instruction Set Table 4 (DTR with SPI Instructions)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(1-1-1)	8	4	4	4	6	4	4
DTR Fast Read	0Dh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
Number of Clock(1-2-2)	8	2	2	2	6	2	2
DTR Fast Read Dual I/O	BDh	A23-A16	A15-A8	A7-A0	M7-M0&Dummy	(D7-D0)	...
Number of Clock(1-4-4)	8	1	1	1	8	1	1
DTR Fast Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0&Dummy	(D7-D0)	(D7-D0)

9.1.6 Instruction Set Table 4 (DTR with QPI Instructions)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Number of Clock(4-4-4)	2	1	1	1	8	1	1
DTR Read with Wrap[12]	0Eh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
DTR Fast Read	0Dh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	…
DTR Fast Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0&Dummy	(D7-D0)	-

Note:

[1] Most Significant Bit is sent first when shift data Bytes. Data in "( )" indicate data output from the device on either 1, 2 or 4 IO pins.

[2] The Status Register contents and Device ID will repeat continuously until /CS pull high.

[3] (1-256) Byte of data input is required for Page Program, Quad Page Program and Program Security Registers. If more than 256 Bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.

[4] Write Status Register-1 (01h) can be used to write both Status Register-1&2.

[5] Security Register Address:

Security Register1: A23-A16=00H, A15-A12=1H, A11-A10 = 00b, A9-A0= Byte Address;

Security Register2: A23-A16=00H, A15-A12=2H, A11-A10 = 00b, A9-A0= Byte Address;

Security Register3: A23-A16=00H, A15-A12=3H, A11-A10 = 00b, A9-A0= Byte Address.

[6] Dual SPI address input format:

IO_0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0

IO_1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1

[7] Dual SPI data output format:

IO_0 = (D6, D4, D2, D0)

IO_1 = (D7, D5, D3, D1)

[8] Quad SPI address and Set Burst with Wrap Input format:

Quad SPI address input format:	Set Burst with Wrap input format:
IO_0 = A20, A16, A12, A8, A4, A0, M4, M0	IO_0 = x, x, x, x, x, x, W4, x
IO_1 = A21, A17, A13, A9, A5, A1, M5, M1	IO_1 = x, x, x, x, x, x, W5, x
IO_2 = A22, A18, A14, A10, A6, A2, M6, M2	IO_2 = x, x, x, x, x, x, W6, x
IO_3 = A23, A19, A15, A11, A7, A3, M7, M3	IO_3 = x, x, x, x, x, x, x, x

[9] Quad SPI data input/output, Fast Read Quad I/O data output and Word Read Quad I/O data output format:

Quad SPI data input/output format:	*Fast Read Quad I/O data output format:*	*Word Read Quad I/O data output format:*
IO_0 = (D4, D0, ……)	*IO_0 = (x, x, x, x, D4, D0, D4, D0)*	*IO_0 = (x, x, D4, D0, D4, D0, D4, D0)*
IO_1 = (D5, D1, ……)	*IO_1 = (x, x, x, x, D5, D1, D5, D1)*	*IO_1 = (x, x, D5, D1, D5, D1, D5, D1)*
IO_2 = (D6, D2, ……)	*IO_2 = (x, x, x, x, D6, D2, D6, D2)*	*IO_2 = (x, x, D6, D2, D6, D2, D6, D2)*
IO_3 = (D7, D3, ……)	*IO_3 = (x, x, x, x, D7, D3, D7, D3)*	*IO_3 = (x, x, D7, D3, D7, D3, D7, D3)*

[10] QPI Command, Address, Data input/output format:

	Command		*Address*						*Data input/output*				
CLK	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	……
IO_0	*C4*	*C0*	*A20*	*A16*	*A12*	*A8*	*A4*	*A0*	*D4,*	*D0*	*D4*	*D0*	……
IO_1	*C5*	*C1*	*A21*	*A17*	*A13*	*A9*	*A5*	*A1*	*D5,*	*D1*	*D5*	*D1*	……
IO_2	*C6*	*C2*	*A22*	*A18*	*A14*	*A10*	*A6*	*A2*	*D6*	*D2*	*D6*	*D2*	……
IO_3	*C7*	*C3*	*A23*	*A19*	*A15*	*A11*	*A7*	*A3*	*D7*	*D3*	*D7*	*D3*	……

[11] The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.

[12] The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.

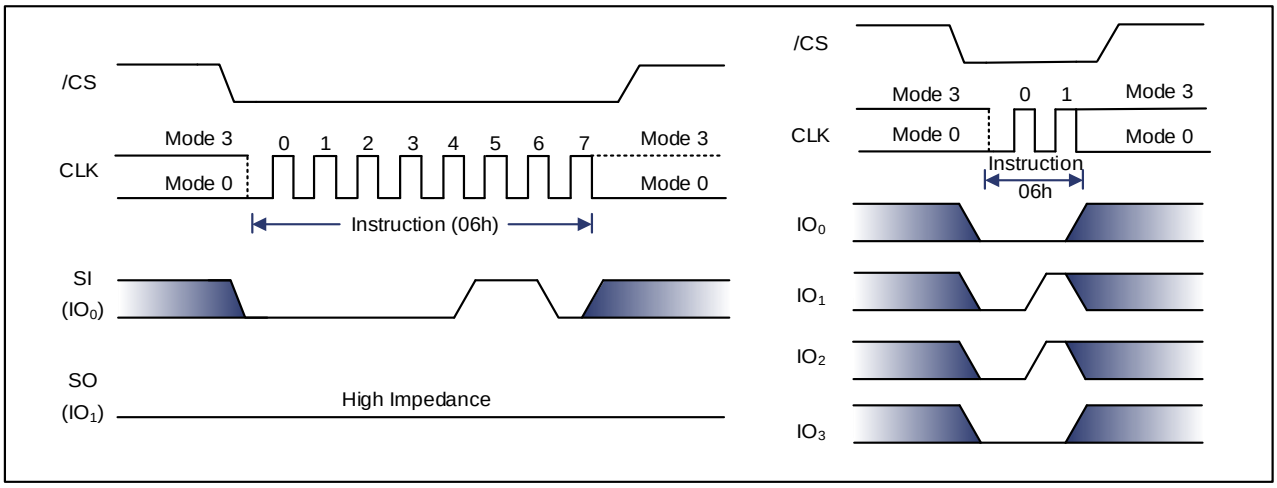
9.2 Instruction Descriptions

9.2.1 Write Enable (06h)

As indicated in Figure 9-1, the Write Enable instruction sets the Write Enable Latch (WEL) bit in the Status Register to 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instructions.

The instruction sequence as follow: set /CS low→transfer code(06h) to the SI pin→ set /CS high.

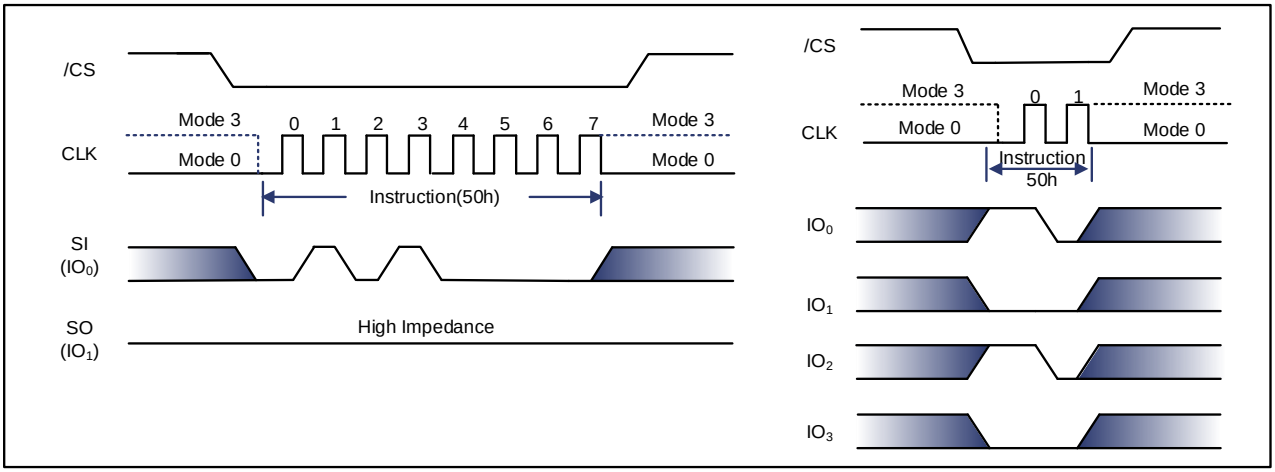
Figure 9-1 Write Enable Instruction for SPI Mode (left) or QPI Mode (right)



9.2.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits outlined in Section 8 can also be written to as volatile bits. This offers more flexibility to change the system configuration and memory protection schemes quickly without waiting for typical non-volatile bit write cycles and no need to affect the persistence of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, a Volatile Status Register (50h) Write Enable instruction must be emitted prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 9-2) will not set the Write Enable Latch (WEL) bit, rather, it only works for the Write Status Register instruction so that the volatile Status Register bit values can be changed.

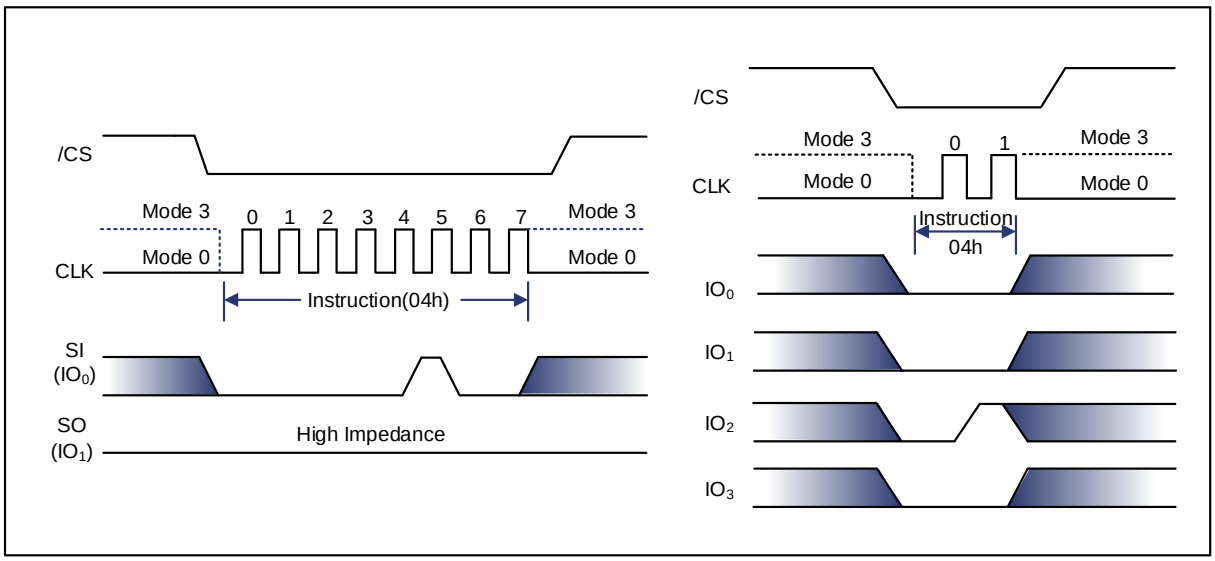
Figure 9-2 Write Enable for Volatile Status Register Instruction for SPI Mode (left) or QPI Mode (right)



9.2.3 Write Disable (04h)

As indicated in Figure 9-3, the Write Disable instruction resets the Write Enable Latch (WEL) bit in the Status Register to 0. Notably, the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset instructions. The instruction sequence: set /CS low→ shift code (06h) to the SI pin→ set /CS high.

Figure 9-3 Write Disable Instruction for SPI Mode (left) or QPI Mode (right)



9.2.4 Read Status Register-1/2/3 (05h/35h/15h)

The Read Status Register instructions enable the 8-bit Status Registers to be read. These instructions are fed by driving /CS low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 into the SI pin on the rising edge of CLK. The bits of status register are then shifted out to the SO pin first with the most significant bit (MSB) on the falling edge of CLK, as demonstrated in Figure 9-4. For a description of the Status Register, please refer to Section 8.1. The Read Status Register instruction can be applied at any time, even during a cycle of Program, Erase or Write Status Register. This allows the BUSY status bit to be checked to identify when the cycle is complete and whether the device is ready to accept another instruction. The Status Register can be read successively, as shown in Figure 9-5. Also, this instruction is completed by driving /CS high.

Figure 9-4 Read Status Register Instruction (SPI Mode)

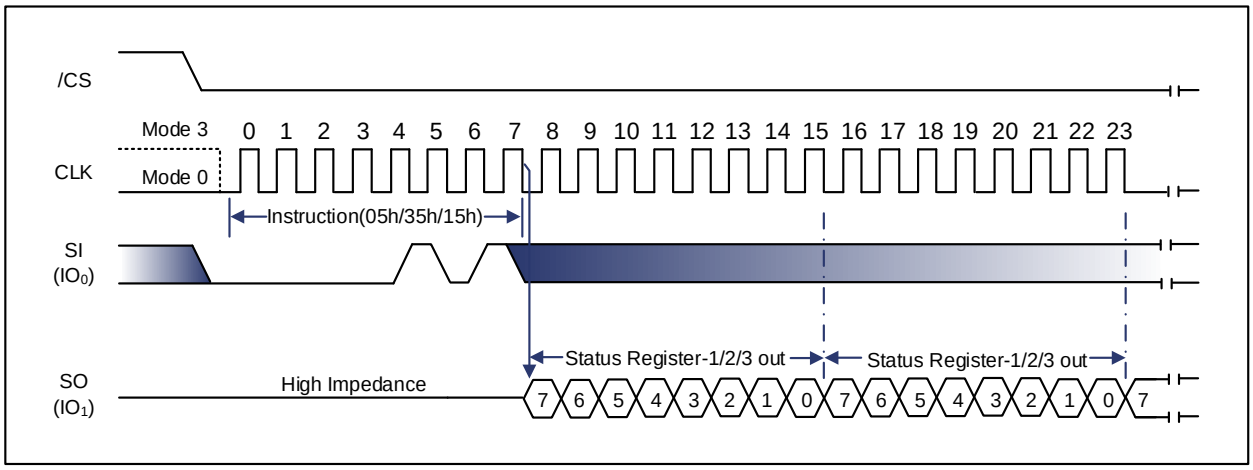
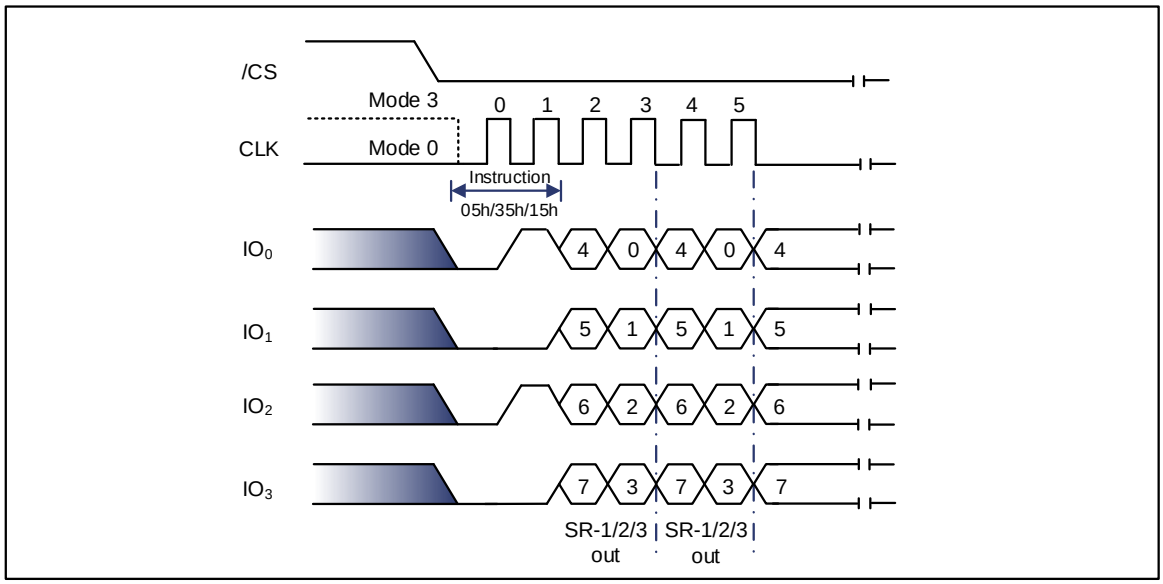


Figure 9-5 Read Status Register Instruction (QPI Mode)



9.2.5 Write Status Register-1/2/3 (01h/31h/11h)

The Write Status Register instruction allows the Status Registers to be written. The bits that can be written are shown below: SRP0, SEC, TB, BP [2:0] in Status Register-1, CMP, LB[3:1], QE, SRP1 in Status Register-2 and HOLD/RST, DRV1, DRV0, DC1, DC0 in Status Register-3. All other Status Register bit locations are read-only and are not affected by the Write Status Register instruction. LB [3:1] are non- volatile OTP bits, and cannot be cleared to 0 once it is set to 1.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must be executed beforehand so that the device can accept the Write Status Register instruction (Status Register bit WEL must be equal to 1). Once the write instruction has been activated, it will be entered by driving /CS low, and its instruction code "01h/31h/11h" will be sent, followed by writing to the status register data Byte, as illustrated in Figure 9-6 and Figure 9-7.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must be executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, SRP1 and LB [3:1] cannot be changed from “1” to “0” as these bits are protected by OTP. Upon power off or execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be retrieved.

As indicated by the Characteristics of AC, during non-volatile Status Register write operation (06h combined with 01h/31h/11h), the self-timed Write Status Register cycle will start after /CS has been driven high for a time duration of t_W. While the Write Status Register cycle is in progress, the Read Status Register instruction can still be accessed to check the status of the BUSY bit. The BUSY bit is 1 during the Write Status Register cycle and 0 when the cycle is over and ready to accept other instructions. The Write Enable Latch (WEL) bit in the status register will be cleared to 0 at the end of the Write Status Register cycle.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (as indicated by the Characteristics of AC). The BUSY bit will remain 0 during the Status Register bit refresh period.

The Write Status Register instruction is available both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, as QE=1 is required for the device to enter and operate in QPI mode, and the details on Status Register can be seen in Section 8.1.

Figure 9-6 Write Status Register-1/2/3 Instruction (SPI Mode)

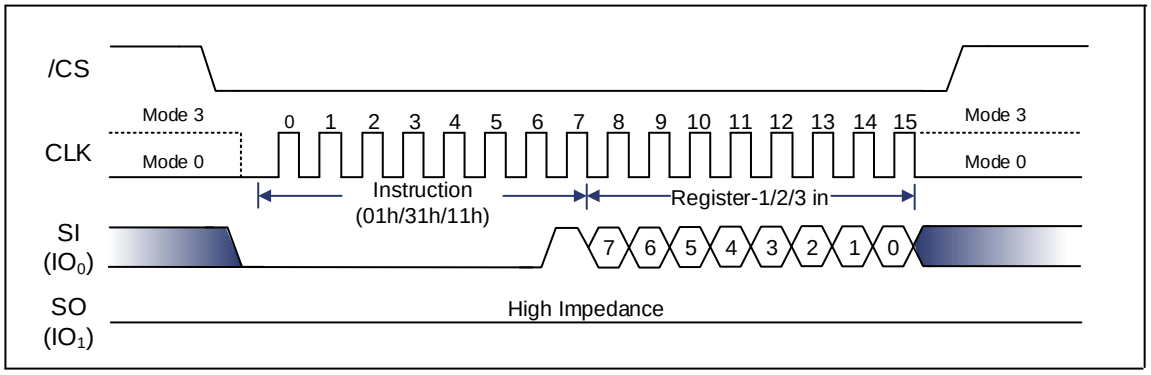
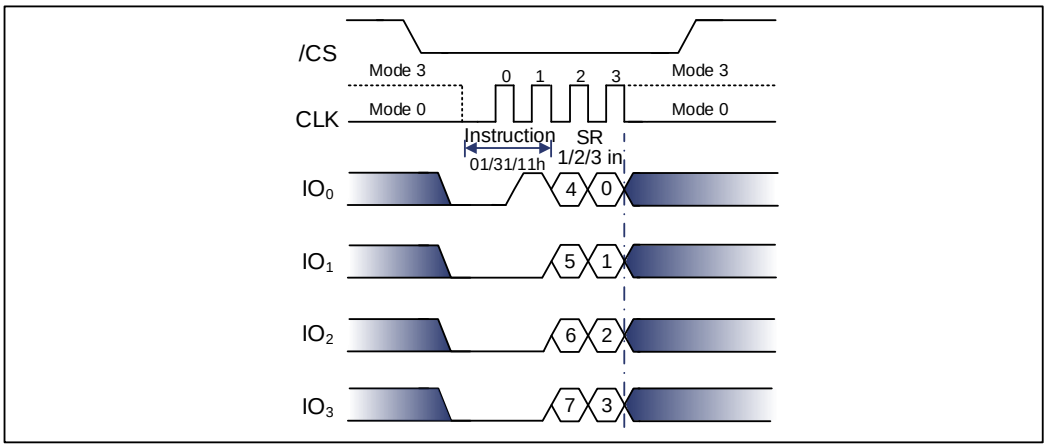


Figure 9-7 Write Status Register-1/2/3 Instruction (QPI Mode)



The device is also backwards compatible with previous generations of XMC serial flash memories where Status Register-1&2 can be written with a single “Write Status Register-1 (01h)” command. To complete the Write Status Register-1&2 instructions, the /CS pin must be driven high after the sixteenth bit of data from the lock input as shown in Figure 9-8 & Figure 9-9. If /CS is driven high after the eighth clock, the Write Status Register-1 (01h) instruction will only program the Status Register-1 without affecting the Status Register-2

Figure 9-8 Write Status Register-1/2 Instruction (SPI Mode)

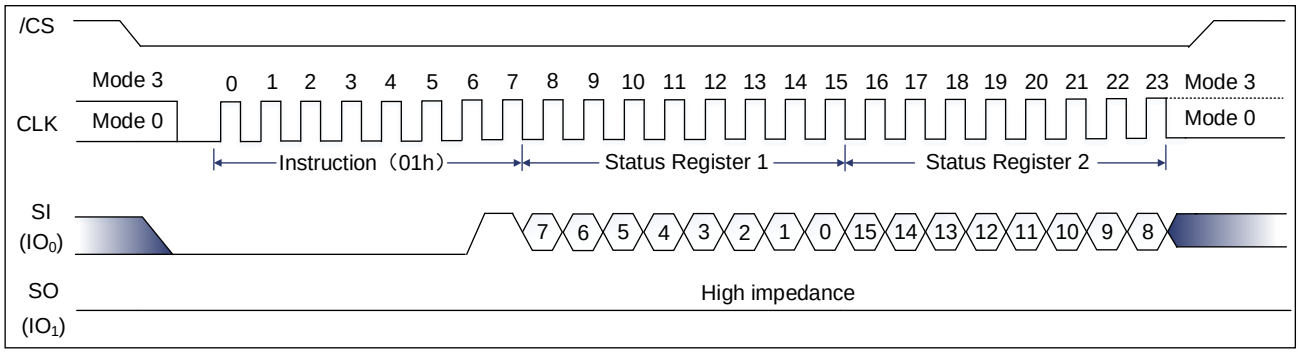
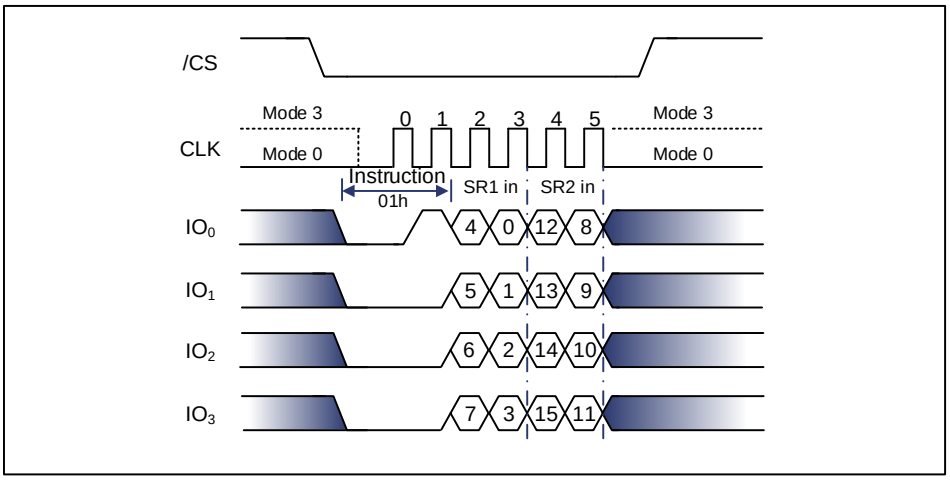


Figure 9-9 Write Status Register-1/2 Instruction (QPI Mode)



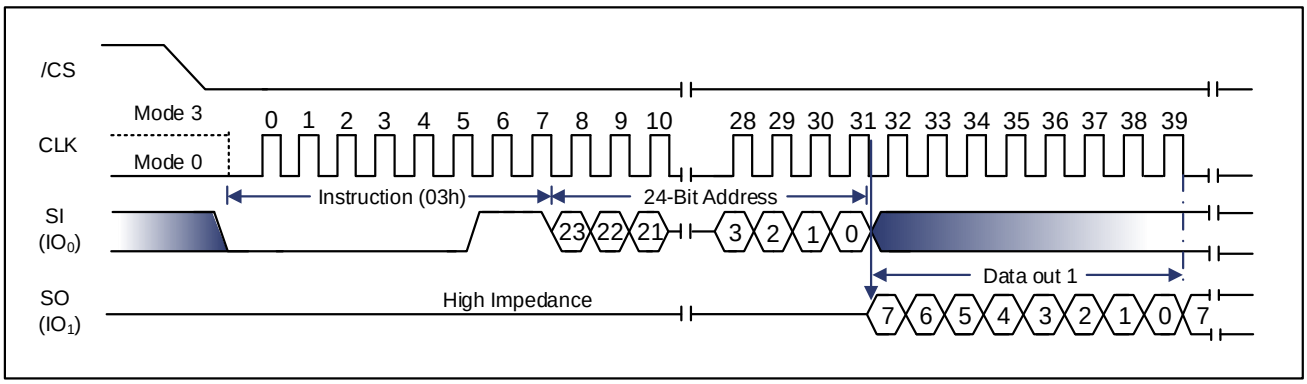
9.2.6 Read Data (03h)

The Read Data instruction enables one or more consecutive data Bytes to be read from memory. The sequence of Read Data instruction is demonstrated in Figure 9-10. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” and the 24-bit address (A23-A0) to the SI pin. The code and address bits are latched at the rising edge of the CLK pin. Subsequent to receipt of the address, the data Byte of the addressed memory location will be shifted out of the SO pin first with the most significant bit (MSB) on the falling edge of CLK. After each Byte of data has been shifted out, the address is automatically incremented to the next higher address, resulting in a continuous flow of data. This means that the entire memory can be accessed with a single instruction as long as the clock remains active. Ultimately, the instruction is done by driving /CS high.

If a Read Data instruction is sent in the middle of an Erase, Program or Write cycle (BUSY=1), the instruction is ignored and has no effect on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (as indicated by the Electrical Characteristics of AC).

The Read Data (03h) instruction is only supported in Standard SPI mode.

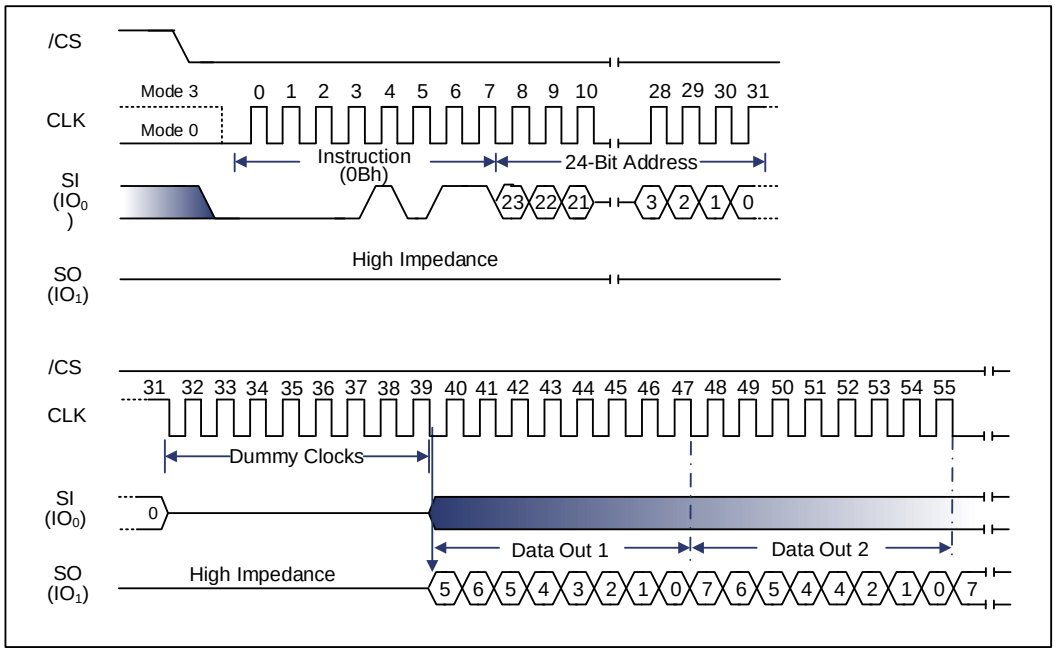
Figure 9-10 Read Data Instruction (SPI Mode only)



9.2.7 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction, except that it can operate at the highest possible frequency of F_C (as indicated by the Electrical Characteristics of AC). This is achieved by adding eight "dummy" clocks after the 24-bit address, as shown in Figure 9-11. These dummy clocks provide the devices internal circuits with extra time to set the initial address. During the dummy clocks, the data value on the SO pin is a "do not care".

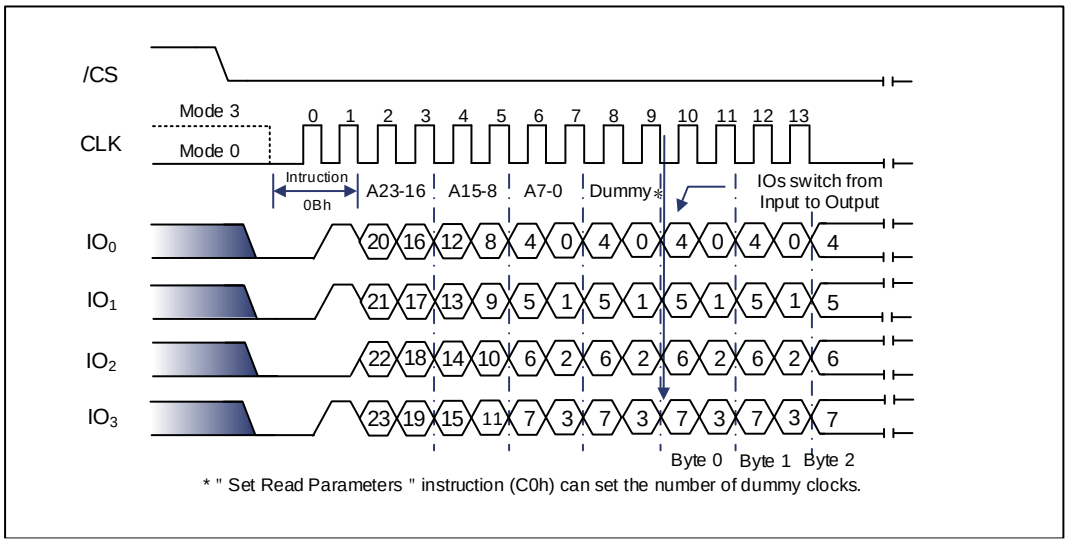
Figure 9-11 Fast Read Instruction (SPI Mode)



Fast Read (0Bh) in QPI Mode

The Fast Read instruction is also supported in QPI mode. When QPI mode is activated, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" instruction to suit a broad spectrum of applications with different requirements for maximum Fast Read frequency or minimum data access latency. It is possible to configure the number of dummy clocks to be 2, 4, 6 or 8 as per the setting of the Read Parameters bits P [5:4]. The default number of dummy clocks is 2 upon power up or after a Reset instruction.

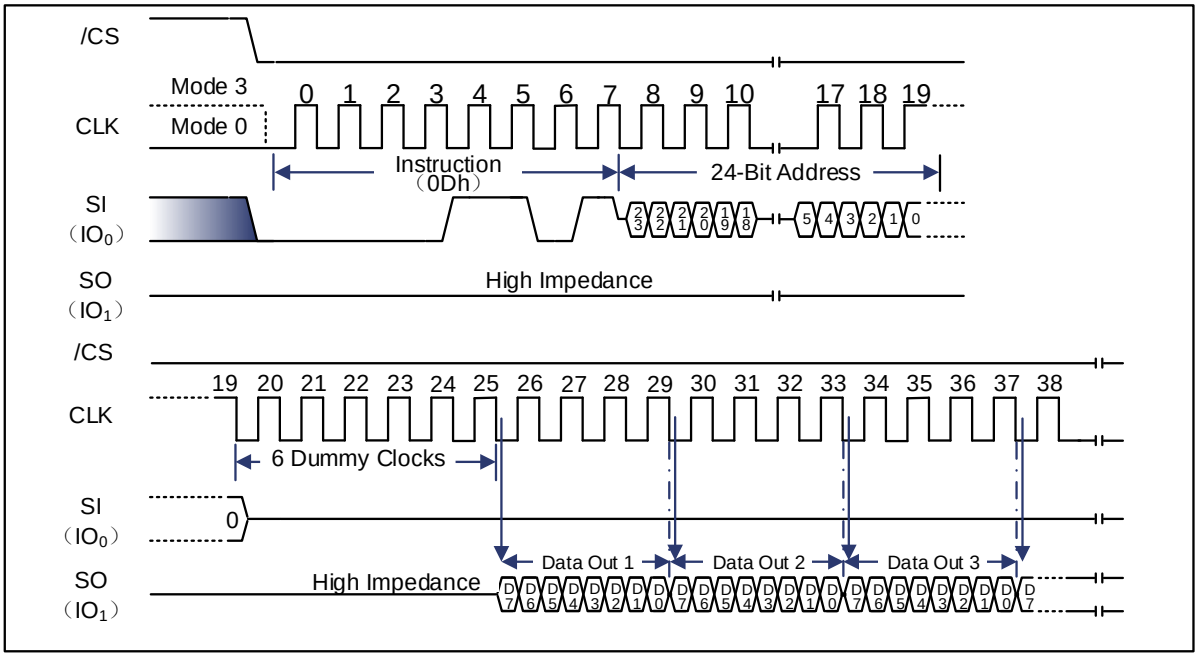
Figure 9-12 Fast Read Instruction (QPI Mode)



9.2.8 DTR Fast Read (0Dh)

The DTR Fast Read instruction is similar to the Fast Read instruction, except that the 24-bit address input and data output involves a DTR (Double Transfer Rate) operation. This is achieved by adding 6 “dummy” clocks after the 24-bit address, as shown in Figure 9-13. The dummy clocks provide additional time for the device's internal circuitry to set the initial address. During the dummy clocks the data value on the SO pin is a “do not care”.

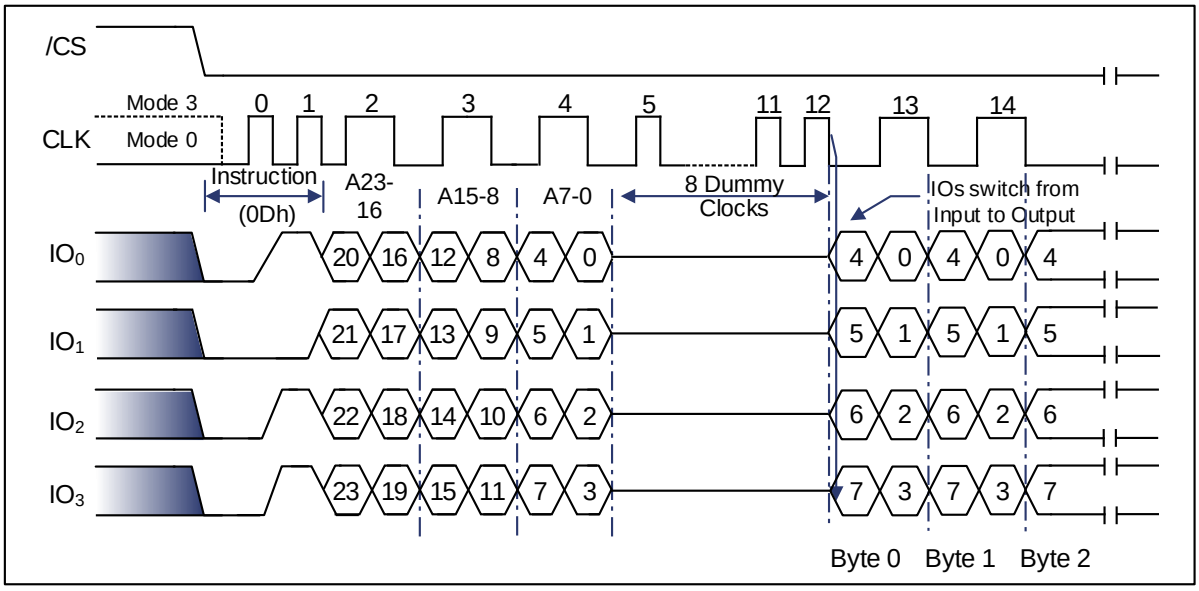
Figure 9-13 DTR Fast Read Instruction (SPI Mode)



DTR Fast Read (0Dh) in QPI Mode

The DTR Fast Read instruction is also supported in QPI mode.

Figure 9-14 DTR Fast Read Instruction (QPI Mode)

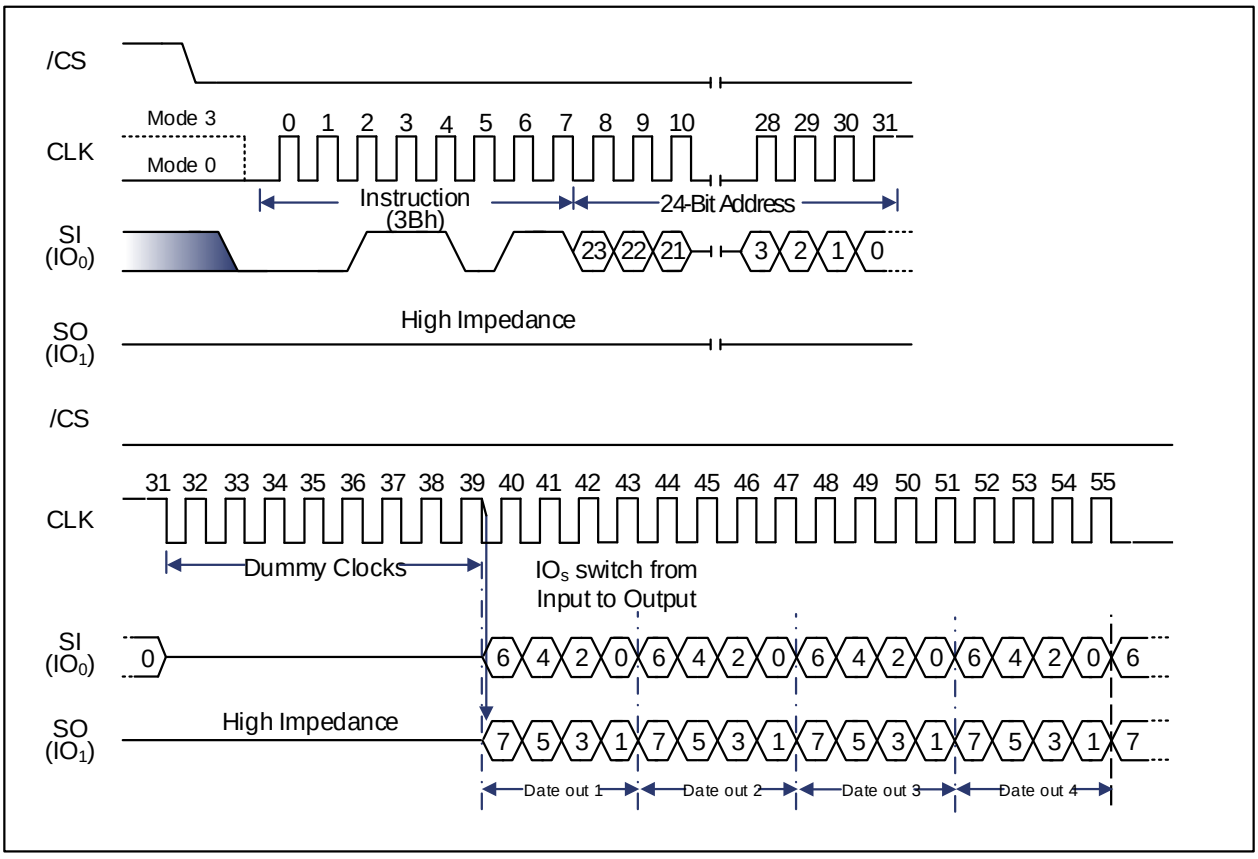


9.2.9 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction works similarly as the standard Fast Read (0Bh) instruction except that data is output on two pins, namely, IO_0 and IO_1. It allows data to be transferred twice as fast as the standard SPI devices. The Fast Read Dual Output instruction is an ideal choice for fast downloading of the code from Flash to RAM at power-up or for applications where code segments are cached into RAM for execution.

Similar to the Fast Read instruction, as indicated by the Electrical Characteristics of AC, the Fast Read Dual Output instruction can operate at the highest possible frequency of F_C. As demonstrated in Figure 9-15, the additional dummy clocks provide the device's internal circuits with extra time to set the initial address. The input data during the dummy clocks is “do not care”. However, the IO_0 pin should be high-impedance until the falling edge of the first data out clock.

Figure 9-15 Fast Read Dual Output Instruction (SPI Mode only)

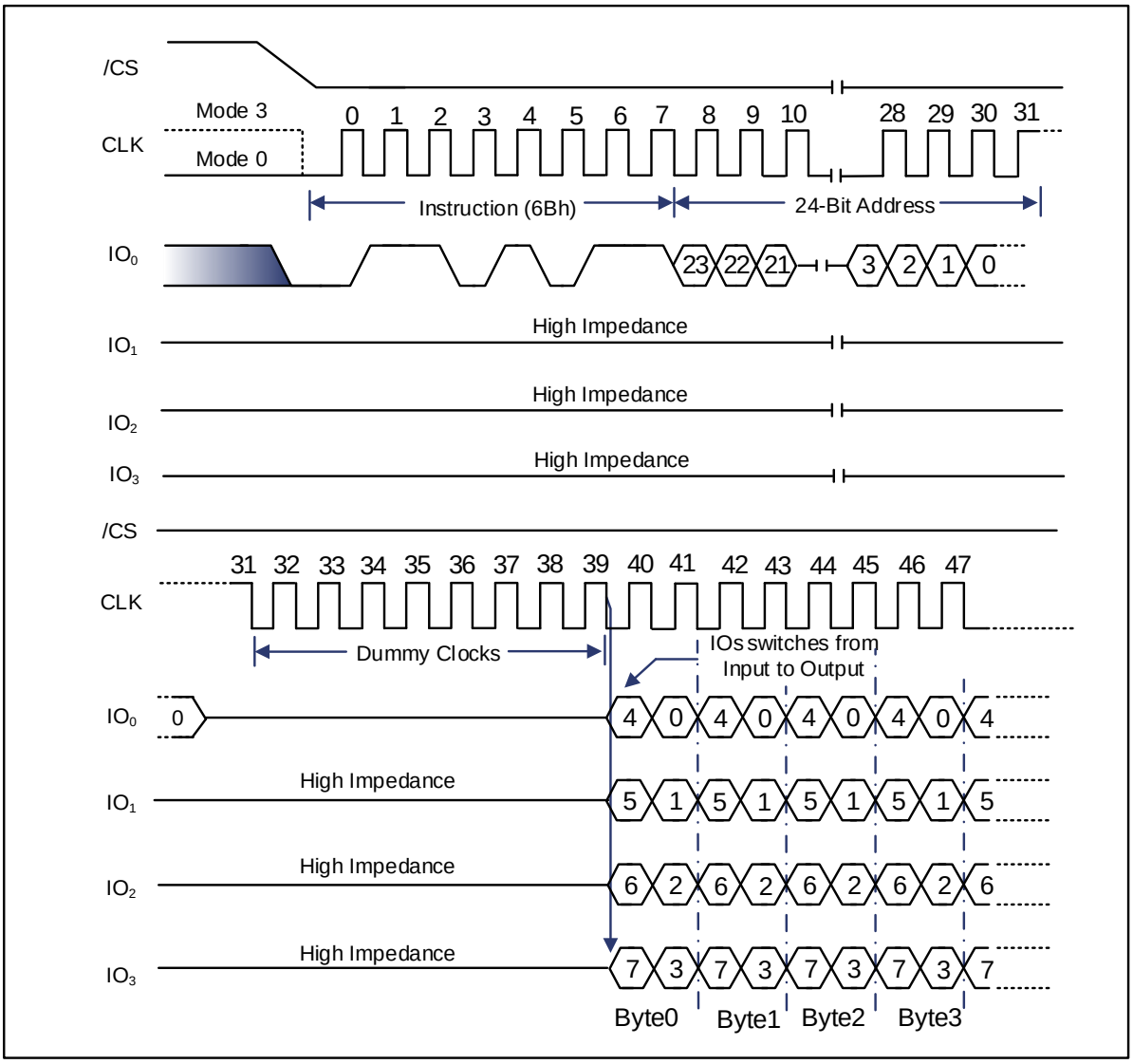


9.2.10 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, that is, IO_0, IO_1, IO_2, and IO_3. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device can receive a Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

As indicated by the Electrical Characteristics of AC, the Fast Read Quad Output instruction can operate at the highest possible frequency of fc. This is achieved by adding eight “dummy” clocks(default) after the 24-bit address, as shown in Figure 9-16. The dummy clocks provide the device's internal circuits with extra time to set the initial address. The input data during the dummy clocks is “do not care”. However, the IO pins should be high-impedance until the falling edge of the first data out clock.

Figure 9-16 Fast Read Quad Output Instruction (SPI Mode only)



9.2.11 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction enables improved random access while maintaining two IO pins, namely, IO_0 and IO_1. It works similarly as the Fast Read Dual Output (3Bh) instruction but it is able to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code (XIP) to be executed directly from the Dual SPI in certain applications.

Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input of Address bits (A23-0), as shown in

Figure 9-17. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction by including or excluding the first Byte of instruction code. The M3-0 bits are "do not care" ("x"). However, the IO pins should be high-impedance until the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1, 0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not involve a BBh instruction code. This reduces the instruction sequence by eight clocks and allows the Read address to be accessed immediately after /CS is asserted low, as shown in Figure 9-18.

If the "Continuous Read Mode" bits M5-4 ≠ (1, 0), the next instruction (after /CS is raised and then lowered) requires the first Byte instruction code, so that it returns to normal operation. It is recommended that FFFFh be entered on IO_0 as the next instruction (16 clocks) to ensure that M4 = 1 and the device return to normal operation.

Figure 9-17 Fast Read Dual I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode only)

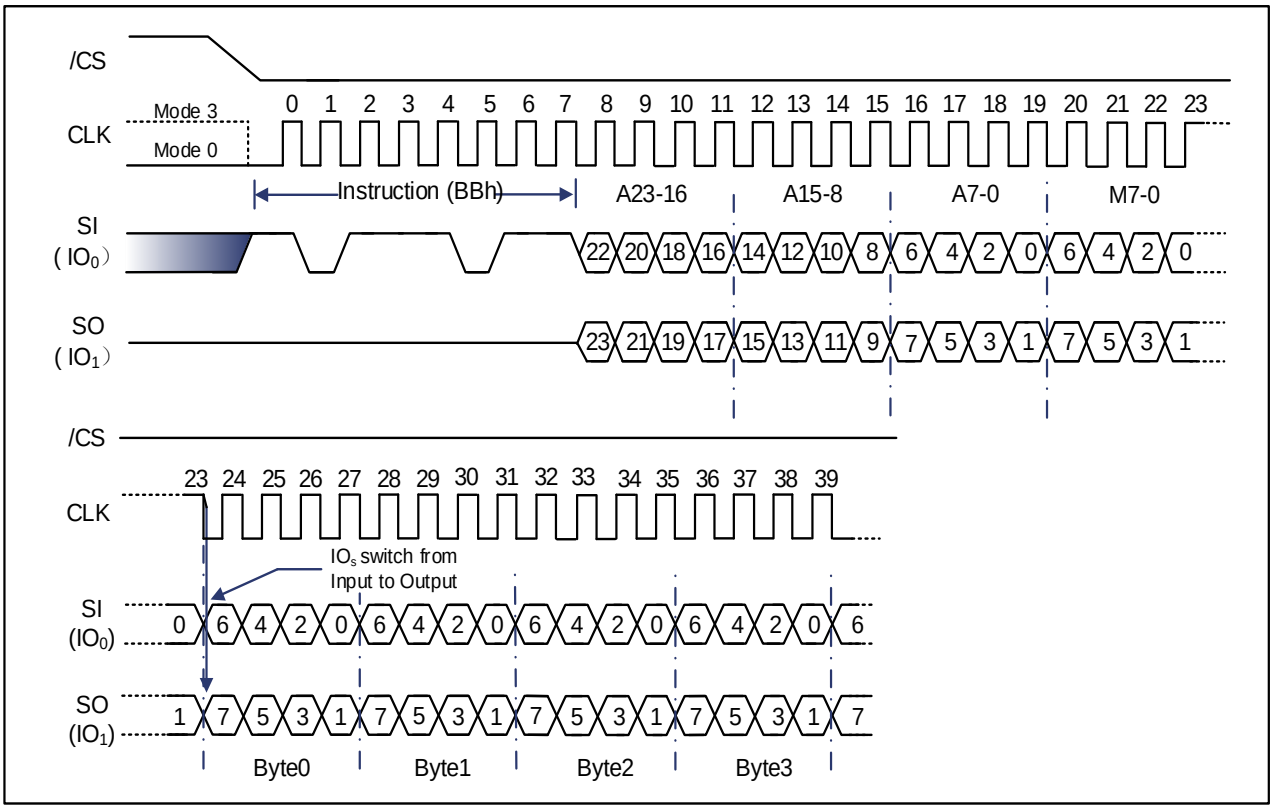
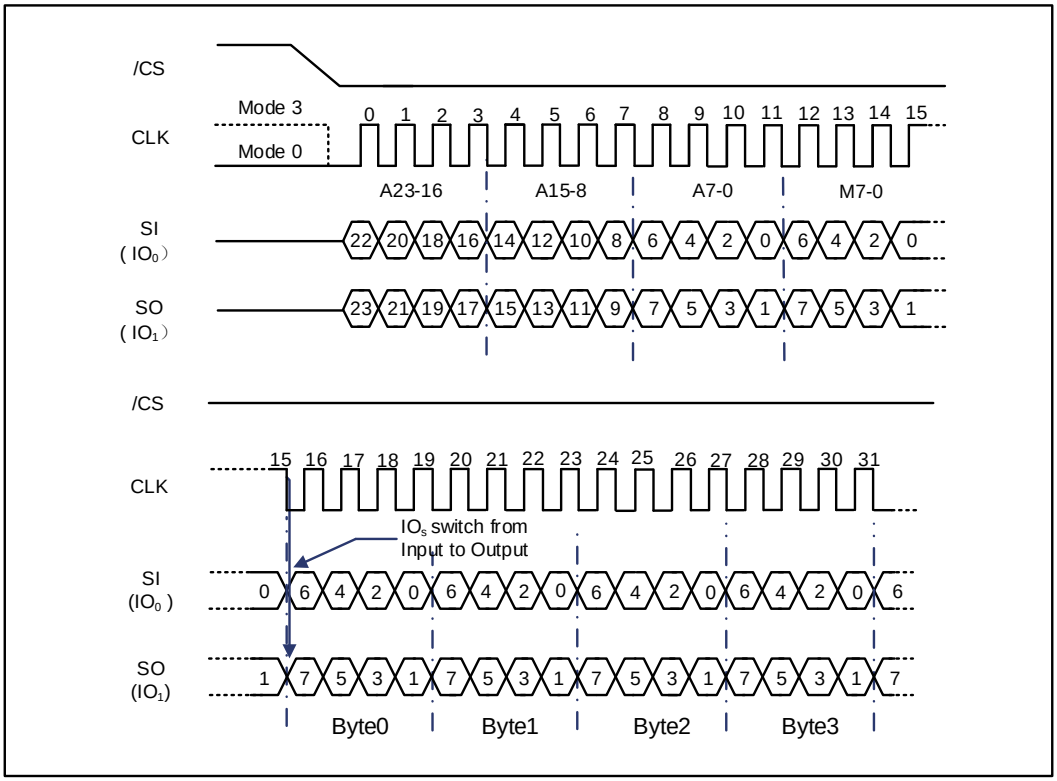


Figure 9-18 Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)



9.2.12 DTR Fast Read Dual I/O (BDh)

The DTR Fast Read Dual I/O (BDh) instruction enables improved random access while maintaining two IO pins, that is, IO_0 and IO_1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the of Address bits (A23-0) two bits in each clock. This reduced instruction overhead may allow for code (XIP) to be executed directly from the Dual SPI in some applications.

DTR Fast Read Dual I/O with "Continuous Read Mode"

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input of Address bits (A23-0), as shown in Figure 9-19. The M5-4 bits control the length of the next Fast Read Dual I/O instruction by including or excluding the first Byte instruction code. The M3-0 bits are "do not care" ("x"). However, the IO pins should be high-impedance until the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not involve the BDh instruction code, as shown in

Figure 9-20. This reduces the instruction sequence by eight clocks and allows access to the Read address immediately after /CS is asserted low.

If the "Continuous Read Mode" bits M5-4 ≠ (1,0), the next instruction (after /CS is raised and then lowered) requires the first Byte instruction code, so that it returns to normal operation. It is recommended that FFFFh/FFFFFh be entered on IO_0 as the next instruction (16/20 clocks) to ensure that M4 = 1 and the device return to normal operation.

Figure 9-19 DTR Fast Read Dual I/O (Initial instruction or previous M5-4≠10, SPI Mode only)

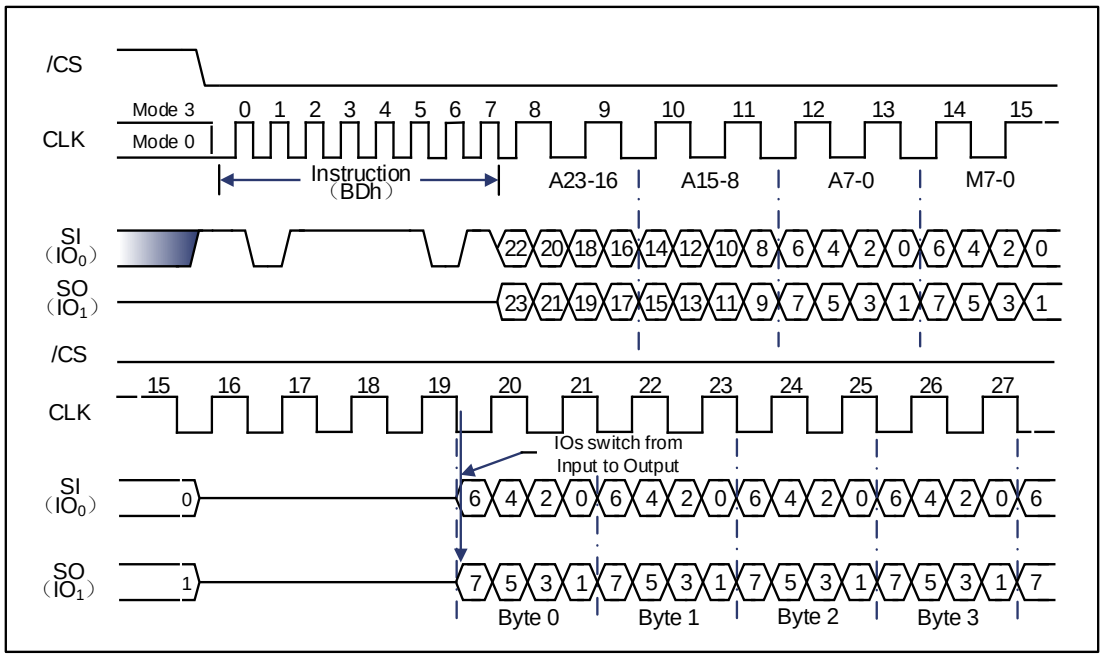
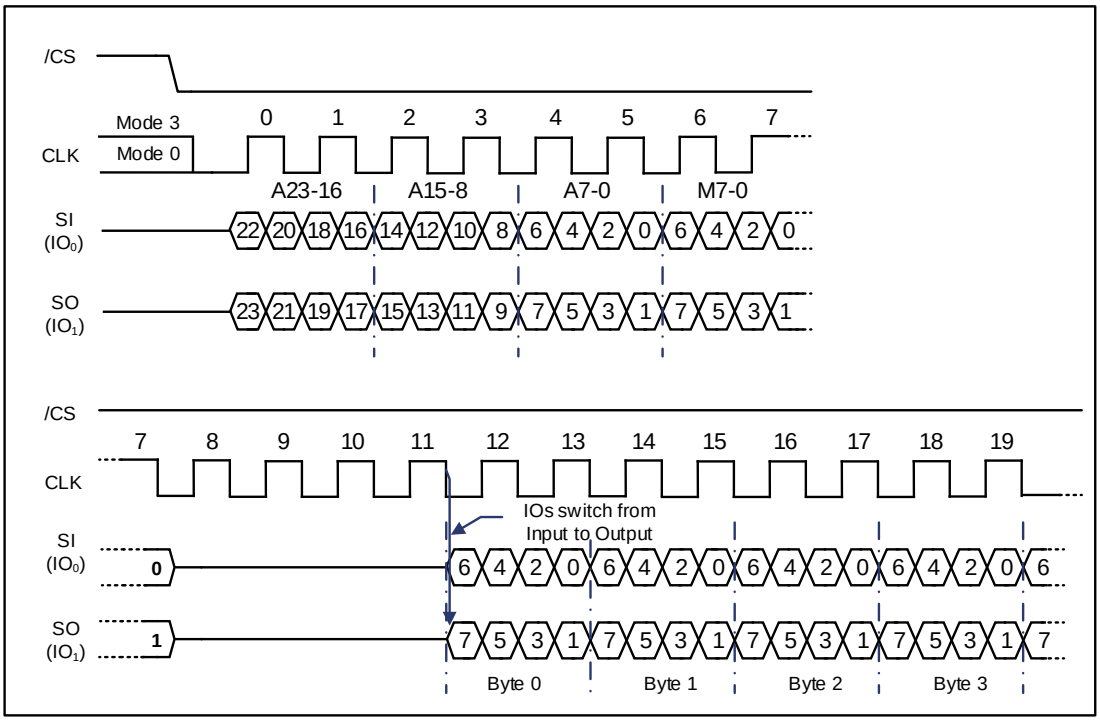


Figure 9-20 DTR Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode only)



9.2.13 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction works similarly as the Fast Read Dual I/O (BBh) instruction, except that address and data bits are input and output via four pins, namely, IO_0, IO_1, IO_2 and IO_3 and four Dummy clocks are required in SPI mode before the data is output. The Quad I/O dramatically reduces instruction overhead and allows faster random access to execute code (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

Fast Read Quad I/O with "Continuous Read Mode"

As demonstrated in Figure 9-21, the Fast Read Quad I/O instruction can further reduce instruction overhead via setting of the "Continuous Read Mode" bits (M7-0) after the input of Address bits (A23-0). The M5-4 bits control the length of the next Fast Read Quad I/O instruction by including or excluding the first Byte instruction code. The M3-0 bits are "do not care" ("x"). However, the IO pins should be high-impedance until the falling edge of the first data out clock.

When the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not involve the EBh instruction code, as shown in

Figure 9-22. This reduces the instruction sequence by eight clocks and allows the Read address to be accessed immediately after /CS is asserted low.

When the "Continuous Read Mode" bits M5-4 ≠ (1,0), the next instruction (after /CS is raised and then lowered) requires the first Byte instruction code, so that it returns to normal operation. It is recommended that FFh be entered on IO_0 for the next instruction (8 clocks) to ensure that M4 = 1 and the device return to normal operation.

Figure 9-21 Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode)

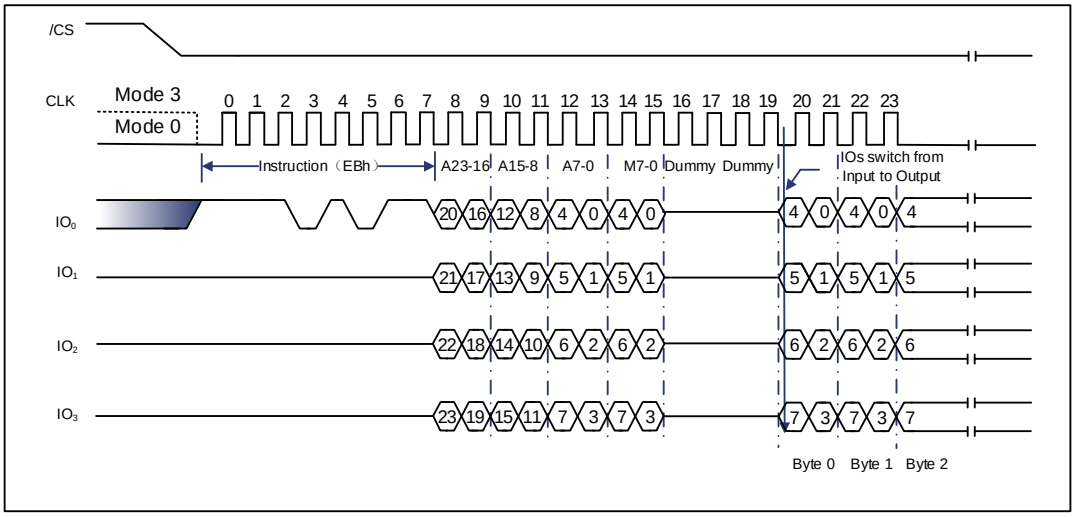
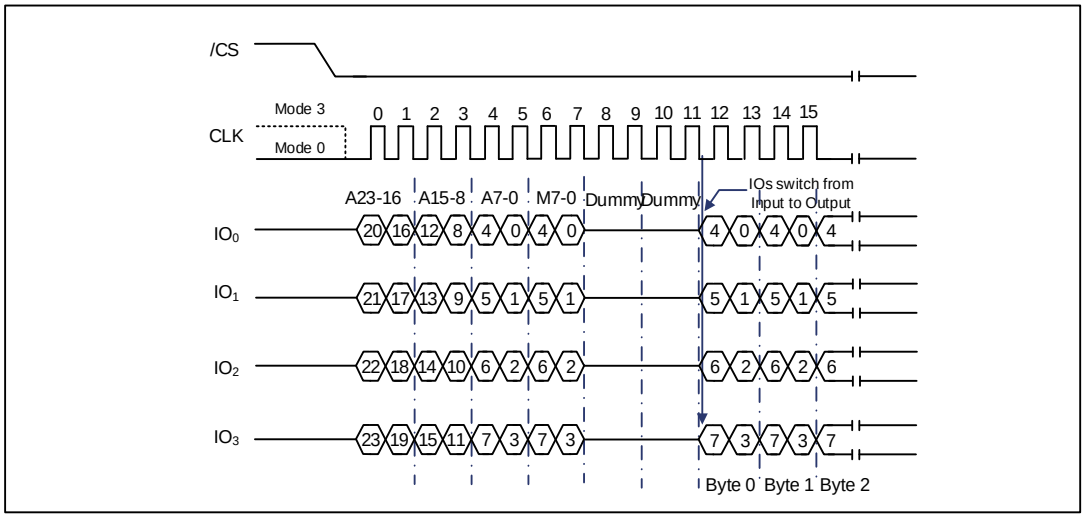


Figure 9-22 Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode)



Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

By issuing the "Set Burst with Wrap" (77h) command prior to EBh the Fast Read Quad I/O instruction can also be applied to access a specific portion within a page. The "Set Burst with Wrap" (77h) command can enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-Byte section of a 256-Byte page. The output data starts at the initial address specified in the instruction, and once the end boundary of the 8/16/32/64-Byte section is reached, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications using the cache to quickly fetch a critical address and then populate the cache afterwards within a fixed length (8/16/32/64-Byte) of data without the need to issue multiple read commands. The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4, to be set. The W4 bit is adopted to enable or disable the "Wrap Around" operation, while W6-5 bits are applied to specify the length of the wrap around section within a page.

9.2.14 DTR Fast Read Quad I/O (EDh)

The DTR Fast Read Quad I/O (EDh) instruction works similarly as the Fast Read Dual I/O (BBh) instruction, except that address and data bits are input and output via four pins IO_0, IO_1, IO_2 and IO_3, which requires four Dummy clocks in SPI mode before the data is output. The Quad I/O dramatically reduces instruction overhead and allows faster random access to execute code (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

DTR Fast Read Quad I/O with "Continuous Read Mode"

As shown in Figure 9-23, the Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input of Address bits (A23 -0). The M5-4 bits control the length of the next Fast Read Quad I/O instruction by including or excluding the first Byte instruction code. The M3-0 bits are "do not care" ("x").

However, the IO pins should be high-impedance until the falling edge of the first data out clock. As can be seen in Figure 9-24, when the "Read Command Bypass Mode" bits M5-4 = (1,0), the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not involve the EDh instruction code. This reduces the instruction sequence by eight clocks and allows the Read address to be accessed immediately after /CS is asserted low.

When the "Read Command Bypass Mode" bits M5-4 ≠ (1,0), the next instruction (after /CS is raised and then lowered) requires the first Byte instruction code, so that it returns to normal operation. It is recommended that FFh/3FFh be entered on IO_0 for the next instruction (8/10 clocks) to ensure M4 = 1 and the device return to normal operation.

Figure 9-23 DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, SPI Mode)

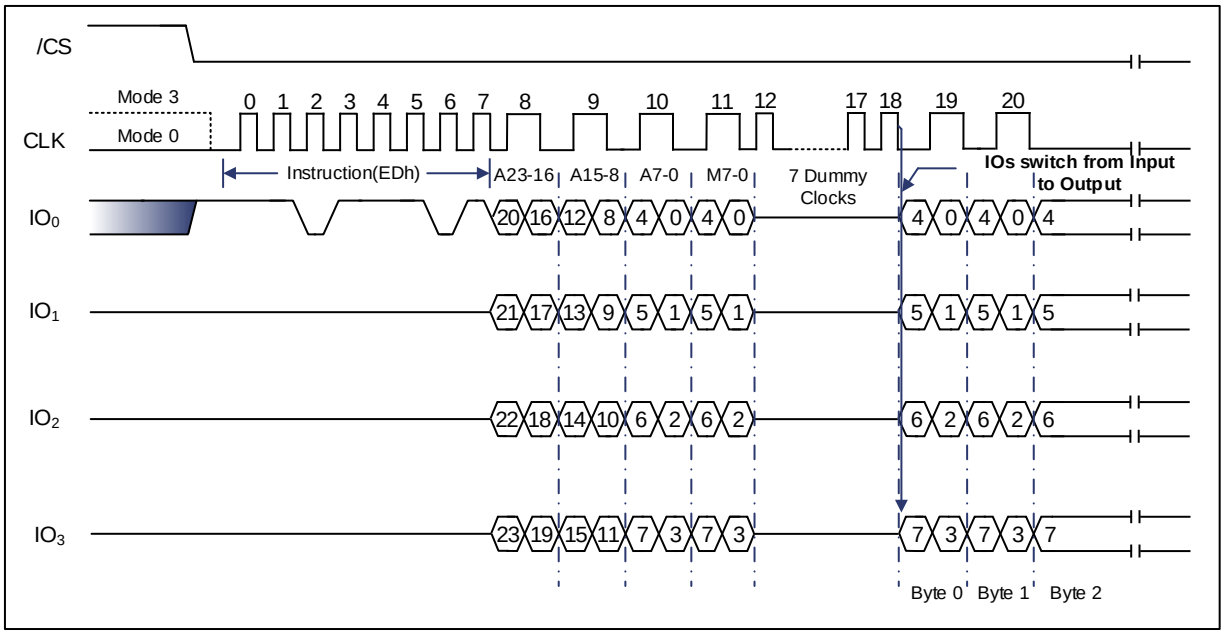
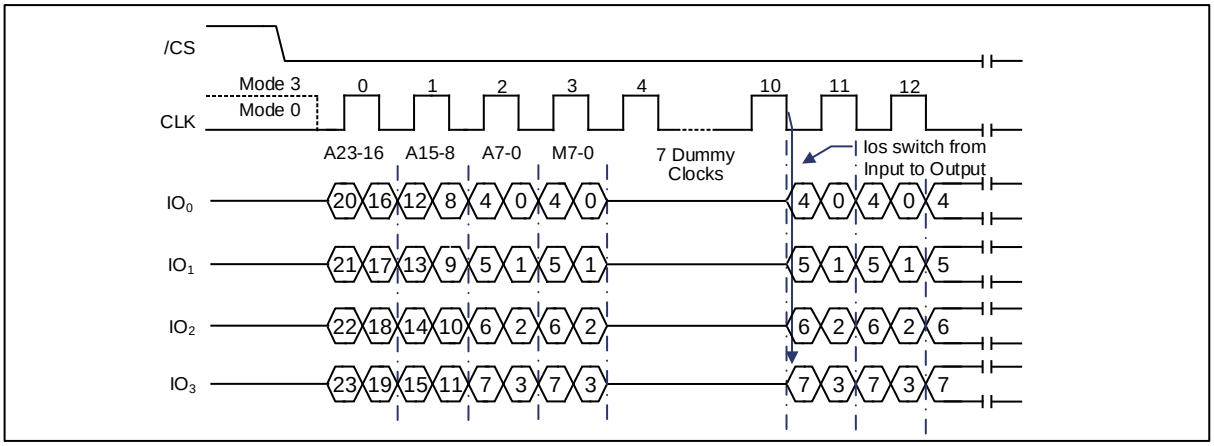


Figure 9-24 Fast Read Quad I/O (Previous instruction set M5-4=10, SPI Mode)



DTR Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

By issuing a "Set Burst with Wrap" (77h) command prior to EDh, the Fast Read Quad I/O instruction (EDh) can also be applied to access a specific portion within a page. The "Set Burst with Wrap" (77h) command can enable or disable the "Wrap Around" feature for the following EDh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-Byte section of a 256-Byte page.

The output data starts at the initial address specified in the instruction and once the end boundary of the 8/16/32/64 Byte section is reached, the output will wrap around to the beginning boundary automatically until /CS is pulled up to terminate the command.

The Burst with Wrap feature enables applications using cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-Byte) of data without issuing multiple read commands.

Three "Wrap Bits", W6-4 can be set by the "Set Burst with Wrap" instruction. The W4 bit is adopted to enable or disable the "Wrap Around" operation while W6-5 bits are used to determine the length of the wrap around section within a page. Section 9.2.16 can be referred to for detailed descriptions.

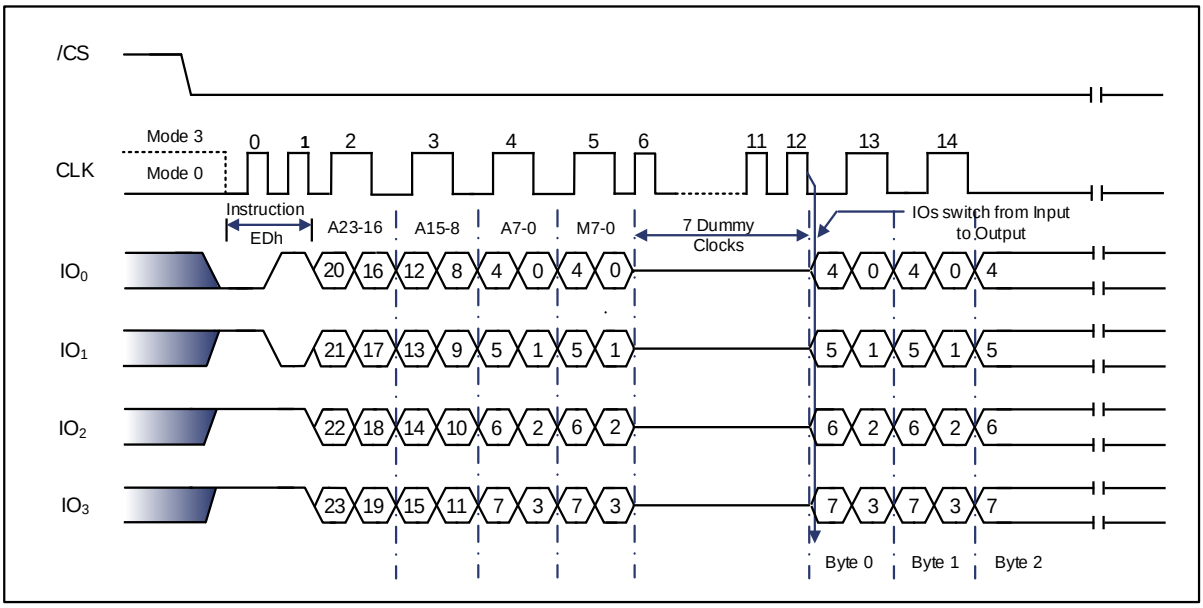
DTR Fast Read Quad I/O (EDh) in QPI Mode

As demonstrated in Figure 9-25, the DTR Fast Read Quad I/O instruction is also supported in QPI mode where the “Read Command Bypass Mode” bits M7-0 are also treated as dummy clocks. In the default setting, the data output will follow the Read Command Bypass Mode bits immediately.

In QPI mode, the “Read Command Bypass Mode” feature is also available for Fast Read Quad I/O instruction, as can be seen in the descriptions from previous pages.

In QPI mode, the “Wrap Around” feature is not available for Fast Read Quad I/O instruction. To perform a wrap-around read operation with a fixed data length in QPI mode, a dedicated “DTR Burst Read with Wrap” (0Eh) instruction must be adopted, and the detailed information is revealed in Section 9.2.38.

Figure 9-25 DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, QPI Mode)



Fast Read Quad I/O (EBh) in QPI Mode

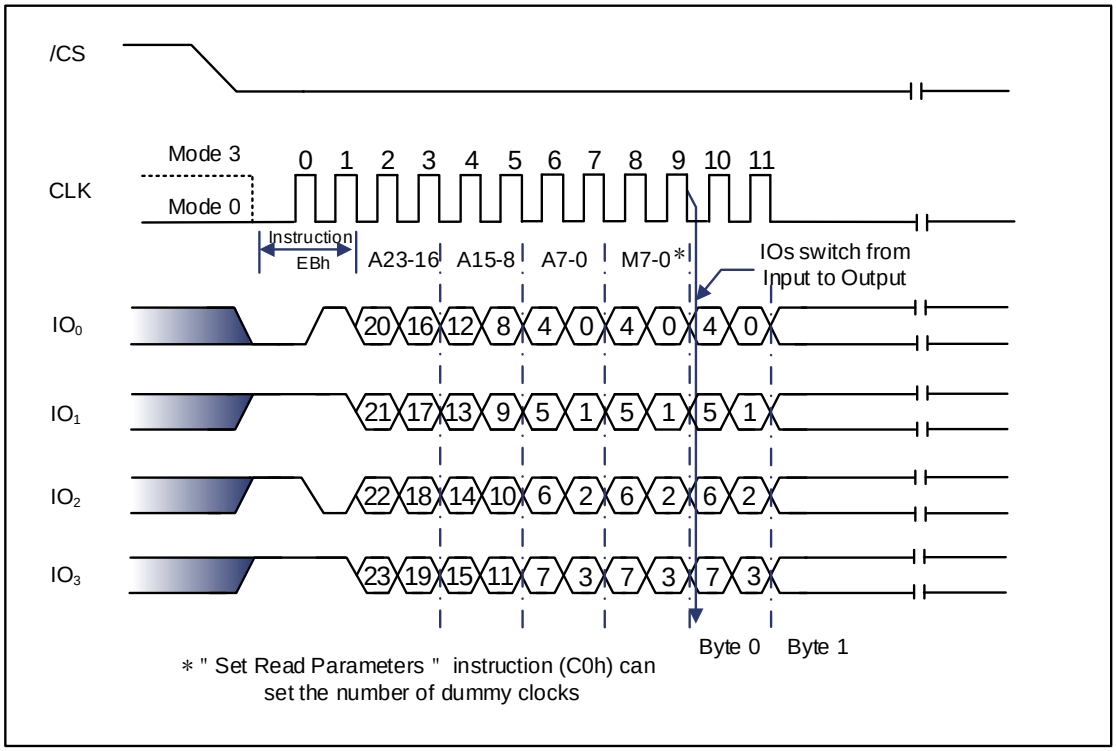
As indicated in Figure 9-26, the Fast Read Quad I/O instruction is also available in QPI mode,. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different requirements for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as 2, 4, 6 or 8. The default number of dummy clocks at power up or after the Reset instruction is 2.

In QPI mode, the “Continuous Read Mode” bits M7-0 are also considered to be dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

In QPI mode, the “Continuous Read Mode” feature is also available for Fast Read Quad I/O instruction, as can be seen in the descriptions from previous pages.

The “Wrap Around” feature is not available for Fast Read Quad I/O instruction in QPI mode. To perform a wrap-around read operation with fixed data length in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) instruction must be adopted.

Figure 9-26 Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, QPI Mode)



9.2.15 Word Read Quad I/O (E7h)

Except that the lowest Address bit (A0) must be equal to 0 and only two Dummy clocks are needed before the data is output, the Word Read Quad I/O (E7h) instruction functions similarly as the Fast Read Quad I/O (EBh) instruction. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O Instruction.

Word Read Quad I/O with "Continuous Read Mode"

As shown in Figure 9-27, the Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0). The bits of M5-4 control the length of the next Fast Read Quad I/O instruction by including or excluding the first Byte instruction code. The bits of the M3-0 are "do not care" ("x"). However, the IO pins should be high-impedance until the falling edge of the first data out clock.

As shown in Figure 9-28, when the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not involve the E7h instruction code,. This reduces the instruction sequence by eight clocks and allows the Read address to be entered immediately after /CS is asserted low.

When the "Continuous Read Mode" bits M5-4 ≠ (1,0), the next instruction (after /CS is raised and then lowered) requires the first Byte instruction code, so that it returns to normal operation. It is recommended that FFh be entered on IO_0 for the next instruction (8 clocks) to ensure M4 = 1 and the device return to normal operation.

Figure 9-27 Word Read Quad I/O Instruction (Initial instruction or previous M5-4≠10, SPI Mode only)

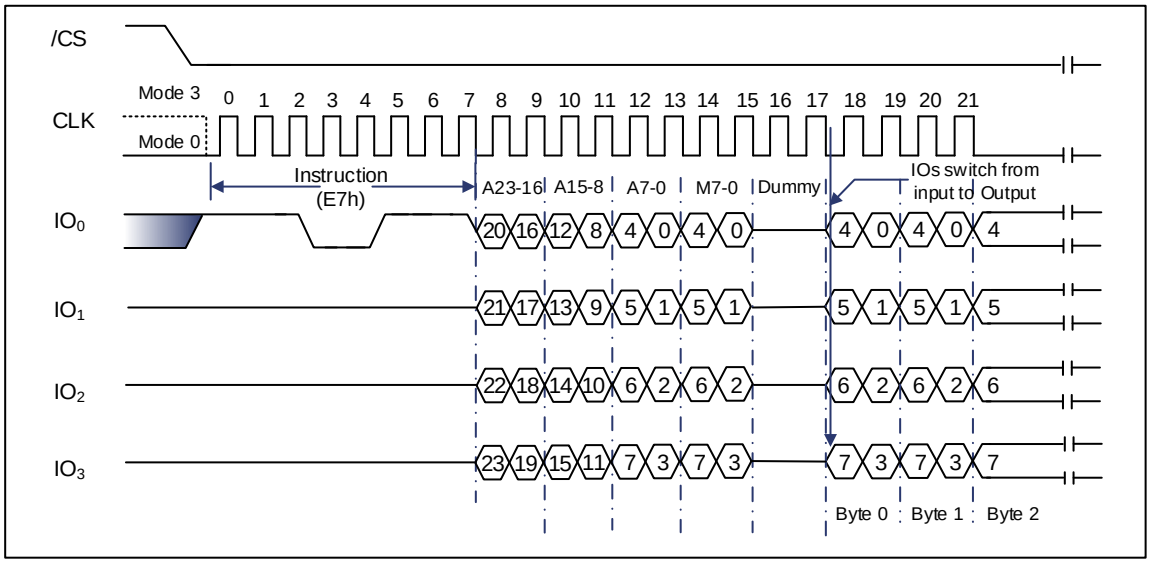
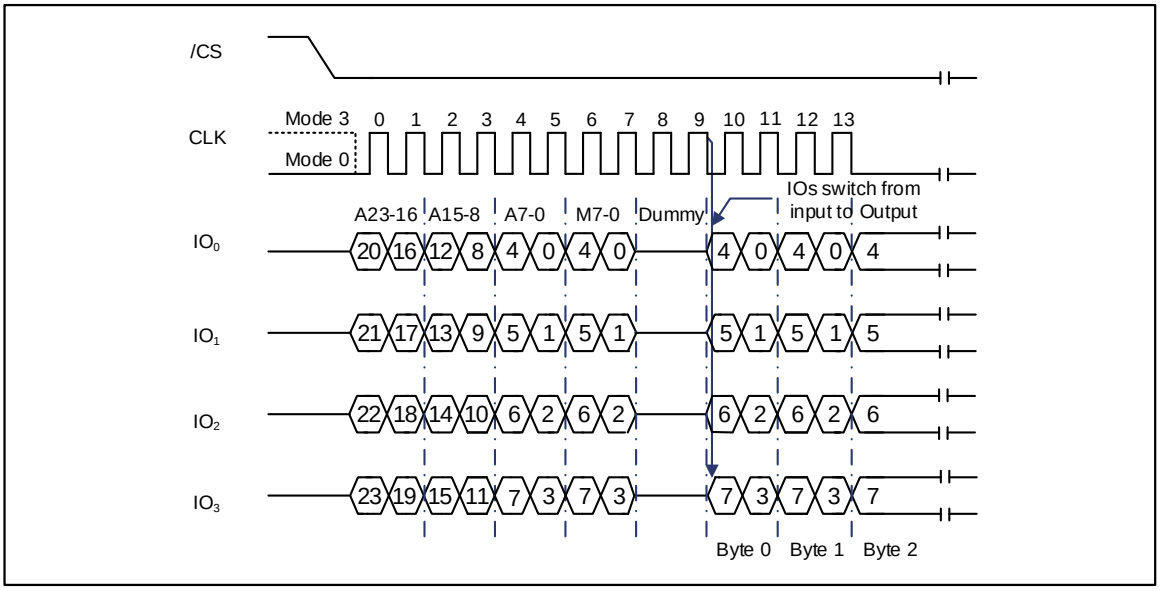


Figure 9-28 Word Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)



Word Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

By issuing the "Set Burst with Wrap" (77h) command before E7h, the Word Read Quad I/O instruction can also be applied to access a specific portion within a page. The "Set Burst with Wrap" (77h) instruction can enable or disable the "Wrap Around" feature for the following E7h commands. When "Wrap Around" is enabled, the data being accessed can be limited to 8, 16, 32 or 64-Byte section of a 256-Byte page. The output data starts at the initial address specified in the instruction and once the end boundary of the 8/16/32/64-Byte section is reached. the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications using cache to quickly fetch a critical address and then populate the cache afterwards within a fixed length (8/16/32/64-Byte) of data without the need to issue multiple read commands. The "Set Burst with Wrap" instruction allows the three "Wrap Bits", W6-4, to be set. The W4 bit is adopted to enable or disable the "Wrap Around" operation while W6-5 bits are applied to determine the length of the wrap around section within a page.

9.2.16 Set Burst with Wrap (77h)

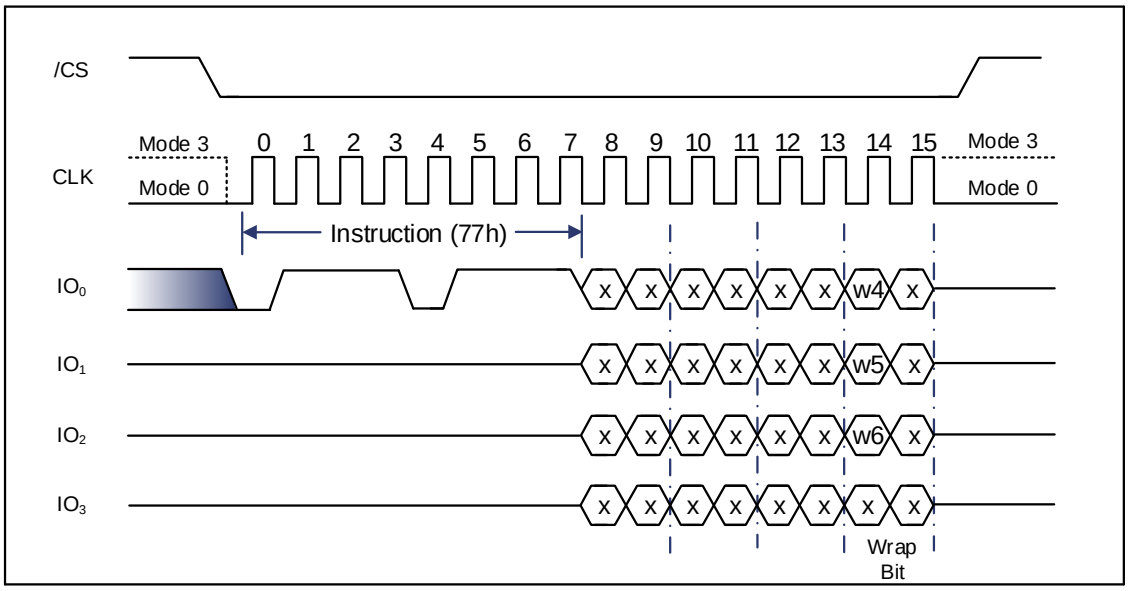
The Set Burst with Wrap (77h) instruction is taken in conjunction with “Fast Read Quad I/O” and “Word Read Quad I/O” instructions in Standard SPI mode to access a fixed length of 8/16/32/64-Byte section within a 256-Byte page. This feature can be of benefit to several applications and improves the execution performance of the entire system code.

As shown in Figure 9-29, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code “77h” followed by 24 dummy bits and the 8 “Wrap Bits”, namely, W7-0 which is similar to the Quad I/O instruction. The Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-Byte	No	N/A
0 1	Yes	16-Byte	No	N/A
1 0	Yes	32-Byte	No	N/A
1 1	Yes	64-Byte	No	N/A

Once the Set Burst with Wrap instruction is applied to set the W6-4 bits, all subsequent “Fast Read Quad I/O” and “Word Read Quad I/O” instructions will access the 8/16/32/64 Byte portion of any page using the W6-4 setting. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 is 1 at power on or after a software/hardware reset.

Figure 9-29 Set Burst with Wrap Instruction (SPI Mode only)



9.2.17 Page Program (02h)

The page program instruction can program the data from one Byte to 256 Bytes at previously erased (FFh) memory locations. Before the device will accept the Page Program Instruction (Status Register bit WEL= 1), a Write Enable instruction must be executed. As revealed in Figure 9-30, this instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data Byte, into the SI pin. The /CS pin must be held low for the entire length of the instruction while data is sent to the device.

To program an entire 256-Byte page, the last address Byte (the least significant 8 address bits) should be set to 0. If the last address Byte is not 0, and the number of clocks exceeds the remaining page length, addressing will wrap around to the beginning of the page. In some cases, it is possible to program less than 256 Bytes (a partial page) without any effect on the other Bytes within the same page. A requirement for performing partial page programming is that the number of clocks does not exceed the remaining page length. If more than 256 Bytes are sent to the device, addressing will wrap around to the beginning of the page and overwrite the data previously sent.

Just like the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last Byte has been latched. If not, the Page Program instruction will not be executed. After /CS is driven high, a self-timed Page Program instruction will start to be executed for a duration of tPP (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may can still be accessed to check the status of the BUSY bit. The BUSY bit is 1 during the Page Program cycle and becomes 0 when the cycle is over and the device is ready to accept other instructions. At the end of the page programming cycle, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

Figure 9-30 Page Program Instruction (SPI Mode)

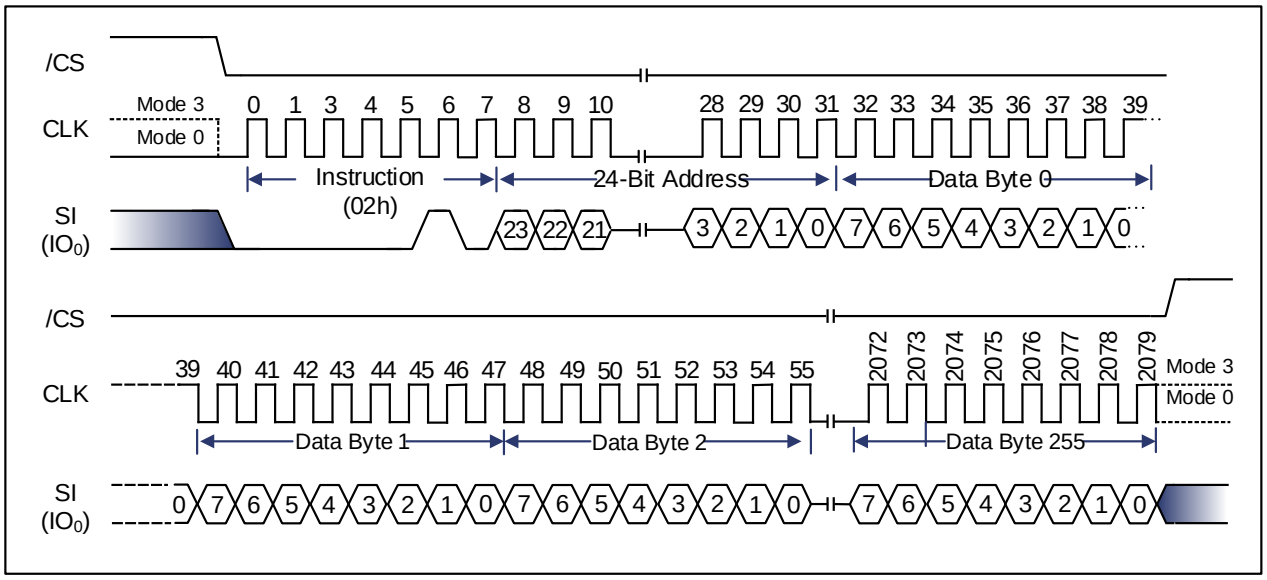
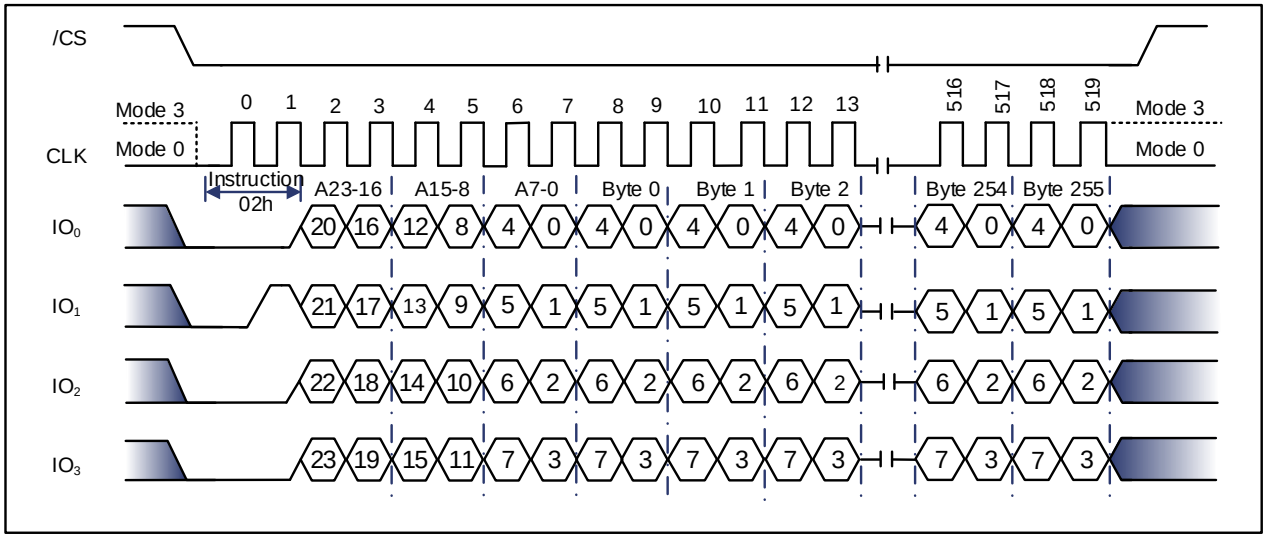


Figure 9-31 Page Program Instruction (QPI Mode)

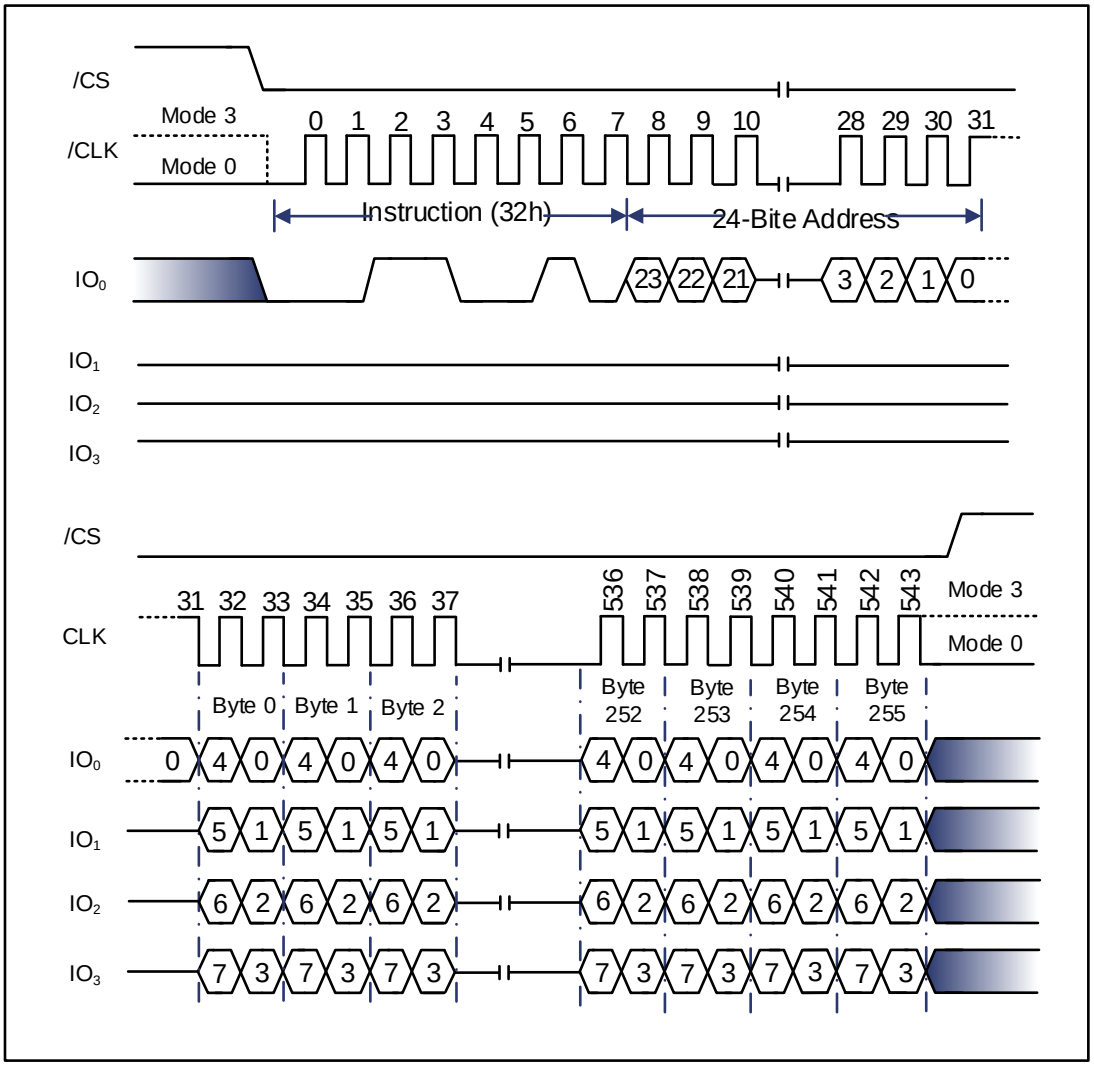


9.2.18 Quad Input Page Program (32h)

The instruction of Quad Input Page Program can program up to 256 Bytes of data in previously erased (FFh) memory locations using four pins, that is, IO_0, IO_1, IO_2, and IO_3. The instruction can improve performance for PROM Programmer and applications with clock speeds <5MHz. Systems with faster clock speed will not benefit from the Quad Input Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

The Quad Enable (QE) bit in Status Register-2 must be set to 1 to use Quad Input Page Program. And before the device accepts the Quad Input Page Program instruction (Status Register-1, WEL=1), A Write Enable instruction must be executed. As shown in Figure 9-32, it is initiated by driving the /CS pin low then shifting the instruction code “32h” followed by a 24-bit address (A23-A0) and at least one data Byte, into the IO pins. The /CS pin must be held low for the entire duration of the instruction while data is being sent to the device. All other functions of Quad Input Page Program have the same function as standard Page Program.

Figure 9-32 Quad Input Page Program Instruction (SPI Mode only)



9.2.19 Sector Erase (20h)

By accepting the Sector Erase instruction, all memory can be set within a specified sector (4K-Bytes) to an erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is activated by driving the /CS pin low and shifting the instruction code “20h” to the 24-bit sector address (A23-A0), demonstrated in Figure 9-33 and Figure 9-34.

After the eighth bit of the last Byte has been latched. the /CS pin must be driven high If not, the Sector Erase instruction will not be implemented. After /CS is driven high, the self-timed Sector Erase instruction will start to be executed for a duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction can still be accessed to check the status of the BUSY bit. The BUSY bit is 1 during the Sector Erase cycle and changes to 0 when the cycle is finished and the device is ready to accept other instructions. After the Sector Erase cycle ends and the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

Figure 9-33 Sector Erase Instruction (SPI Mode)

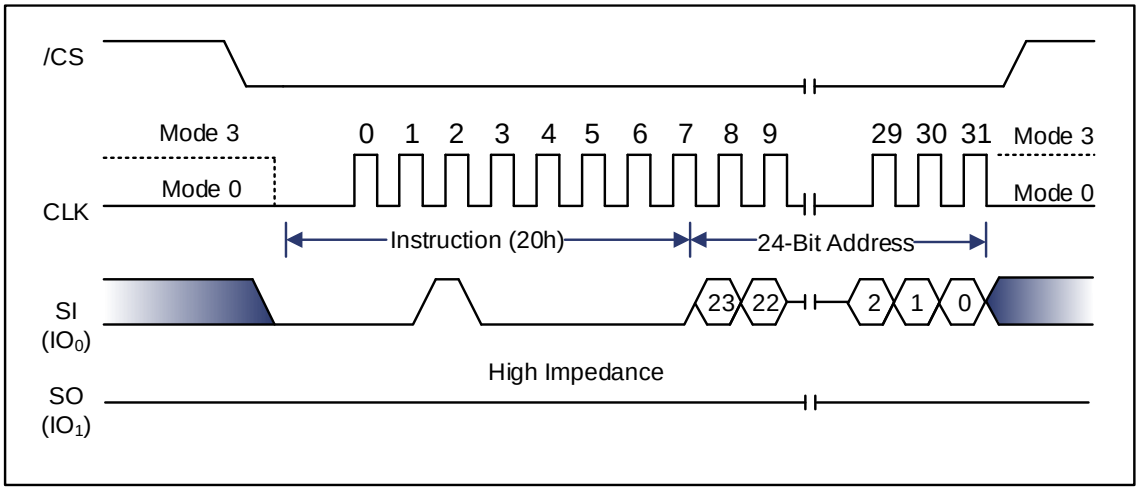
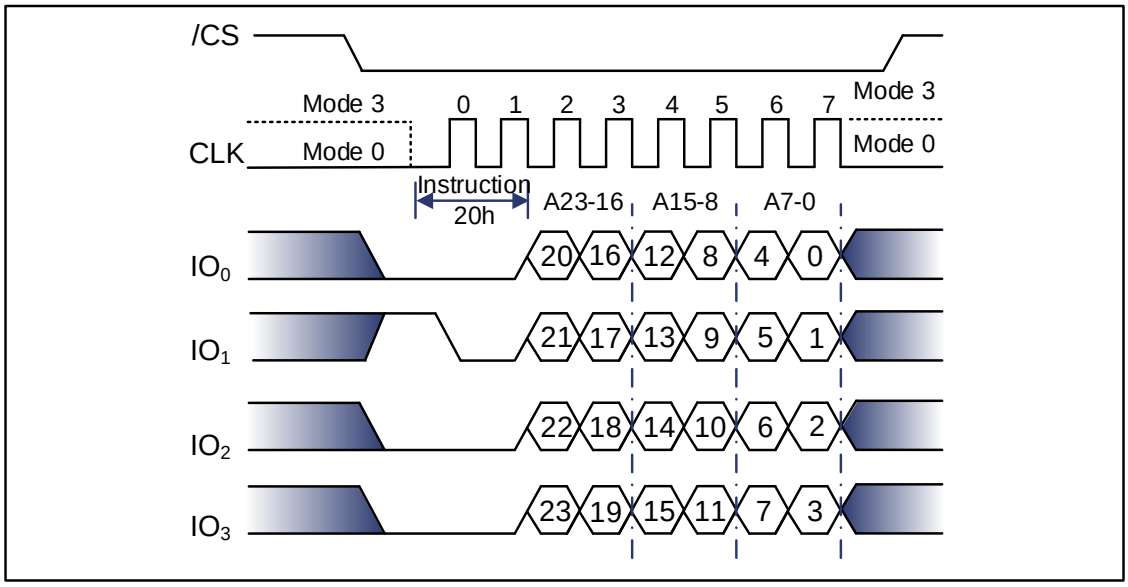


Figure 9-34 Sector Erase Instruction (QPI Mode)



9.2.20 32KB Block Erase (52h)

By accepting the Block Erase instruction, all memory can be set within a specified block (32K-Bytes) to an erased state of all 1s (FFh). A Write Enable instruction must be performed before the device can accept the Block Erase Instruction (Status Register bit WEL must be equal to 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” to the 24-bit block address (A23-A0), shown in Figure 9-35 & Figure 9-36.

After the eighth bit of the last Byte has been latched, the /CS pin must be driven high. If not, the Block Erase instruction will not be implemented. After /CS is driven high, the self-timed Block Erase instruction will start to be executed for a duration of t_{BE1} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction can still be accessed to check the status of the BUSY bit. The BUSY bit is 1 during the Block Erase cycle and turns to 0 when the cycle ends and the device is ready to accept other instructions. The Write Enable Latch (WEL) bit in the Status Register is cleared to 0 at the end of the Block Erase cycle. If the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits, the Block Erase instruction will not be executed.

Figure 9-35 32KB Block Erase Instruction (SPI Mode)

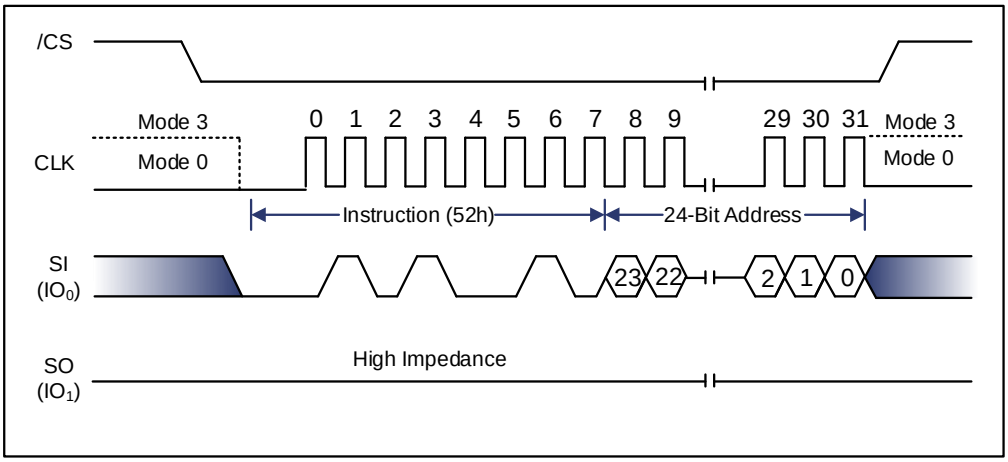
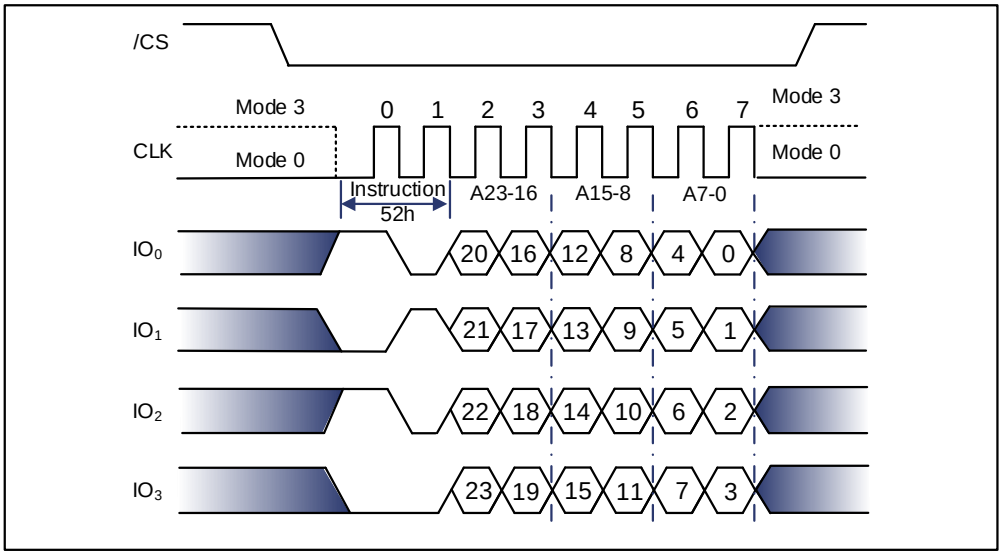


Figure 9-36 32KB Block Erase Instruction (QPI Mode)



9.2.21 64KB Block Erase (D8h)

By accepting theBlock Erase instruction, all memory can be set within a specified block (64K-Bytes) to an erased state of all 1s (FFh). A Write Enable instruction must be executed before the device can accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” to the 24-bit block address (A23-A0), demonstrated in Figure 9-37 and Figure 9-38. After the eighth bit of the last Byte has been latched, the /CS pin must be driven high. If not, the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will start to be executed for a duration of t_{BE} (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction can still be accessed to check the status of the BUSY bit. The BUSY bit is 1 during the Block Erase cycle and changes to 0 when the cycle ends and the device is ready to accept other instructions. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. If the page being addressed is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits, the Block Erase instruction will not be implemented.

Figure 9-37 64KB Block Erase Instruction (SPI Mode)

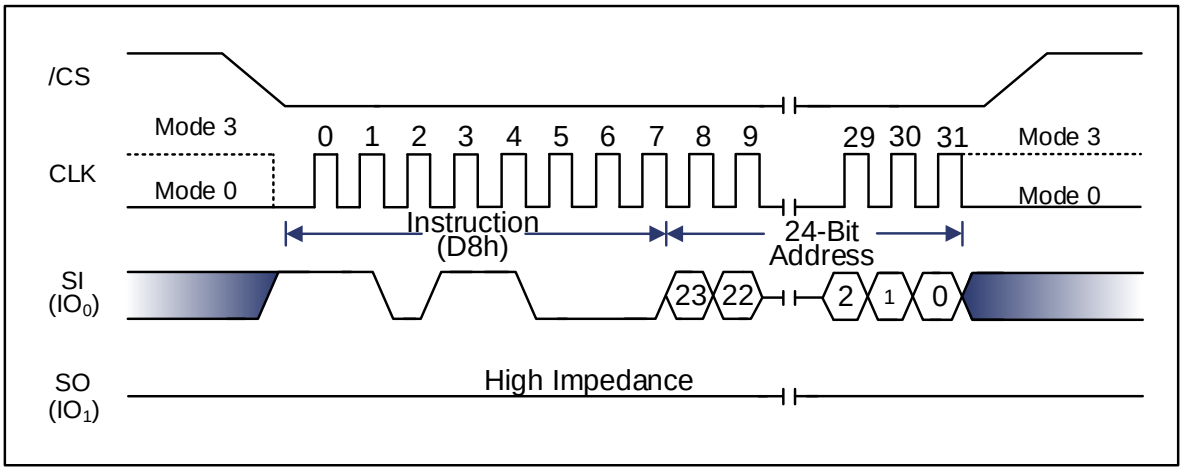
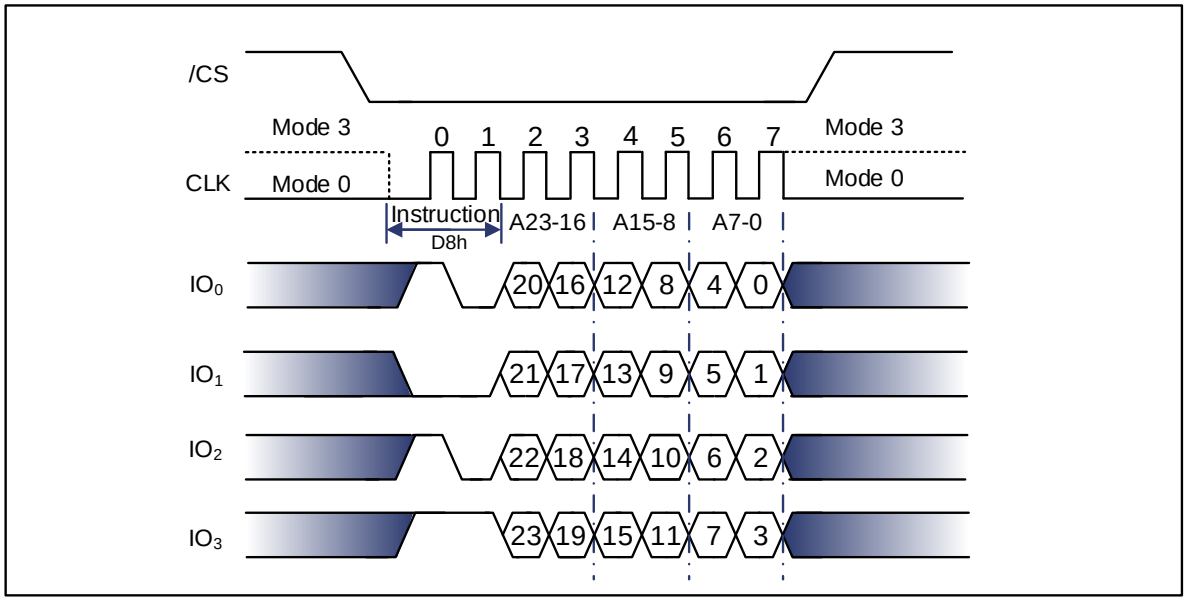


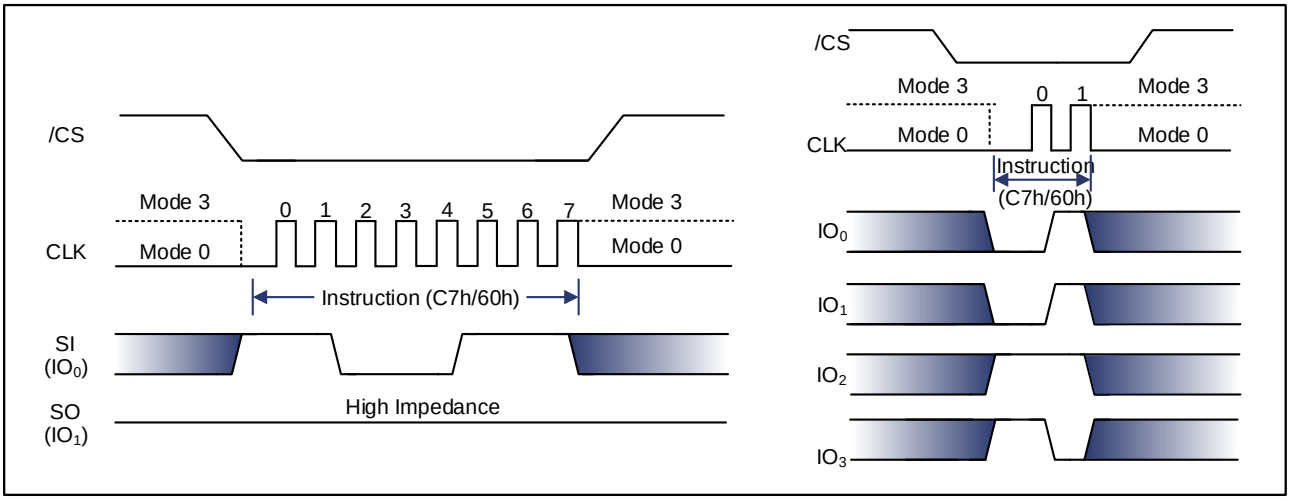
Figure 9-38 64KB Block Erase Instruction (QPI Mode)



9.2.22 Chip Erase (C7h / 60h)

By accepting the Chip Erase instruction, all memory can be set within the device to an erased state of all 1s (FFh). A Write Enable instruction must be carried out before the device can accept the Chip Erase Instruction (Status Register bit WEL must be equal to 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”, displayed in Figure 9-39. After the eighth bit has been latched, the /CS pin must be driven high. If not, the Chip Erase instruction will not be performed. After /CS is driven high, the self-timed Chip Erase instruction will start to be executed for a duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction can still be accessed to check the status of the BUSY bit. The BUSY bit is 1 during the Chip Erase cycle and turns to 0 when completed and the device is ready to accept other instructions. At the end of the Chip Erase cycle, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region If any memory area is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

Figure 9-39 Chip Erase Instruction for SPI Mode (left) or QPI Mode (right)



9.2.23 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h” allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from any other sector or block. The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h, 44h and 42h) are not allowed to be executed during Erase Suspend. Erase Suspend is only valid during the Sector or Block erase operation. The Erase Pause instruction is ignored if it is written during a Chip Erase operation. Write Status Register instructions (01h, 31h and 11h) and Erase instructions (20h, 52h, D8h, C7h, 60h and 44h) and Program instructions (02h, 32h and 42h) are not accepted during Program Suspend. Program Suspend is only valid during Page Program or Quad Page Program operation, demonstrated in Figure 9-40 and Figure 9-41. The device will only accept the Erase/Program Suspend instruction "75h" if the SUS bit in the Status Register equals 0 and the BUSY bit equals 1 while a Sector or Block Erase or Page Program operation is in progress. If the SUS bit is equal to 1 or the BUSY bit is equal to 0, the Suspend instruction will be ignored by the device. A maximum time of “tSUS” (as indicated by the Characteristics of AC) is required to suspend the Erase or Program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “tSUS” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” can’t be issued earlier than a minimum of time of “tSUS” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. The SUS bit in the Status Register will also be reset to 0. Data within the page, sector or block being suspended may become corrupted. To prevent unexpected power interruptions and to maintain data integrity during Erase/Program Suspend state, system design techniques are advised to use.

Figure 9-40 Erase/Program Suspend Instruction (SPI Mode)

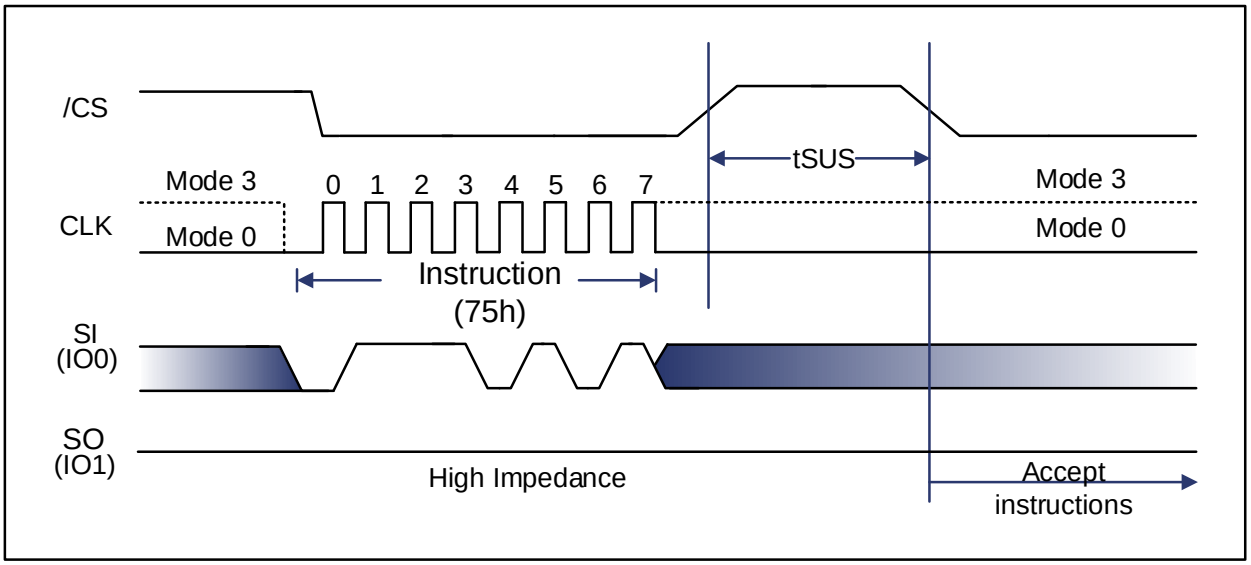
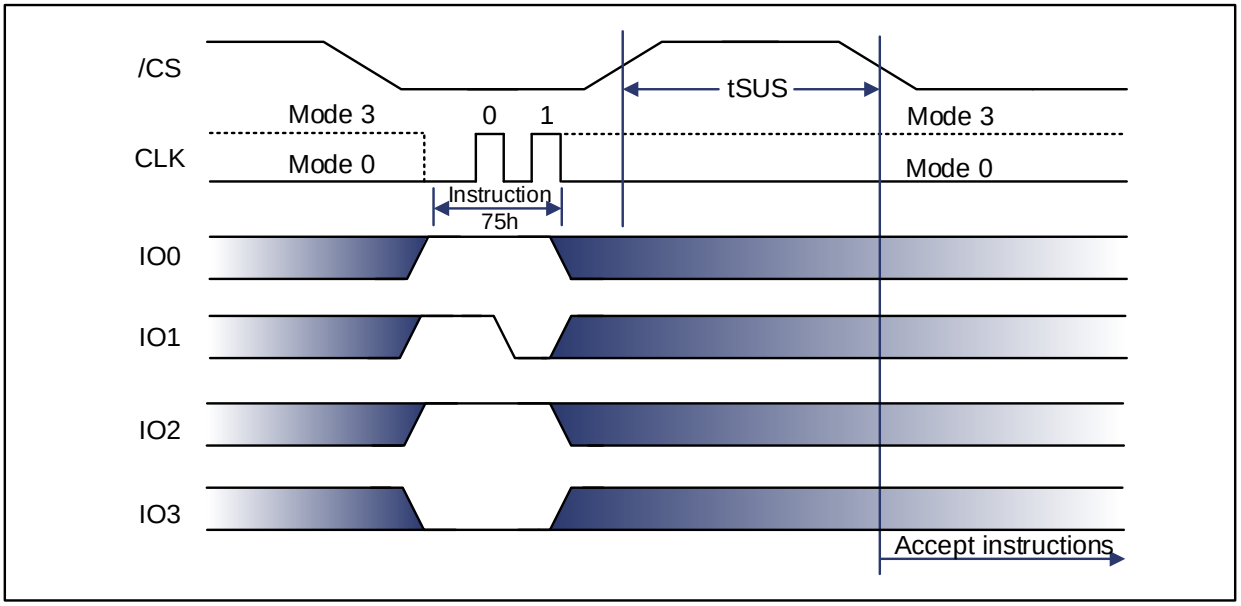


Figure 9-41 Erase/Program Suspend Instruction (QPI Mode)



9.2.24 Erase / Program Resume (7Ah)

After an Erase/Program Suspend, the Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation. The Resume instruction "7Ah" will be accepted by the device only if the SUS bit in the Status Register is equal to 1 and the BUSY bit equal to 0. Immediately after the instruction is issued, the SUS bit will be cleared from 1 to 0, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device.

When the previous Erase/Program Suspend operation is interrupted by an unexpected power failure, the Resume instruction is ignored. It is also required that no subsequent Erase/Program Suspend instruction is issued within the minimum time of “t_{ERS}” after the previous Resume instruction. The sequence of Erase/Program Resume instruction is shown in Figure 9-42 and Figure 9-43.

Figure 9-42 Erase/Program Resume Instruction (SPI Mode)

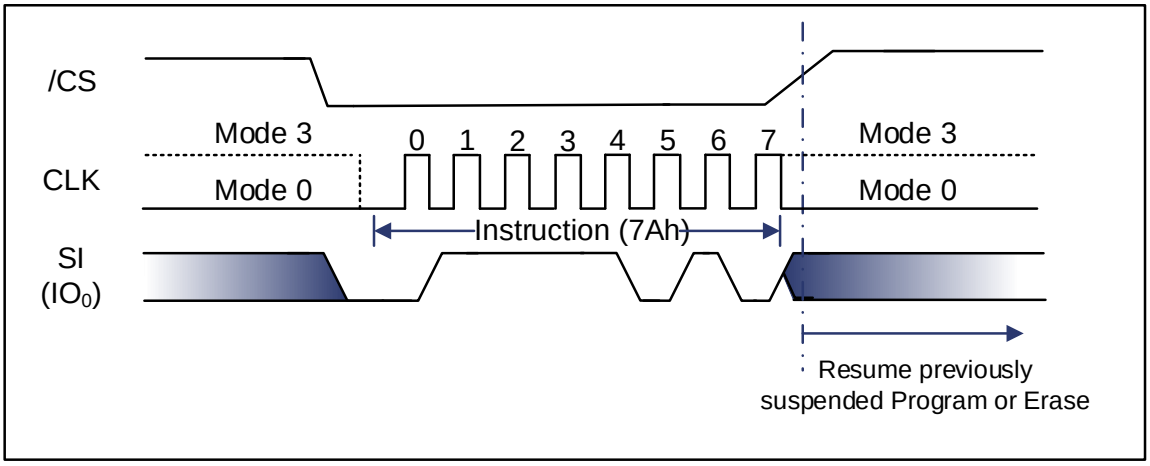
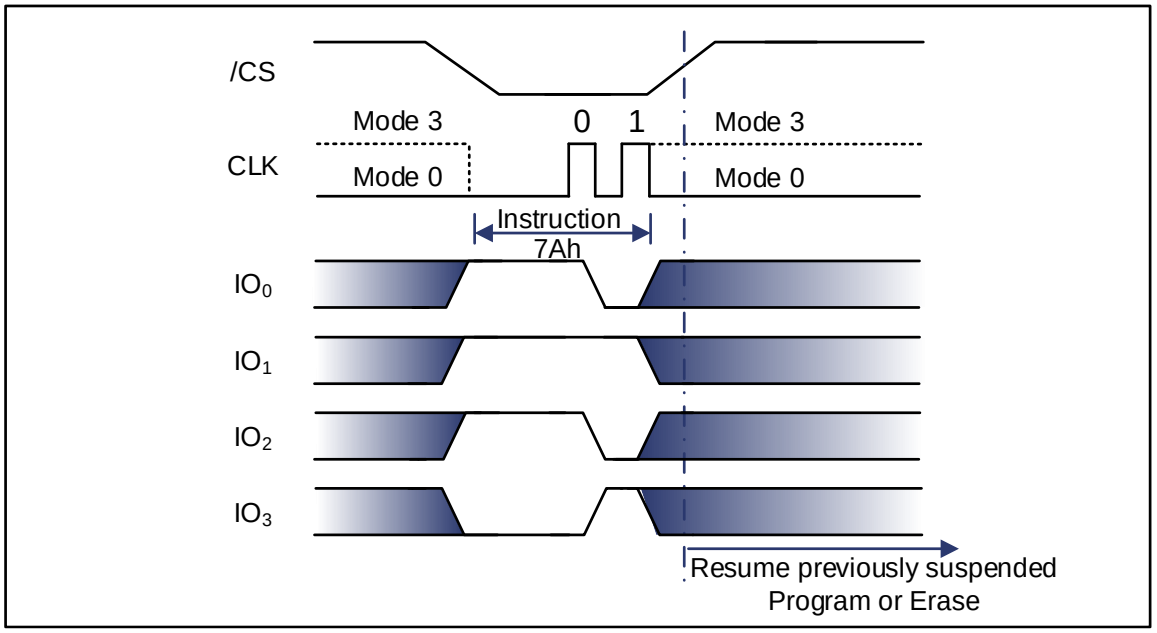


Figure 9-43 Erase/Program Resume Instruction (QPI Mode)



9.2.25 Power-down (B9h)

The standby current can be further reduced by means of a Power-down instruction, although it is relatively low during normal operation. The lower power consumption makes the Power-down instruction particularly useful for battery-powered applications (as indicated by the Characteristics of ICC1 and ICC2 in AC).

After the eighth bit has been latched, the /CS pin must be driven high. If not, the Power-down instruction will not be executed. After /CS is driven high, the power-down state will be entered for the duration of t_{DP} (as indicated by the Characteristics of AC). While in the power-down state, only the Release Power- down/Device ID (ABh) instruction, which restores the device to normal operation, will be recognized. All other instructions are disabled. This includes the Read Status Register instruction, which is always available during normal operation. All but one instruction is forbidden, which makes the Power Down state a useful condition for securing maximum write protection. The device is always powered up at the standby current of ICC1 during normal operation. The instruction is initiated by driving the /CS pin low and transferring the instruction code “B9h”, as demonstrated in Figure 9-44 and Figure 9-45.

Figure 9-44 Deep Power-down Instruction (SPI Mode)

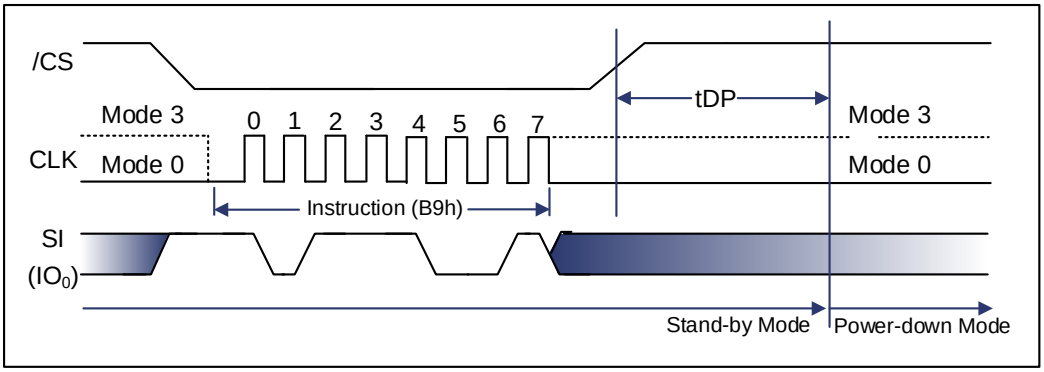
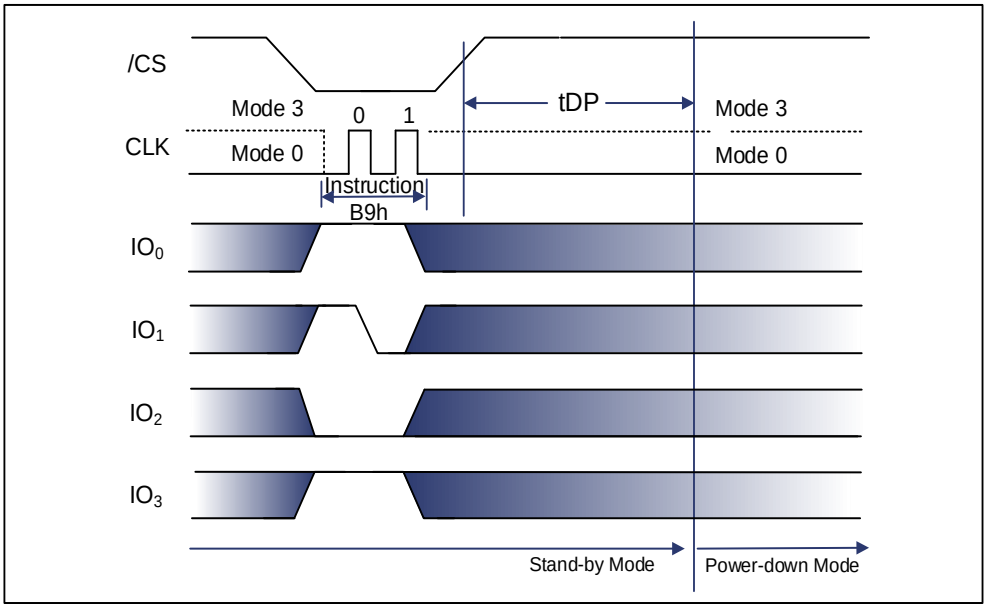


Figure 9-45 Deep Power-down Instruction (QPI Mode)



9.2.26 Release Power-down / Device ID (ABh)

The multi-purpose instruction of Release from Power-down/Device ID can be adopted to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

As shown in Figure 9-46 and Figure 9-47, to release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high. Before the device will resume normal operation and accept other commands, release from a power-down state will take a duration of t_{RES1} (as indicated by the Characteristics of AC) The /CS pin must remain high for the duration of tRES1.

When used only to obtain the Device ID in a non-power-down state, the instruction is initiated by driving the /CS pin low and shifting the 3 dummy Bytes after the instruction code "ABh". The Device ID bits are then shifted out on the falling edge of CLK, with the most significant bit (MSB) first. The Device ID can be read continuously and the instruction is done by driving /CS high. The Device ID value is listed in the Manufacturer and Device Identification table.

Figure 9-46 Release Power-down Instruction (SPI Mode)

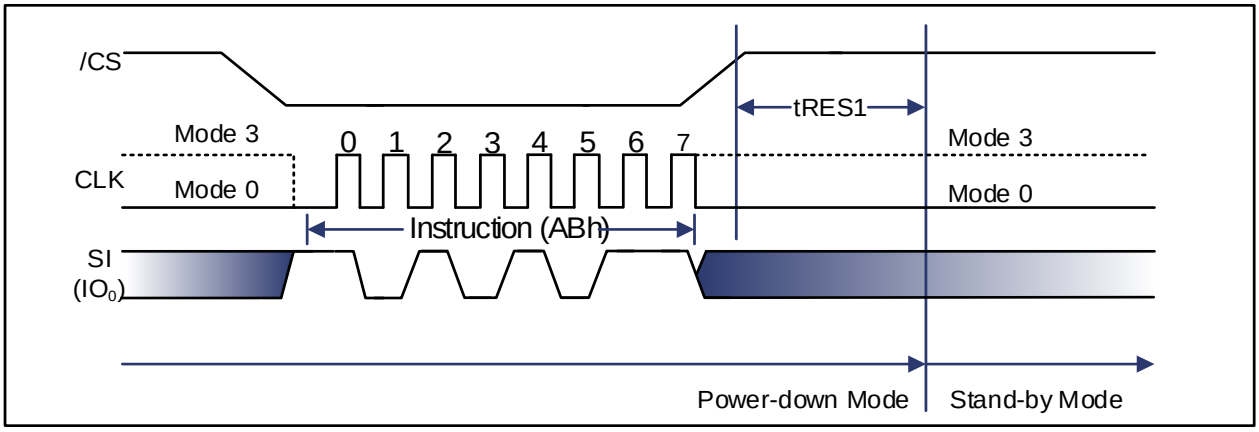


Figure 9-47 Release Power-down Instruction (QPI Mode)

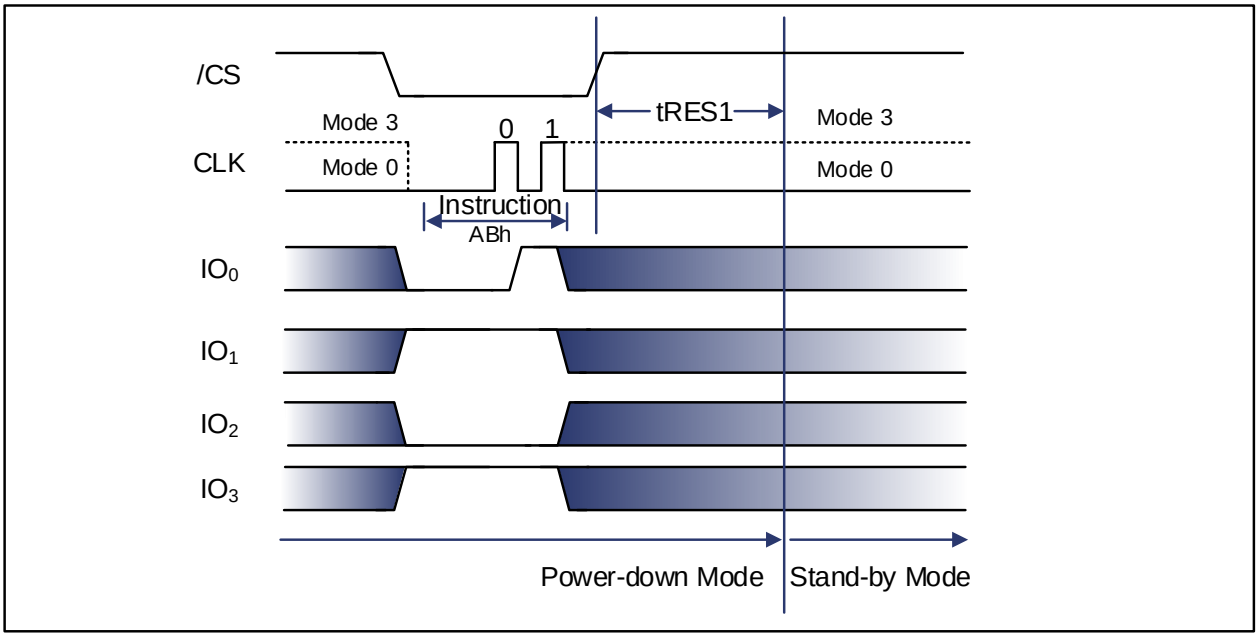


Figure 9-48 Release Power-down / Device ID Instruction (SPI Mode)

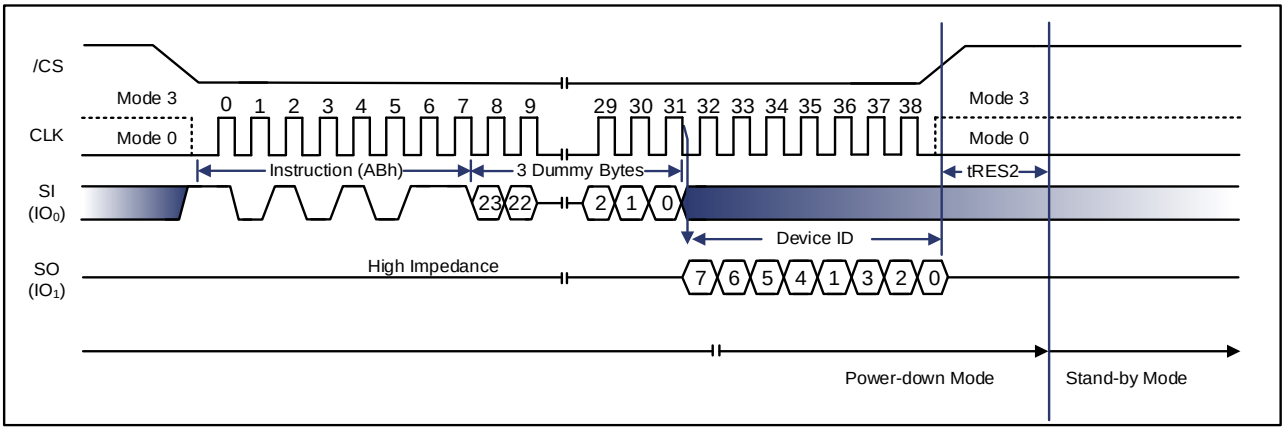
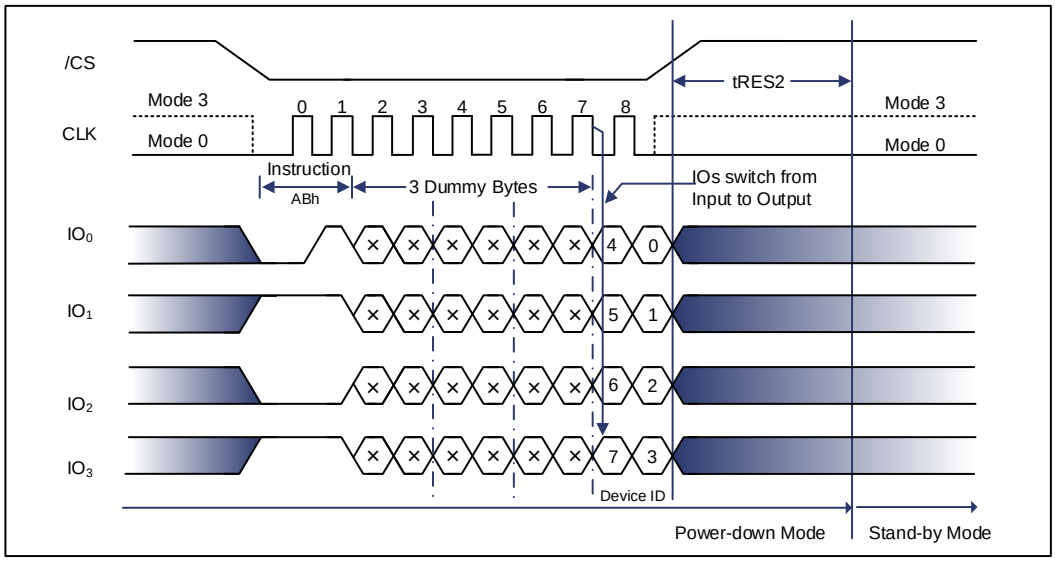


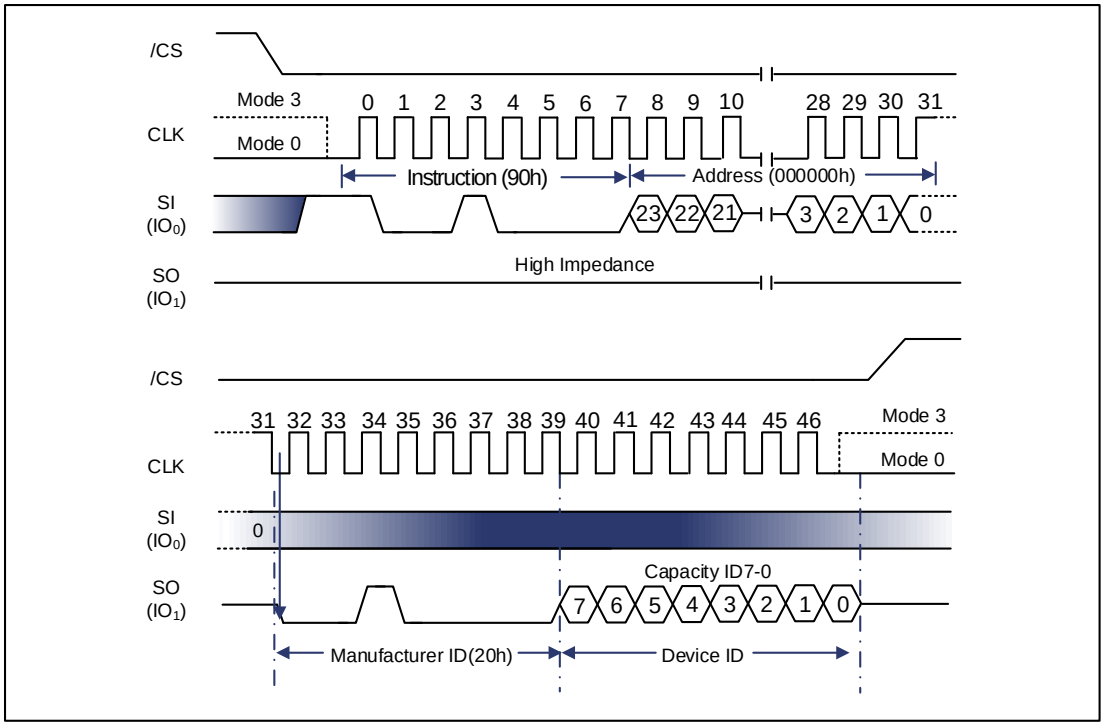
Figure 9-49 Release Power-down / Device ID Instruction (QPI Mode)



9.2.27 Read Manufacturer / Device ID (90h)

As a replacement for the Release from Power-down/Device ID instruction, the Read Manufacturer/Device ID instruction (90h) provides both the JEDEC assigned manufacturer ID and the specific device ID. The Read Manufacturer/Device ID instruction works very similarly as the Release from Power-down/Device ID instruction. As shown in Figure 9-50, the instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” and the 24-bit address (A23-A0) of 000000h. Afterwards, the Manufacturer ID for XMC (20h) and the Device ID are shifted out first with the most significant bit (MSB) on the falling edge of CLK. The Device ID values for the device are listed in Manufacturer and Device Identification table and the instruction is done by driving /CS high.

Figure 9-50 Read Manufacturer / Device ID Instruction (SPI Mode)

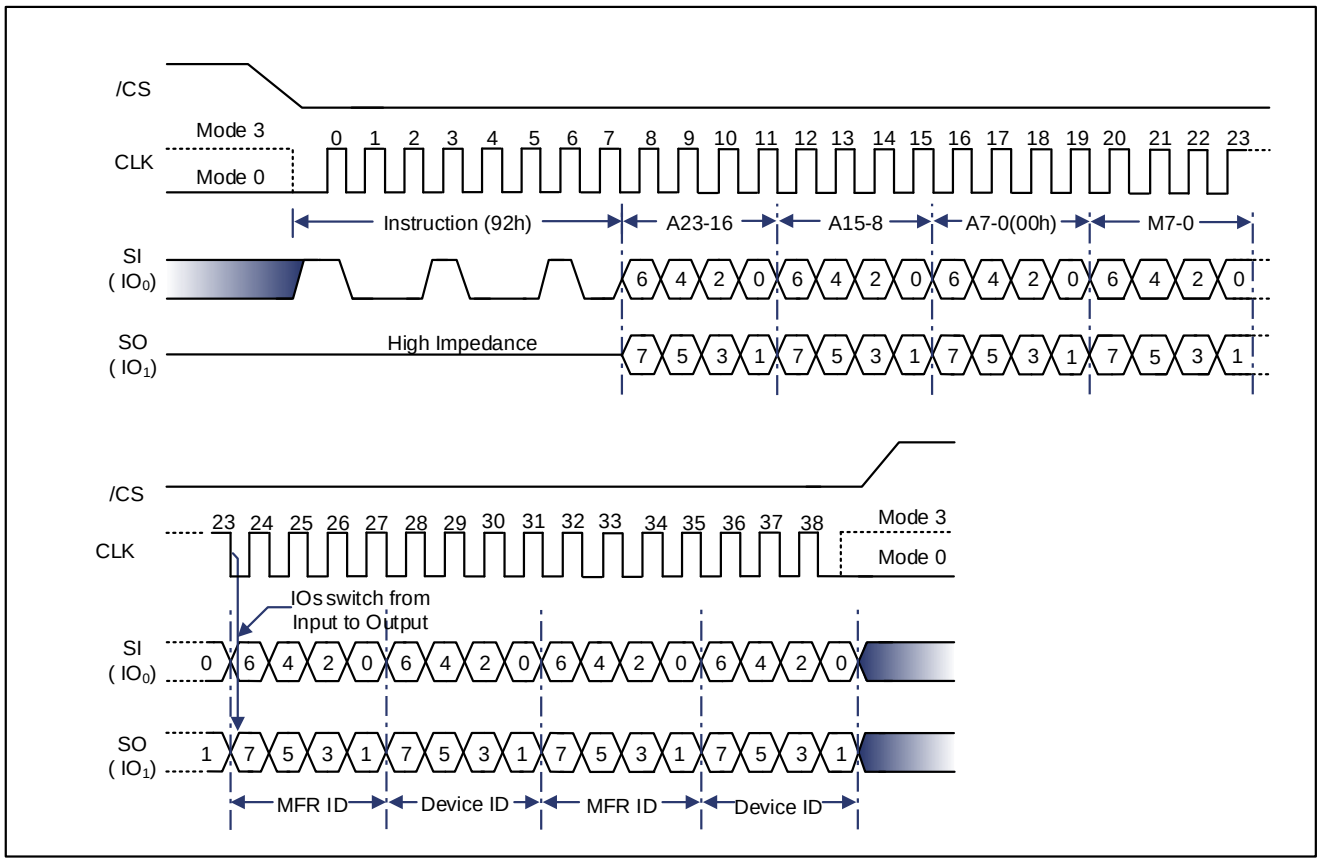


9.2.28 Read Manufacturer / Device ID Dual I/O (92h)

As an alternative to the Read Manufacturer/Device ID instruction, the Read Manufacturer/Device ID Dual I/O instruction (92h) provides both the JEDEC assigned manufacturer ID and specific device ID at twice the speed.

The Read Manufacturer / Device ID Dual I/O instruction works similar to the Fast Read Dual I/O instruction. As shown in Figure 9-51, the instruction is initiated by driving the /CS pin low and shifting the instruction code “92h” followed by a 24-bit address (A23-A0) of 000000h, but two Address bits can be entered at each clock. After that, the Manufacturer ID for XMC (20h) and the Device ID are shifted out 2 bits per clock with the most significant bit (MSB) first on the falling edge of CLK with the most significant bits (MSB) first. The Device ID values for the device are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

Figure 9-51 Read Manufacturer / Device ID Dual I/O Instruction (SPI Mode only)



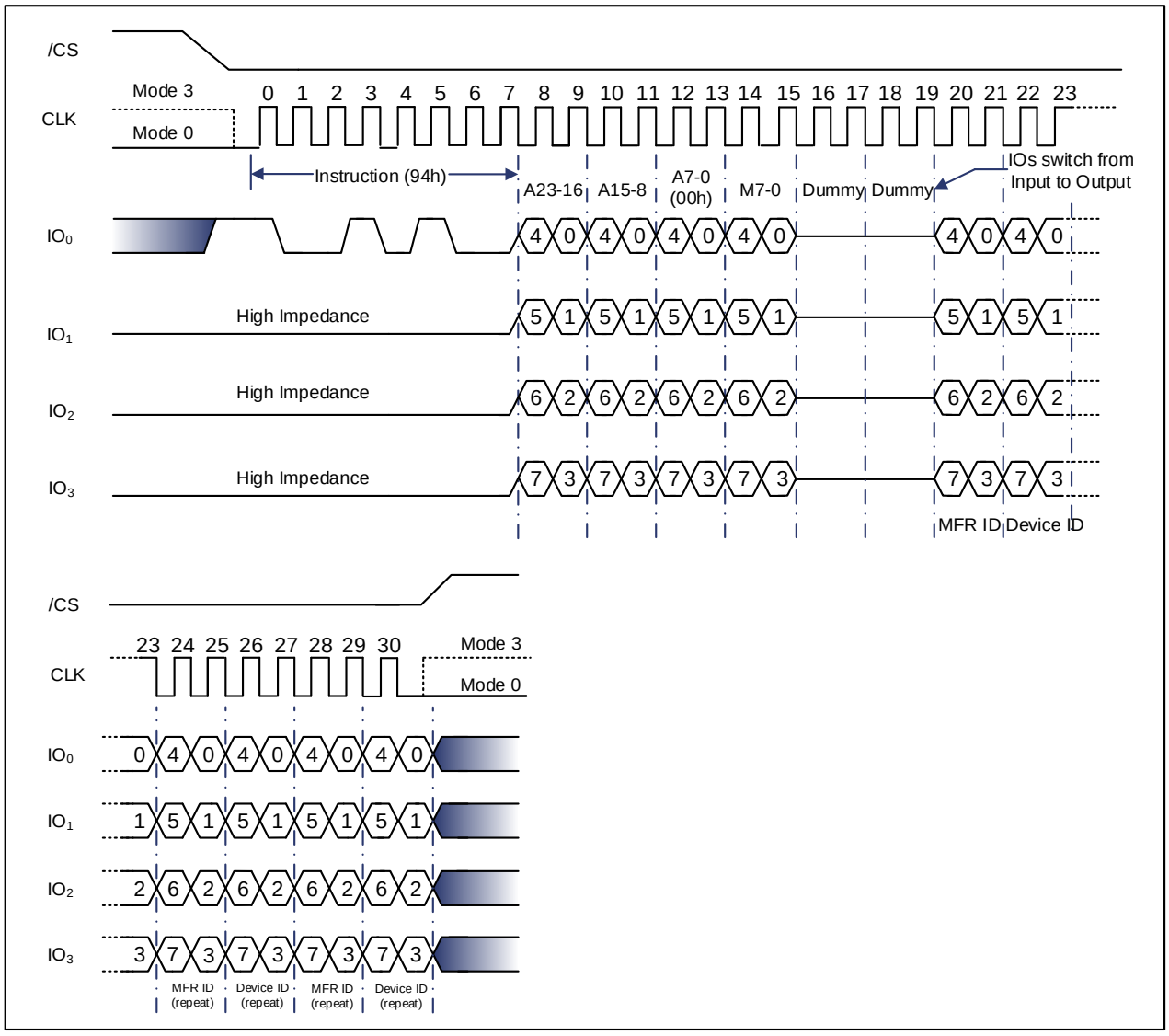
Note:

The “the Manufacturer / Device ID Dual I/O Instruction (SPI Mode only) low and shifting the instruction.

9.2.29 Read Manufacturer / Device ID Quad I/O (94h)

As an alternative to the Read Manufacturer/Device ID instruction, the Read Manufacturer/Device ID Quad I/O instruction (94h) provides both the JEDEC assigned manufacturer ID and specific device ID at four times the speed. The Read Manufacturer / Device ID Quad I/O instruction works similarly as the Fast Read Quad I/O instruction. As shown in Figure 9-52, the instruction is initiated by driving the /CS pin low and shifting the instruction code “94h”, followed by a four clock dummy cycles and then a 24-bit address (A23-A0) of 000000h, but with the capability to enter a 4 bit address at each clock. After that, the Manufacturer ID for XMC (20h) and the Device ID are shifted out four bits per clock with the most significant bit (MSB) first on the falling edge of CLK. The Device ID values for the XM25QH16D are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

Figure 9-52 Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode only)



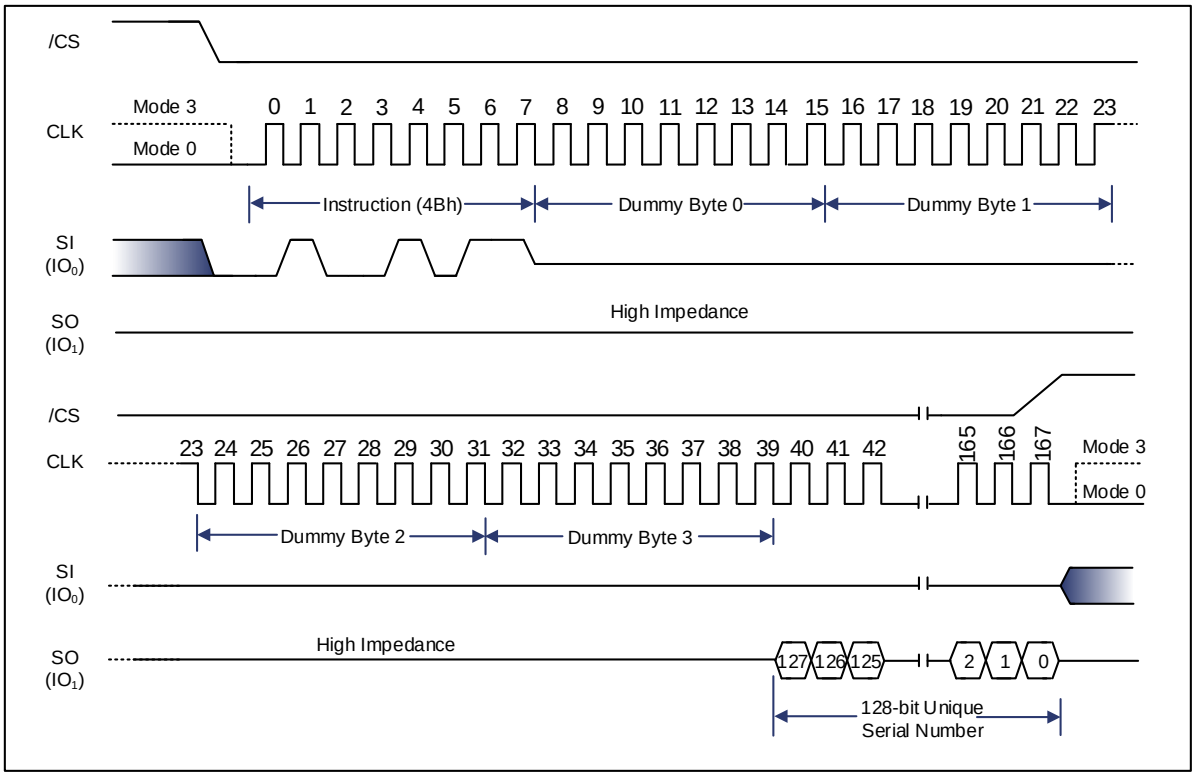
Note:

The Manufacturer / Device ID Quad I/O Instruction (SPI Mode only) low and shifting the instruction.

9.2.30 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction (4Bh) is unique to each device by accessing a factory-set and read-only 128-bit number. The ID number can be applied together with user software methods to help prevent copying or cloning of the system. Followed by a four Bytes of dummy clocks driving the /CS pin low and shifting the instruction code “4Bh” can activated the Read Unique ID instruction., After that, as shown in Figure 9-53, the 128-bit ID is shifted out on the falling edge of CLK (data read after the 128-bit ID will always be FFh).

Figure 9-53 Read Unique ID Number Instruction (SPI Mode only)



9.2.31 Read JEDEC ID (9Fh)

For compatibility reasons, the device provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories adopted in 2003.

As shown in Figure 9-54 & Figure 9-55, the instruction is activated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID Byte for XMC (20h) and two Device ID Bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out with the most significant bit (MSB) first on the falling edge of CLK. For memory type and capacity values, please refer to Manufacturer and Device Identification table.

Figure 9-54 Read JEDEC ID Instruction (SPI Mode)

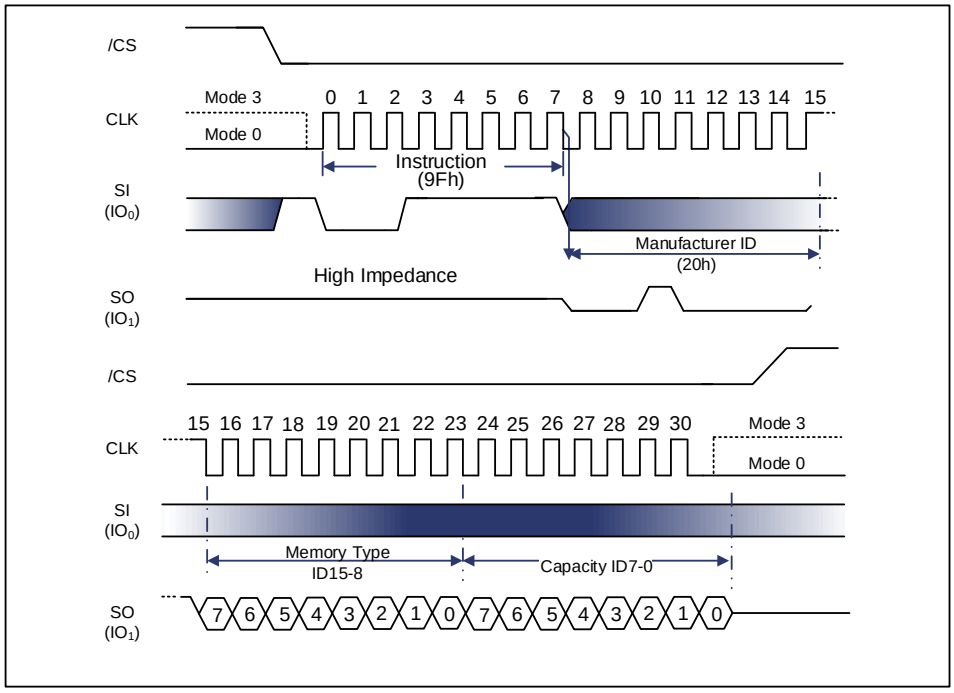
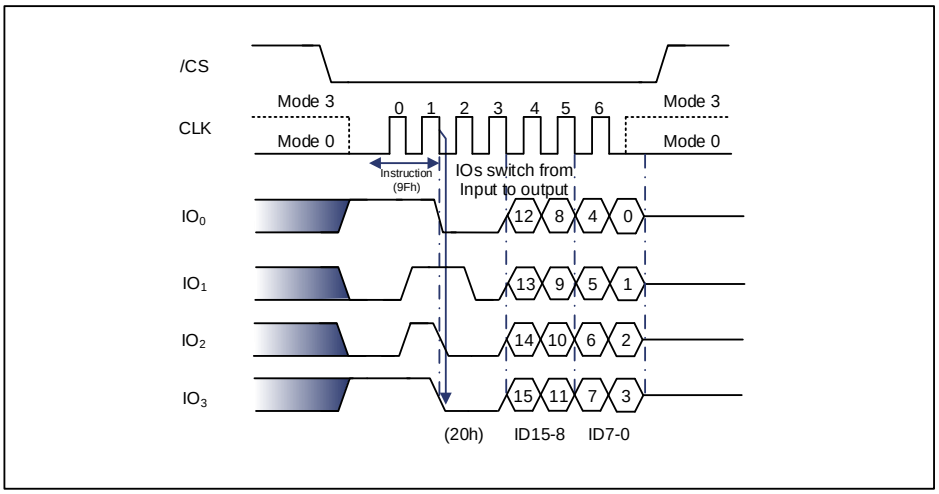


Figure 9-55 Read JEDEC ID Instruction (QPI Mode)



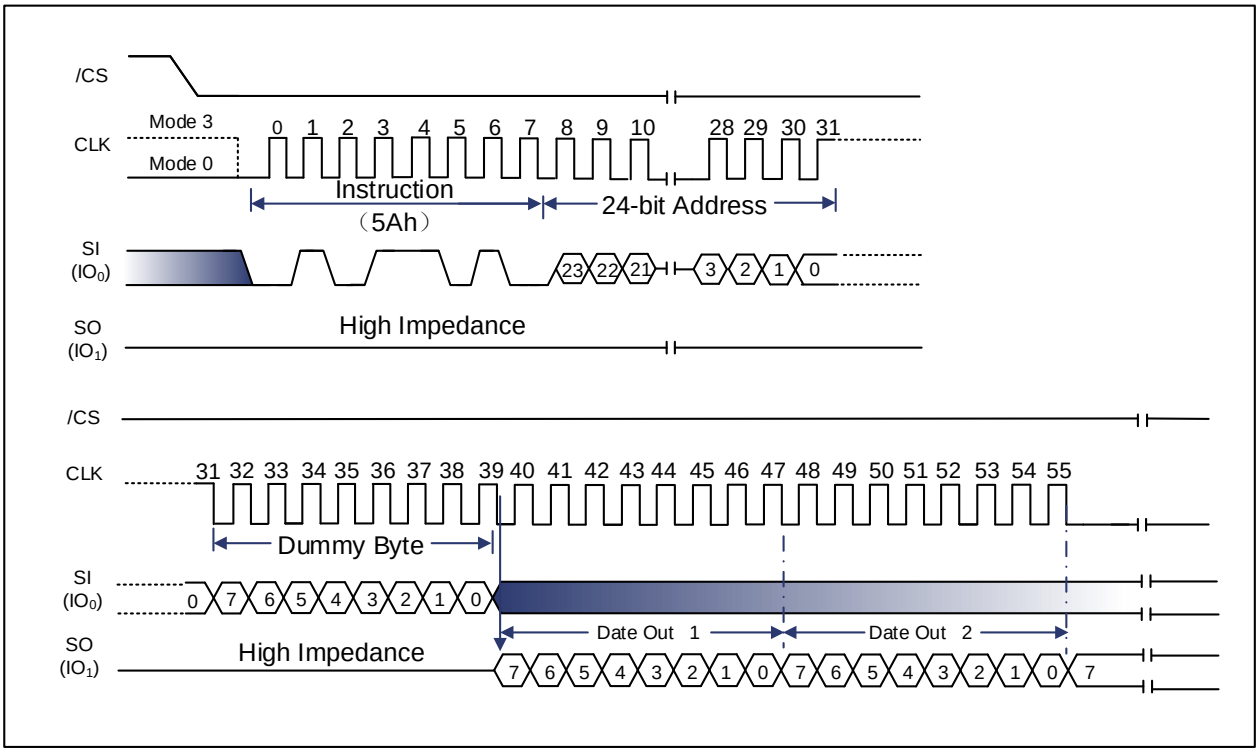
9.2.32 Read SFDP Register (5Ah)

The device features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available instructions and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. There is currently only one PID table specified, but more tables will be added in the future. The Read SFDP Register instruction is compatible with the SFDP standard originally developed in 2010 for PC and other applications, as well as the JEDEC standard JESD216 published in 2011. The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216B

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah", followed by a 24-bit address (A23-A0)(1) into the SI pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out with the most significant bit (MSB) first on the falling edge of the 40th CLK, as shown in Figure 9-56. After each Byte of data is shifted out, the Byte address is automatically incremented to the next Byte address. The last Byte address of the register is FFh (data read after the last address will always be FFh), For SFDP register values and descriptions, please refer to the following SFDP Definition Table.

Note: A23-A8 = 0; A7-A0 are used to define the starting Byte address for the 256-Byte SFDP Register.

Figure 9-56 Read SFDP Register Instruction Sequence Diagram(Only SPI Mode)



Serial Flash Discoverable Parameters (SFDP) Signature and Parameter Identification Data Value

(Advanced Information)

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
SFDP Signature	00h	07 : 00	53h	Fixed: 50444653h
	01h	15 : 08	46h	
	02h	23 : 16	44h	
	03h	31 : 24	50h	
SFDP Minor Revision Number	04h	07 : 00	06h	Star from 0x00
SFDP Major Revision Number	05h	15 : 08	01h	Star from 0x01
Number of Parameter Headers (NPH)	06h	23 : 16	02h	This number is 0-based.Therefore,0 indicates 1 parameter header.
Unused	07h	31 : 24	FFh	Reserved
ID Number(JEDEC)	08h	07 : 00	00h	00h:it indicates a JEDEC specified header.
Parameter Table Minor Revision Number	09h	15 : 08	06h	Star from 0x00
Parameter Table Major Revision Number	0Ah	23 : 16	01h	Star from 0x01
Parameter Table Length (in double word)	0Bh	31 : 24	10h	How many DWORDs in the parameter table
Parameter Table Pointer (PTP)	0Ch	07 : 00	30h	First address of JEDEC Flash Parameter table
	0Dh	15 : 08	00h	
	0Eh	23 : 16	00h	
Unused	0Fh	31 : 24	FFh	
ID number(Manufacturer ID)	10h	07 : 00	20h	It indicates manufacture ID
Parameter Table Minor Revision Number	11h	15 : 08	00h	Start from 00h
Parameter Table Major Revision Number	12h	23 : 16	01h	Start from 01h
Parameter Table Length(in double word)	13h	31 : 24	04h	How many DWORDs in the parameter table
Parameter Table Pointer(PTP)	14h	07 : 00	D0h	First address of VENDOR Flash Parameter table
	15h	15 : 08	00h	
	16h	23 : 16	00h	
Unused	17h	31 : 24	FFh	
ID number (4-Byte Address Instruction)	18h	07 : 00	84h	4-Byte Address Instruction parameter ID
Parameter Table Minor Revision Number	19h	15 : 08	00h	Start from 00h
Parameter Table Major Revision Number	1Ah	23 : 16	01h	Start from 01h
Parameter Table Length (in double word)	1Bh	31 : 24	02h	How many DWORDs in the Parameter table
Parameter Table Pointer (PTP)	1Ch	07 : 00	C0h	First address of 4-Byte Address Instruction table
	1Dh	15 : 08	00h	
	1Eh	23 : 16	00h	
Unused	1Fh	31 : 24	FFh	

Parameter ID (0) JEDEC Flash Parameter Tables 1/9

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Block / Sector Erase sizes	30h	01 : 00	01b	00:Reserved, 01:4KB erase, 10:Reserved, 11:not supported 4KB erase
Write Granularity		02	1b	0:1Byte,1:64Byte or larger
Volatile Status Register Block Protect bits		03	0b	0: Block Protect bits in device's status register are solely non-volatile or may be programmed either as volatile using the 50h instruction for write enable or non-volatile using the 06h instruction for write enable. 1: Block Protect bits in device's status register are solely volatile.
Write Enable Instruction Select for Writing to Volatile Status Registers		04	0b	0:use 50h instruction 1:use 06h instruction
Unused		07 : 05	111b	Contains 111b and can never be changed
4KB Erase Instruction	31h	15 : 08	20h	
(1-1-2) Fast Read(1)	32h	16	1b	0 = not supported 1 = supported
Address Bytes Number used in addressing flash array		18 : 17	00b	00:3Byte only, 01:3 or 4Byte 10:4Byte only, 11:Reserved
Double Transfer Rate (DTR) clocking		19	1b	0 = not supported 1 = supported
(1-2-2) Fast Read		20	1b	0 = not supported 1 = supported
(1-4-4) Fast Read		21	1b	0 = not supported 1 = supported
(1-1-4) Fast Read		22	1b	0 = not supported 1 = supported
Unused		23	1b	
Unused	33h	31 : 24	FFh	

Parameter ID (0) JEDEC Flash Parameter Tables 2/9

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Flash Memory Density	37h : 34h	31 : 00	00FFFFFFh	For densities 2 gigabits or less, bit-31 is set to 0b. The field 30:0 defines the size in bits. Example: 00FFFFFFh = 16 megabits For densities 4 gigabits and above, bit-31 is set to 1b. The field 30:0 defines 'N' where the density is computed as 2^N bits (N must be >= 32). Example: 80000021h = 2^33 = 8 gigabits

Parameter ID (0) JEDEC Flash Parameter Tables 3/9

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
(1-4-4)Fast Read number of Wait states(2)	38h	04 : 00	00100b	**00000b**: Not supported;00100b:4; 00110b:6; 01000b:8;
(1-4-4)Fast Read number of Mode Clocks(3)		07 : 05	010b	Mode clocks: **000b**:Not supported; 010: 2 clocks;
(1-4-4)Fast Read instruction	39h	15 : 08	EBh	
(1-1-4)Fast Read Number of Wait states	3Ah	20 : 16	01000b	**00000b**:Not suppoted; 00100b:4; 00100b:6; 01000b:8;
(1-1-4)Fast Read Number of Mode Clocks		23 : 21	000b	Mode clocks: **000b**:Not supported; 010b:2 clocks
(1-1-4)Fast Read Instruction	3Bh	31 : 24	6Bh	

Parameter ID (0) JEDEC Flash Parameter Tables 4/9

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
(1-1-2)Fast Read Number of Wait states	3Ch	04 : 00	01000b	00000b:Not supported; 00100b:4; 00110b:6; 01000b:8;
(1-1-2)Fast Read Number of Mode Clocks		07 : 05	000b	Mode clocks: 000b:Not supported; 010:2 clocks;
(1-1-2)Fast Read Instruction	3Dh	15 : 08	3Bh	
(1-2-2)Fast Read Number of Wait states	3Eh	20 : 16	00010b	00000b:Not supported; 00010b:2; 00100b:4; 0 0110b:6; 01000b:8
(1-2-2)Fast Read Number of Mode Clocks		23 : 21	010b	Mode clocks: 000b:Not supported; 010:2 clocks
(1-2-2)Fast Read Instruction	3Fh	31 : 24	BBh	

Parameter ID (0) JEDEC Flash Parameter Tables 5/9

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
(2-2-2)Fast Read	40h	00	0b	0 = not supported 1 = supported
Unused		03 : 01	111b	
(4-4-4)Fast Read		04	1b	0 = not supported 1 = supported
Unused		07 : 05	111b	
Unused	43h : 41h	31 : 08	FFFFFFh	

Parameter ID (0) JEDEC Flash Parameter Tables 6/9

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Unused	45h : 44h	15 : 00	FFFFh	
(2-2-2)Fast Read Number of Wait states	46h	20 : 16	00000b	**00000b**:Not supported; 00100b:4; 00110b:6; 01000b:8;
(2-2-2) Fast Read Number of Mode Clocks		23 : 21	000b	Mode Clocks: **000b**:Not supported; 010:2 clocks;
(2-2-2)Fast Read Instruction	47h	31 : 24	FFh	

Parameter ID (0) JEDEC Flash Parameter Tables 7/9

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Unused	49h : 48h	15 : 00	FFFFh	
(4-4-4)Fast Read Number of Wait states	4Ah	20 : 16	00010b	**00000b:**Not supported; 00010:2; 00100b:4; 00110b:6; 01000b:8;
(4-4-4) Fast Read Number of Mode Clocks		23 : 21	010b	Mode Clocks: **000b**:Not supported; 010:2 clocks;
(4-4-4)Fast Read Instruction	4Bh	31 : 24	EBh	

Parameter ID (0) JEDEC Flash Parameter Tables 8/9

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Erase Type 1 Size	4Ch	07 : 00	0Ch	Sector/block size=2^N Bytes(4) 0Ch:4KB; 0Fh:32KB; 10h:64KB;
Erase Type 1 Erase Instruction	4Dh	15 : 08	20h	
Erase Type 2 Size	4Eh	23 : 16	0Fh	Sector/block size=2^N Bytes 00h:NA; 0Fh:32KB; 10h:64KB
Erase Type 2 Erase Instruction	4Fh	31 : 24	52h	

Parameter ID (0) JEDEC Flash Parameter Tables 9/9

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Erase Type 3 Size	50h	07 : 00	10h	Sector/block size=2^N Bytes 00h:NA; 0Fh:32KB; 10h:64KB
Erase Type 3 Erase Instruction	51h	15 : 08	D8h	
Erase Type 4 Size	52h	23 : 16	00h	Sector/block size=2^N Bytes 00h:NA; 0Fh:32KB; 10h:64KB
Erase Type 4 Erase Instruction	53h	31 : 24	FFh	Not support

Parameter ID (0) JEDEC Flash Parameter Tables 9/9

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
Multiplier from typical erase time to maximum erase time	54h	03 : 00	0101b	Multiplier value: 0h~Fh (0~15); Max. time = 2 * (Multiplier + 1) * Typical Time
Erase Type 1 Erase Time (Typical)	54h	07 : 04	00001b	Count value: 00h~1Fh (0~31); Typical Time = (Count + 1) * Units
	55h	08		
		10 : 09	01b	Units 00: 1ms, 01: 16ms; 10b: 128ms; 11b: 1s
Erase Type 2 Erase Time (Typical)		15 : 11	00011b	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units
	56h	17 : 16	01b	Units 00: 1ms, 01: 16ms; 10b: 128ms; 11b: 1s;
Erase Type 3 Erase Time (Typical)		22 : 18	00101b	Count value: 00h~1Fh (0~31); Typical Time = (Count + 1) * Units
		24 : 23	01b	Units 00: 1 ms; 01: 16 ms; 10b: 128ms; 11b: 1s
Erase Type 4 Erase Time (Typical)	57h	29 : 25	00000b	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units
		31 : 30	00b	Units 00: 1ms, 01: 16ms 10b: 128 ms, 11b: 1s
Multiplier from typical time to max time for Page or Byte program	58h	03 : 00	0100b	Multiplier value: 0h~Fh (0~15) Max. time = 2 * (Multiplier + 1) *Typical Time
Page Program Size		07 : 04	1000b	Page size = 2^N Bytes 2^8 = 256 Bytes, 8h = 1000b
Page Program Time (Typical)	59h	12 : 08	00011b	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units
		13	1b	Units 0: 8us, 1: 64us
Byte Program Time, First Byte (Typical)		15 : 14	1110b	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * Units
	5Ah	17 : 16		
		18	0b	Units 0: 1us, 1: 8us
Byte Program Time, Additional Byte (Typical)		22 : 19	0010b	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * Units
		23	0b	Units 0: 1us, 1: 8us
Chip Erase Time (Typical)	5Bh	28 : 24	00111b	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units
		30 : 29	01b	Units 00: 16ms, 01: 256ms 10: 4s, 11: 64s

Reserved		31	1b	Reserved
Prohibited Operations During Program Suspend	5Ch	03 : 00	1100b	**xxx0b**: May not initiate a new erase anywhere (erase nesting not permitted) **xxx1b**: May not initiate a new erase in the program suspended page size **xx0xb**: May not initiate a new page program anywhere (program nesting not permitted) **xx1xb**: May not initiate a new page program in the program suspended page size **x0xxb**: Refer to vendor datasheet for read restrictions **x1xxb**: May not initiate a read in the program suspended page size **0xxxb**: Additional erase or program restrictions apply **1xxxb**: The erase and program restrictions in bits 1:0 are sufficient
Prohibited Operations During Erase Suspend		07 : 04	1100b	**xxx0b**: May not initiate a new erase anywhere (erase nesting not permitted) **xxx1b**: May not initiate a new erase in the erase suspended erase type size **xx0xb**: May not initiate a page program anywhere **xx1xb**: May not initiate a page program in the erase suspended erase type size **x0xxb**: Refer to vendor datasheet for read restrictions **x1xxb**: May not initiate a read in the erase suspended erase type size **0xxxb**: Additional erase or program restrictions apply **1xxxb**: The erase and program restrictions in bits 5:4 are sufficient
Reserved	5Dh	08	1b	Reserved
Program Resume to Suspend Interval (Typical)		12 : 09	0000b	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * 64us
Program Suspend Latency (Max.)		15: 13	10101b	Count value: 00h~1Fh (0~31) Maximum Time = (Count + 1) * Units
	5Eh	17 : 16		
		19 : 18	01b	Units 00: 128ns, 01: 1us 10: 8us, 11: 64us
Erase Resume to Suspend Interval (Typical)		23 : 20	0111b	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * 64us
Erase Suspend Latency (Max.)	5Fh	28 : 24	10101b	Count value: 00h~1Fh (0~31) Maximum Time = (Count + 1) * Units

		30 : 29	01b	Units 00: 128ns, 01: 1us 10: 8us, 11: 64us
Suspend / Resume supported		31	0b	0= Support 1= Not supported
Program Resume Instruction	60h	07 : 00	7Ah	Instruction to Resume a Program
Program Suspend Instruction	61h	15 : 08	75h	Instruction to Suspend a Program
Erase Resume Instruction	62h	23 : 16	7Ah	Instruction to Resume Write/Erase
Erase Suspend Instruction	63h	31 : 24	75h	Instruction to Suspend Write/Erase
Reserved	64h	01 : 00	11b	Reserved: 11b
Status Register Polling Device Busy		07 : 02	111101b	**Bit 2**: Read BUSY bit [0] by 05h Read instruction **Bit 3**: Read bit 7 of Status Register by 70h Read instruction (0=not supported 1=support) **Bit 07:04**,Reserved: 1111b
Release from Deep Power-down (RDP) Delay (Max.)	65h	12 : 08	10011b	**Count value:** 00h~1Fh (0~31) Maximum Time = (Count + 1) * Units
		14 : 13	01b	Units 00: 128ns, 01: 1us 10: 8us, 11: 64us
Release from Deep Power-down (RDP) Instruction		15	10101011b	Instruction to Exit Deep Power Down **FFh:** Don't need command
	66h	22 : 16		
Enter Deep Power Down Instruction		23	10111001b	Instruction to Enter Deep Power Down
	67h	30 : 24		
Deep Power Down Supported		31	0b	0: Supported 1: Not supported
4-4-4 Mode Disable Sequences	68h	03 : 00	1001b	Methods to exit 4-4-4 mode **xxx1b**: issue FFh instruction **xx1xb**: issue F5h instruction **x1xxb**: device uses a read-modify-write sequence of operations **1xxxb**: issue the Soft Reset 66/99 sequence
4-4-4 Mode Enable Sequences	69h	07 : 04	00001b	Methods to enter 4-4-4 mode **x_xxx1b**: set QE per QER description above, then issue instruction 38h **x_xx1xb**: issue instruction 38h **x_x1xxb**: issue instruction 35h
		08		
0-4-4 Mode Supported		09	1b	Performance Enhance Mode, Continuous Read, Execute in Place 0: Not supported 1: Supported

0-4-4 Mode Exit Method		15 : 10	111101b	**xx_xxx1b**: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation. **xx_xx1xb**: If 3-Byte address active, input Fh on DQ0-DQ3 for 8 clocks. If 4-Byte address active, input Fh on DQ0-DQ3 for 10 clocks. **xx_x1xxb**: Reserved **xx_1xxxb**: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. **x1_xxxxb**: Mode Bit[7:0]≠Axh **1x_xxxxb**: Reserved
0-4-4 Mode Entry Method	6Ah	19 : 16	1101h	**xxx1b**: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode **x1xxb:** Mode Bit[7:0]=Axh **1xxxb**: Reserved
Quad Enable (QE) bit Requirements		22 : 20	100b	**000b**: No QE bit. Detects 1-1-4/1-4- 4 reads based on instruction **100b**: QE is bit 1 of status register 2. **010b**: QE is bit 6 of Status Register. where 1=Quad Enable or 0=not Quad Enable **111b**: Not Supported
HOLD and RESET Disable by bit 4 of Ext. Configuration Register		23	0b	0: Not supported
Reserved	6Bh	31 : 24	FFh	Reserved
Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1	6Ch	06 : 00	1101001b	**xxx_xxx1b**: Non-Volatile Status Register 1, powers-up to last written value, use instruction 06h to enable write **xxx_1xxxb**: Non-Volatile/Volatile status register 1 powers-up to last written value in the nonvolatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register. **xx1_xxxxb**: Status Register 1 contains a mix of volatile and non-volatile bits. The 06h instruction is used to enable writing of the register. **x1x_xxxxb**: Reserved **1xx_xxxxb**: Reserved
Reserved		07	1b	Reserved
Soft Reset and Rescue Sequence Support	6Dh	13 : 08	010000b	Return the device to its default power-on state Exit 4-Byte Addressing issue reset enable instruction 66h, then issue reset instruction 99h.
Exit 4-Byte Addressing		15 : 14	00b	**xx_xxxx_xxx1b**: issue instruction E9h to exit

	6Eh	23 : 16	11000000b	4-Byte address mode (write enable instruction 06h is not required) **xx_xxxx_x1xxb**: 8-bit volatile extended address register used to define A[31:A24] bits. Read with instruction C8h. Write instruction is C5h, data length is 1 Byte. Return to lowest memory segment by setting A[31:24] to 00h and use 3-Byte addressing. **xx_xx1x_xxxxb**: Hardware reset **xx_x1xx_xxxxb**: Software reset (see bits 13:8 in this DWORD) **xx_1xxx_xxxxb**: Power cycle **x1_xxxx_xxxxb**: Reserved **1x_xxxx_xxxxb**: Reserved
Enter 4-Byte Addressing	6Fh	31 : 24	10000000b	**xxxx_xxx1b**: issue instruction B7h (preceding write enable not required) **xxxx_x1xxb**: 8-bit volatile extended address register used to define A [31:24] bits. Read with instruction C8h. Write instruction is C5h with 1 Byte of data. Select the active 128 Mbit memory segment by setting the appropriate A [31:24] bits and use 3-Byte addressing. **xx1x_xxxxb**: Supports dedicated 4-Byte address instruction set. Consult vendor data sheet for the instruction set definition. **1xxx_xxxxb**: Reserved

Parameter ID (0) JEDEC Flash Parameter Tables 9/9

Description	Add(h) (Byte)	DW Add (Bit)	Data	Comment
Support for (1-1-1) READ Command, Instruction=13h	C0h	00	0b	0=not supported 1=supported
Support for (1-1-1) FAST_READ Command, Instruction=0Ch		01	0b	0=not supported 1=supported
Support for (1-1-2) FAST_READ Command, Instruction=3Ch		02	0b	0=not supported 1=supported
Support for (1-2-2) FAST_READ Command, Instruction=BCh		03	0b	0=not supported 1=supported
Support for (1-1-4) FAST_READ Command, Instruction=6Ch		04	0b	0=not supported 1=supported
Support for (1-4-4) FAST_READ Command, Instruction=ECh		05	0b	0=not supported 1=supported
Support for (1-1-1) Page Program Command, Instruction=12h		06	0b	0=not supported 1=supported
Support for (1-1-4) Page Program Command, Instruction=34h		07	0b	0=not supported 1=supported
Support for (1-4-4) Page Program Command, Instruction=3Eh	C1h	08	0b	0=not supported 1=supported
Support for Erase Command – Type 1 size, Instruction lookup in next Dword		09	0b	0=not supported 1=supported
Support for Erase Command – Type 2 size, Instruction lookup in next Dword		10	0b	0=not supported 1=supported
Support for Erase Command – Type 3 size, Instruction lookup in next Dword		11	0b	0=not supported 1=supported
Support for Erase Command – Type 4 size, Instruction lookup in next Dword		12	0b	0=not supported 1=supported
Support for (1-1-1) DTR_Read Command, Instruction=0Eh		13	0b	0=not supported 1=supported
Support for (1-2-2) DTR_Read Command, Instruction=BEh		14	0b	0=not supported 1=supported
Support for (1-4-4) DTR_Read Command, Instruction=EEh		15	0b	0=not supported 1=supported
Support for volatile individual sector lock Read command, Instruction=E0h	C2h	16	0b	0=not supported 1=supported
Support for volatile individual sector lock Write command, Instruction=E1h		17	0b	0=not supported 1=supported
Support for non-volatile individual sector lock read command, Instruction=E2h		18	0b	0=not supported 1=supported
Support for non-volatile individual sector lock write command, Instruction=E3h		19	0b	0=not supported 1=supported
Reserved		23 : 20	1111b	Reserved
Reserved	C3h	31 : 24	FFh	Reserved
Instruction for Erase Type 1	C4h	07 : 00	FFh	FFh=not supported
Instruction for Erase Type 2	C5h	15 : 08	FFh	FFh=not supported
Instruction for Erase Type 3	C6h	23 : 16	FFh	FFh=not supported
Instruction for Erase Type 4	C7h	31 : 24	FFh	FFh=not supported

Parameter ID (0) Flash Parameter Tables

Description	Add (h) (Byte)	DW Add (Bit)	Data	Comment
VCC supply maximum voltage	D1h:D0h	07:00	00h	2000h=2.000V 2700h=2.700V 3600h=3.600V
		15:08	36h	
VCC supply minimum voltage	D3h:D2h	23:16	00h	1650h=1.65V 1750h=1.75V 2250h=2.25V 2300h=2.3V 2350h=2.35V 2650h=2.65V 2700h=2.7V
		31:24	23h	
H/W /Reset pin	D5h:D4h	0	F99Fh	0 = not supported 1 = supported
H/W /Hold pin		1		0 = not supported 1 = supported
Deep Power Down Mode		2		0 = not supported 1 = supported
S/W Reset		3		0 = not supported 1 = supported
S/W Reset Instruction		11:04		Reset Enable(66h)should be issued before Reset instruction
Program suspend/resume		12		0 = not supported 1 = supported
Erase suspend/resume		13		0 = not supported 1 = supported
Unused		14		
Wrap-Around Read mode		15		0 = not supported 1 = supported
Wrap-Around Read mode instruction	D6h	23:16	77h	
Wrap-Around Read data length	D7h	31:24	64h	08h:support 8B wrap-around read 16h:8B&16B 32h:8B&16B&32B 64h:8B&16B&32B&64B
Individual block lock	DBh:D8h	0	E800h	0 = not supported 1 = supported
Individual block lock bit(Volatile/Nonvolatile)		1		0:Volatile 1:Nonvolatile
Individual block lock Instruction		09:02		0 = not supported 1 = supported
Individual block lock Volatile protect bit default protect status		10		0:Protect 1:Unprotect
Secured OTP		11		0 = not supported 1 = supported
Read Lock		12		0 = not supported 1 = supported
Permanent Lock		13		0 = not supported 1 = supported
Unused		15:14		
Unused		31:16	FFFFh	
Unused	DFh:DCh	31:00	FFFFFFFFh	

Note:

*[1] **(x-y-z)** means I/O mode nomenclature used to indicate the number of active pins used for the instruction (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4);*

*[2] **Wait States** is required dummy clock cycles after the address bits or optional mode clocks;*

*[3] **Mode clocks** is optional control bits that follow the address bits. These bits are driven by the system controller if they are specified. (eg,read performance enhance toggling bits);*

[4] 4KB=2^0Ch,32KB=2^0Fh,64KB=2^10h;;

[5] All unused and undefined area data is blank FFh.

9.2.33 Erase Security Registers (44h)

The device offers three 1024-Byte Security Registers that can be individually erased and programmed. These registers can be adopted by the system manufacturers to store security and other important information separately from the main memory array.The instruction works similarly as the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must be equal to 1). As displayed in

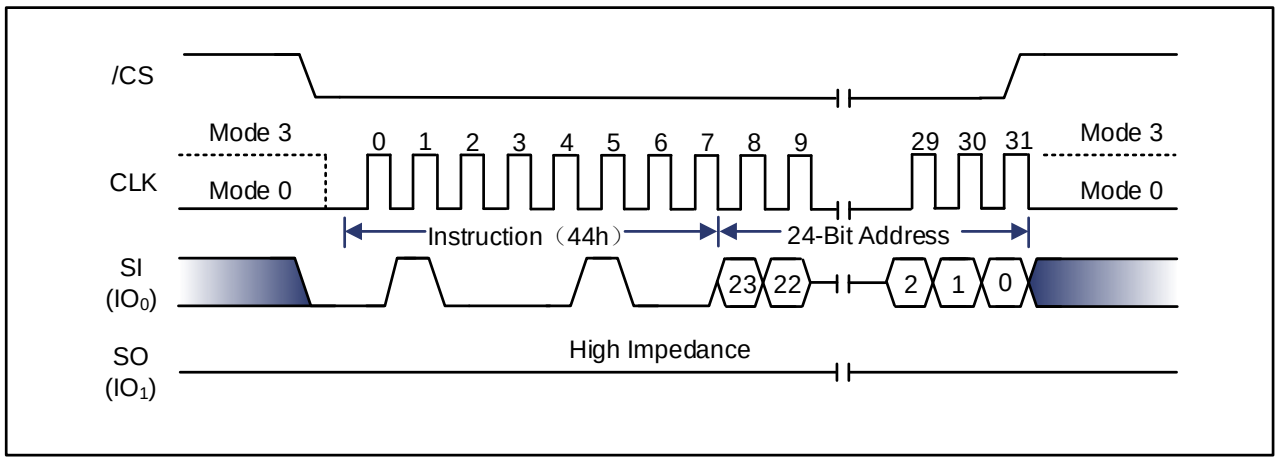
Figure 9-57, the instruction sequence as follow: set /CS low→ transfer instruction(44h)→24-bit address→ drive /CS high.

The /CS pin must be driven high after the eighth bit of the last Byte has been latched, otherwise, the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of tSE (as indicated by the Characteristics of AC).

While the Erase Security Register cycle is in progress, the Read Status Register instruction can still be accessed to check the status of the BUSY bit. The BUSY bit is 1 during the erase cycle and changes to 0 when the cycle is over and the device is ready to accept other instructions. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be applied to OTP protection of the security registers. Once the lock bit is set to 1, the corresponding security register will be permanently locked, Erase Security Register instruction to that register will be ignored.

ADDRESS	A23-16	A15-12	A11-10	A9-0
Security Register #1	00h	0 0 0 1	0 0	Do not Care
Security Register #2	00h	0 0 1 0	0 0	Do not Care
Security Register #3	00h	0 0 1 1	0 0	Do not Care

Figure 9-57 Erase Security Registers Instruction (SPI Mode only)



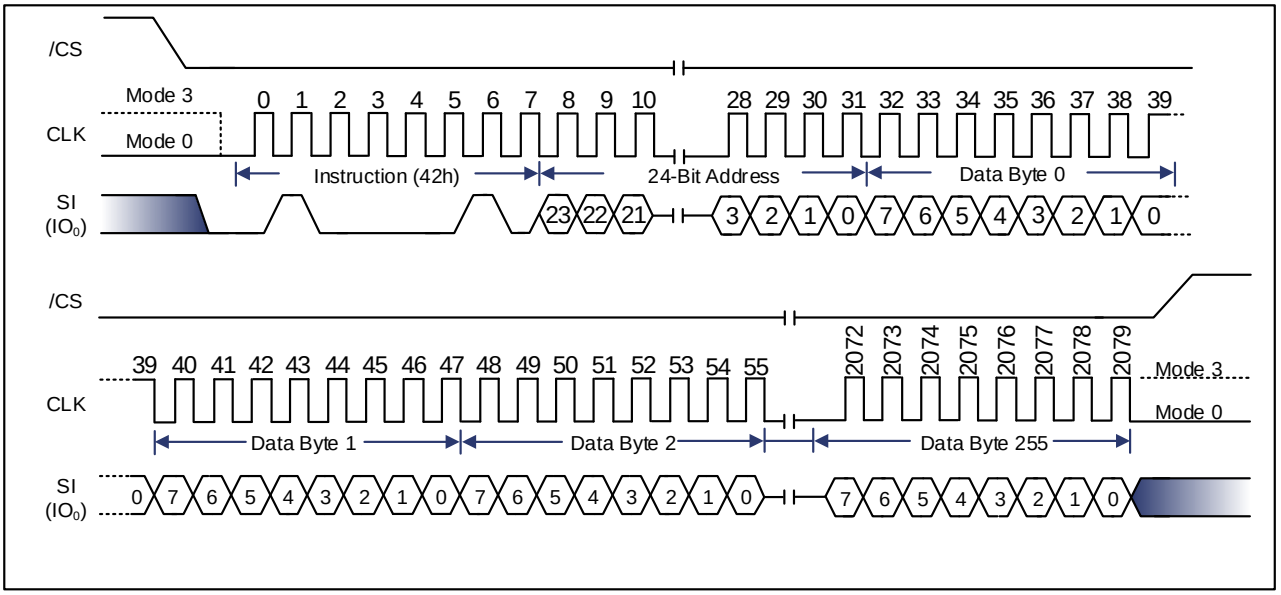
9.2.34 Program Security Registers (42h)

The Program Security Register instruction is similar to the Page Program instruction. It allows one Byte up to 1024 Bytes of security register data to be programmed on previously erased (FFh) memory locations. A Write Enable instruction must be initiated before the device will accept the Program Security Register Instruction (Status Register bit WEL=1). The instruction sequence: set /CS low → transfer instruction(42h) → send 24-bit address → drive /CS high, demonstrated in Figure 9-58.

The /CS pin must be held low for the entire duration of the instruction while data is being sent to the device. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be applied to OTP protection of the security registers. Once the lock bit is set to 1, the corresponding security register will be permanently locked, and Program Security Register instruction to that register will be ignored (Section 8.1.9 can be referred to for detailed descriptions).

ADDRESS	A23-16	A15-12	A11-10	A9-0
Security Register #1	00h	0 0 0 1	0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0	Byte Address

Figure 9-58 Program Security Registers Instruction (SPI Mode only)



9.2.35 Read Security Registers (48h)

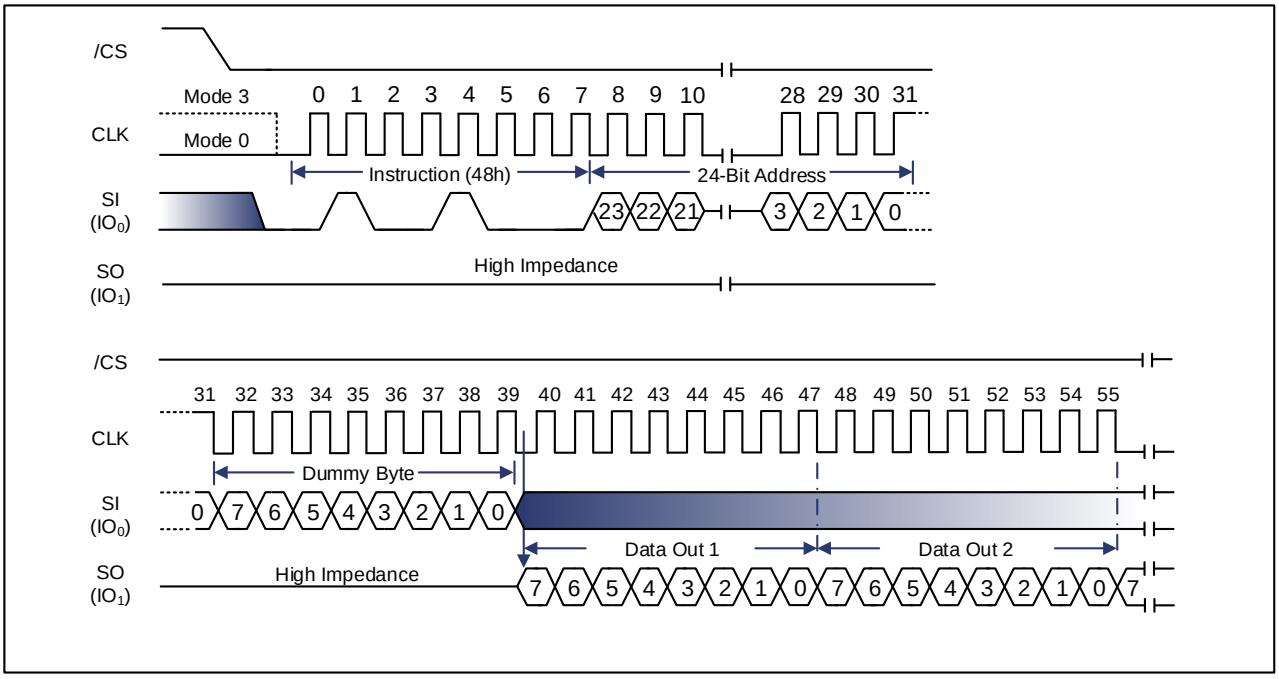
Working similarly as the Fast Read instruction, the Read Security Register instruction, allows one or more data Bytes to be sequentially read from one of the three security registers. The sequence of Read Security Register instruction is shown in Figure 9-59. The instruction sequence is initiated by driving the /CS pin low and then shifting the instruction code “48h”, followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the SI pin. The code and address bits are latched on the rising edge of the CLK pin. Upon receipt of the address, the data Byte of the addressed memory location will be shifted out first with the most significant bit (MSB) on the SO pin at the falling edge of CLK.

After each Byte of data has been shifted out, the Byte address is automatically added to the address of the next Byte. Once the Byte address reaches the last Byte of the register (Byte address 3FFh), it is reset to address 00h, the first Byte of the register, and continue to increment. This instruction is completed by driving /CS high. If this instruction is issued during an Erase, Program or Write cycle is in process (BUSY=1), it is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock rates to be varied from D.C. to a maximum of FR (as indicated by the Electrical Characteristics of AC).

ADDRESS	A23-16	A15-12	A11-10	A9-0
Security Register #1	00h	0 0 0 1	0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0	Byte Address

Note: If the 24-bit address (A23-A0) out of the table, the data of the addressed memory location will always be FFh.

Figure 9-59 Read Security Regis444ters Instruction (SPI Mode only)



9.2.36 Set Read Parameters (C0h)

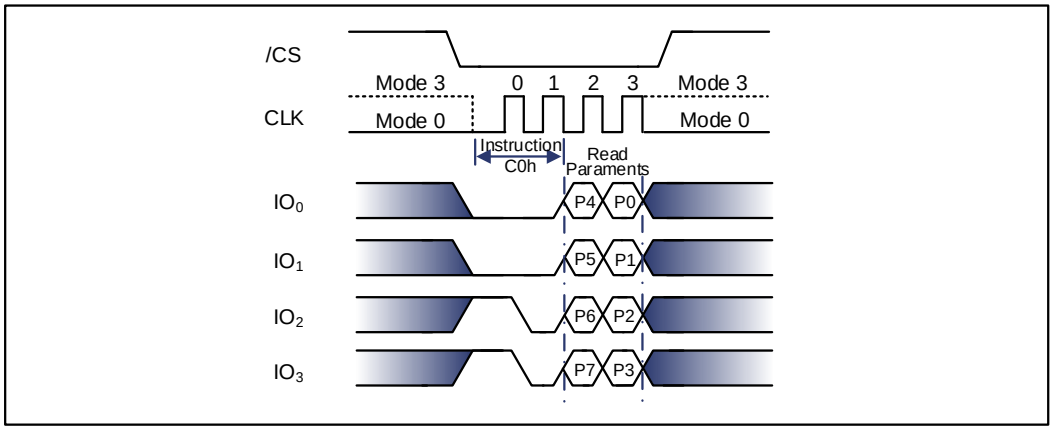
In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” instruction can be adopted to configure the number of dummy clocks for “Fast Read (0Bh)”, “Fast Read Quad I/O (EBh)” and “Burst Read with Wrap (0Ch)” instructions, and the number of "Wrap Length" Bytes for the "Burst Read with Wrap (0Ch)" instruction can be configured.

In Standard SPI mode, the “Set Read Parameters (C0h)” instruction is not accepted. In Standard/Dual/Quad SPI mode, the dummy clocks for various Fast Read instruction are set in Dummy Cycle Bits, Status register 3 can be referred to for more details. The “Wrap Length” is set by W5-4 bit in the “Set Burst with Wrap (77h)” instruction.

After a Power-Up or Reset instruction, the default "Wrap Length" is 8 Bytes and the default number of dummy clocks is 4 for STR, 10 for DTR. The number of dummy clocks is only programmable for “Fast Read (0Bh/0Dh)”, “Fast Read Quad I/O (EBh/EDh)” and “Burst Read with Wrap (0Ch/0Eh)” instructions in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks should be set again before any 0B/0Dh, EB/EDh or 0C/0Eh instructions.

P5 – P4		STR Fast Read		DTR Fast Read		P1 – P0		Wrap Length
		Dummy Clocks	Max Read Freq	Dummy Clocks	Max Read Freq			
0	0	4	80MHz	10	166MHz	0	0	8-Byte
0	1	6	108MHz	4	80MHz	0	1	16-Byte
1	0	8	133MHz	6	108MHz	1	0	32-Byte
1	1	10	166MHz	8	133MHz	1	1	64-Byte

Figure 9-60 Set Read Parameters Instruction (QPI Mode only)

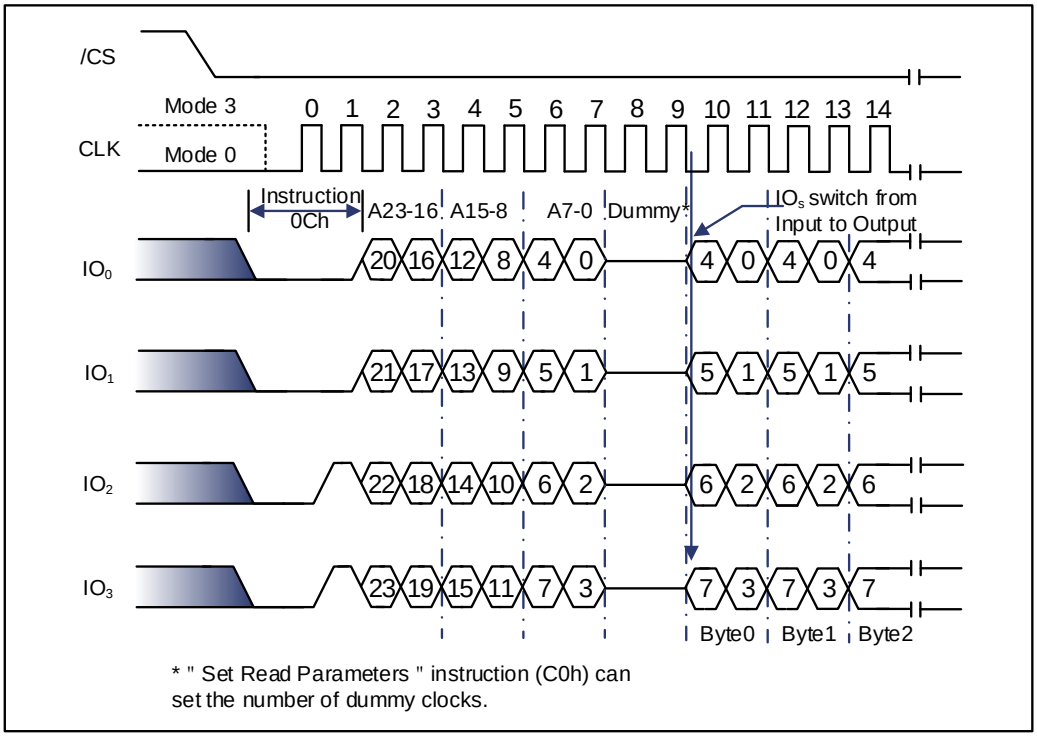


9.2.37 Burst Read with Wrap (0Ch)

The “Burst Read with Wrap (0Ch)” instruction provides an alternative way of performing a "Wrap Around" read operation in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except that once the end boundary is reached, the addressing of the read operation will "wrap around" to the start boundary of the "Wrap Length".

The “Wrap Length” and the number of dummy clocks can be configured with the “Set Read Parameters (C0h)” instruction.

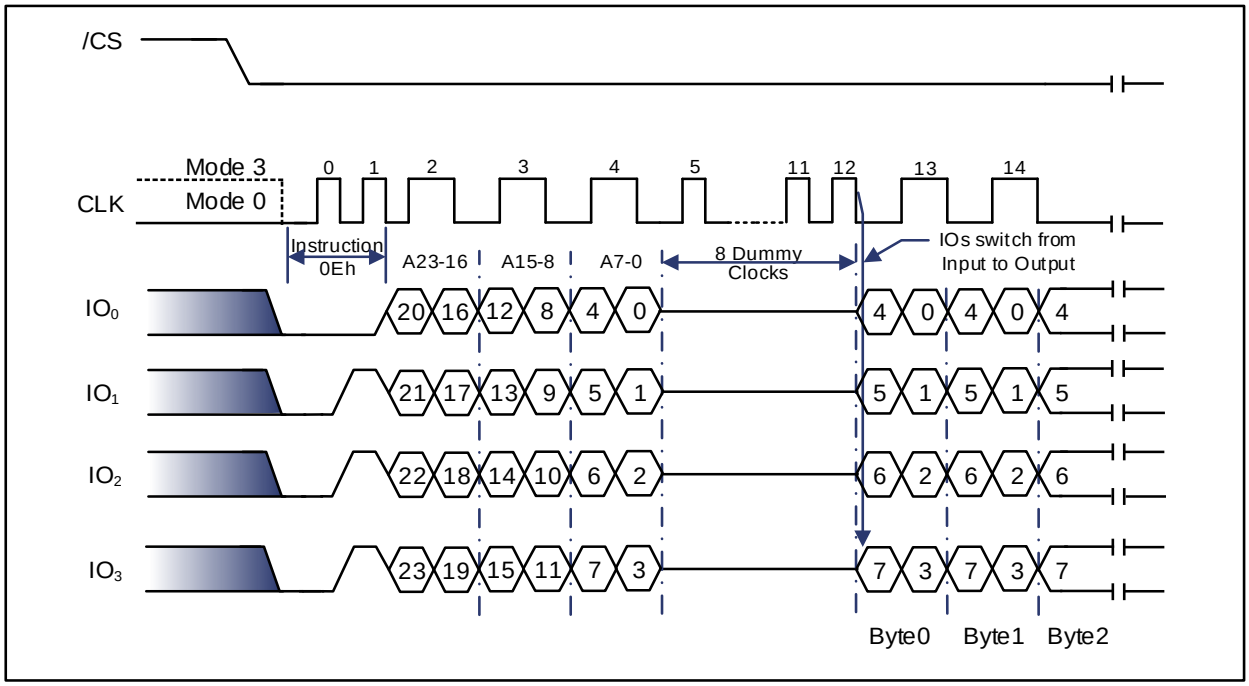
Figure 9-61 Burst Read with Wrap Instruction (QPI Mode only)



9.2.38 DTR Burst Read with Wrap (0Eh)

The “DTR Burst Read with Wrap (0Eh)” instruction presents an alternative method of performing a "Wrap Around" read operation in QPI mode. This instruction works similarly as the “Fast Read (0Bh)” instruction in QPI mode, except that once the end boundary is reached, the read operation is addressed "Wrap Around" to the start boundary of the "Wrap Length". The “Wrap Length” can be configured with the “Set Read Parameters (C0h)” instruction.

Figure 9-62 DTR Burst Read with Wrap Instruction (QPI Mode only)



9.2.39 Enter QPI Mode (38h) and Exit QPI Mode (FFh)

The XM25QH16D supports both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). The SPI mode and QPI mode are exclusive and the only way to switch the device from SPI mode to QPI mode is to execute the “Enter QPI (38h)” instruction.

The default state of the device upon is Standard/Dual/Quad SPI mode upon power-up. Before switching the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and the “Enter QPI (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI (38h)” instruction will be ignored and the device will remain in SPI mode. This provides full backward compatibility with previous generations of XMC serial flash memories.

Please refer to Command Set Table 1-3 for all the commands supported in QPI mode. When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status will remain unchanged, but the Wrap Length setting will reset to default. Instruction Set Table 3 can be referred to for all the commands supported in QPI mode.

The “Exit QPI (FFh)” instruction must be sent before exiting the QPI mode and returning to the Standard/Dual/Quad SPI mode. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Figure 9-63 Enter QPI Instruction (SPI Mode only)

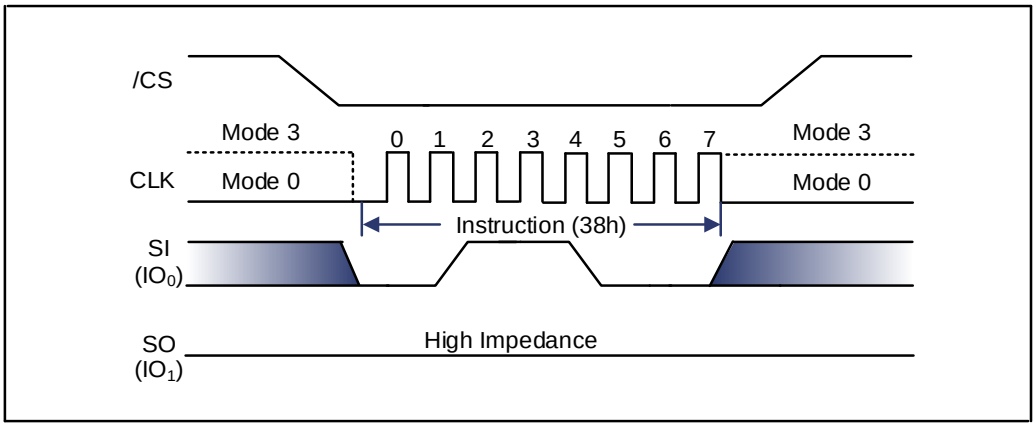
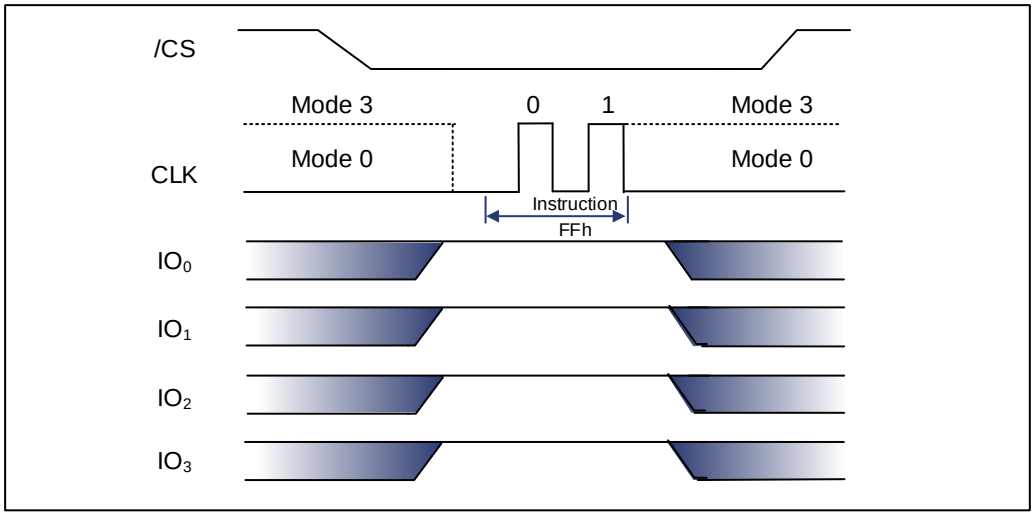


Figure 9-64 Exit QPI Instruction (QPI Mode only)



9.2.40 Enable Reset (66h) and Reset Device (99h)

Because of the small package and pin count limitations, the device provides a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0) and Wrap Bit setting (W6-W4) will be lost.

"Enable Reset (66h)" and "Reset (99h)" instructions can be issued in SPI mode or QPI mode. To avoid accidental reset, these two instructions must be initiated in sequence. Any instruction other than "Reset (99h)" after the "Enable Reset (66h)" command will disable the "Reset Enable" state. A new sequence of "Enable Reset (66h)" and "Reset (99h)" is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tSR to reset. During this period, no command will be accepted.

If there is an internal Erase or Program operation in progress or suspended while the device is receiving a Reset command sequence, data corruption may occur. It is recommended that the BUSY bit and SUS bit in the Status Register be checked before issuing a reset command sequence.

Figure 9-65 Enable Reset and Reset Instruction Sequence (SPI Mode)

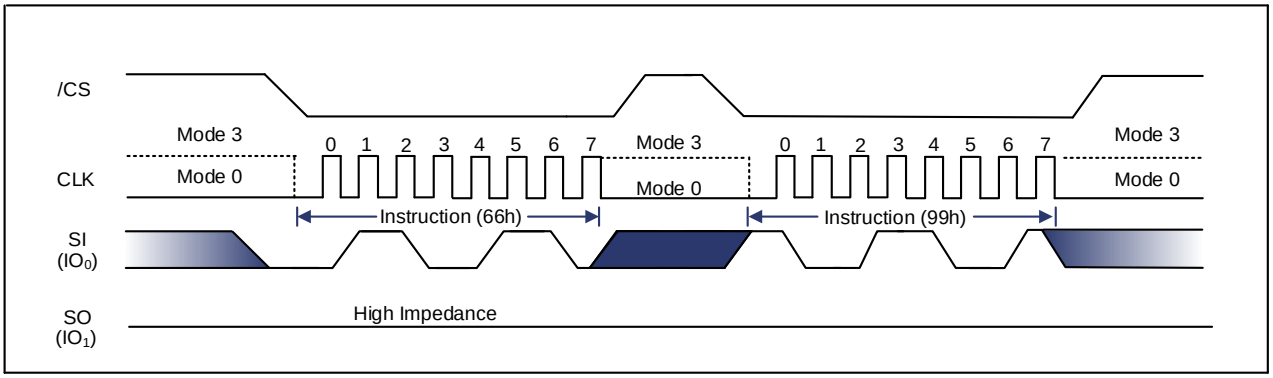
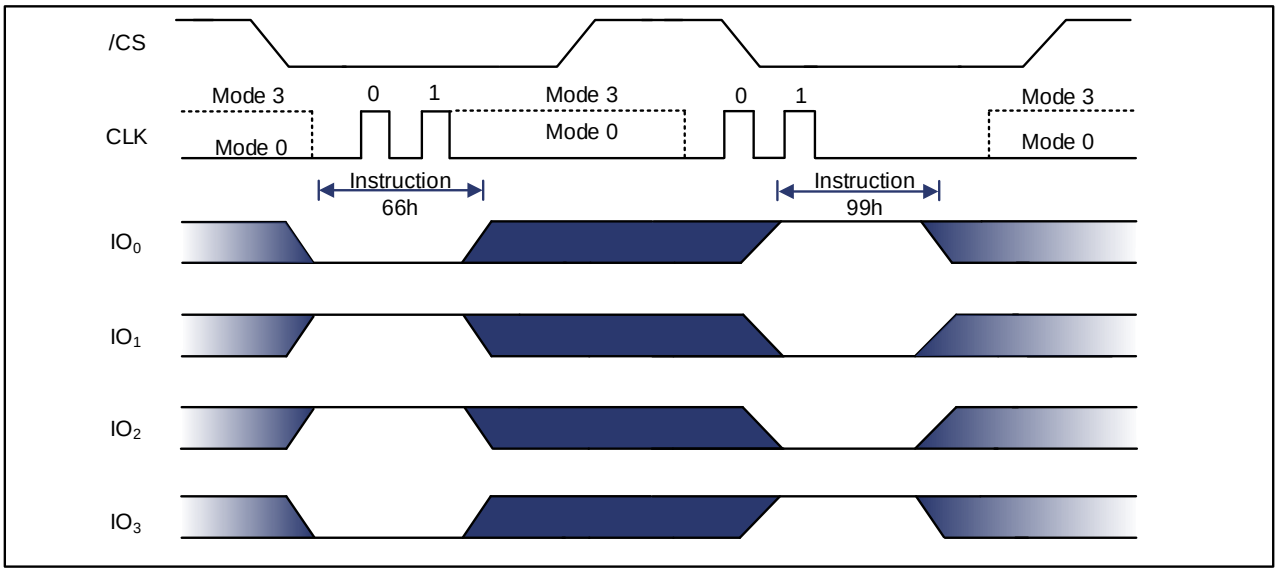


Figure 9-66 Enable Reset and Reset Instruction Sequence (QPI Mode)



10 ELECTRICAL CHARACTERISTICS

10.1 Operating Ranges[1]

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC	fc = 166MHz, fR = 108MHz	2.7	3.6	V
Supply Voltage	VCC	fc = 133MHz, fR = 80MHz	2.3	2.7	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C
		Industrial Plus	–40	+105	°C

Note:

[1] These parameters are characterized only

10.2 Absolute Maximum Ratings[1]

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to 4.6V	V
Transient Voltage on Any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.4	V
Electrostatic Discharge Voltage	VESD	Human Body Model[2]	–2000 to +2000	V
Storage Temperature	TSTG		–65 to +150	°C

Note:

[1] Stresses greater than those spec listed in the "Absolute Maximum Ratings" table may lead to permanent damage to the device. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage;

[2] JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms);

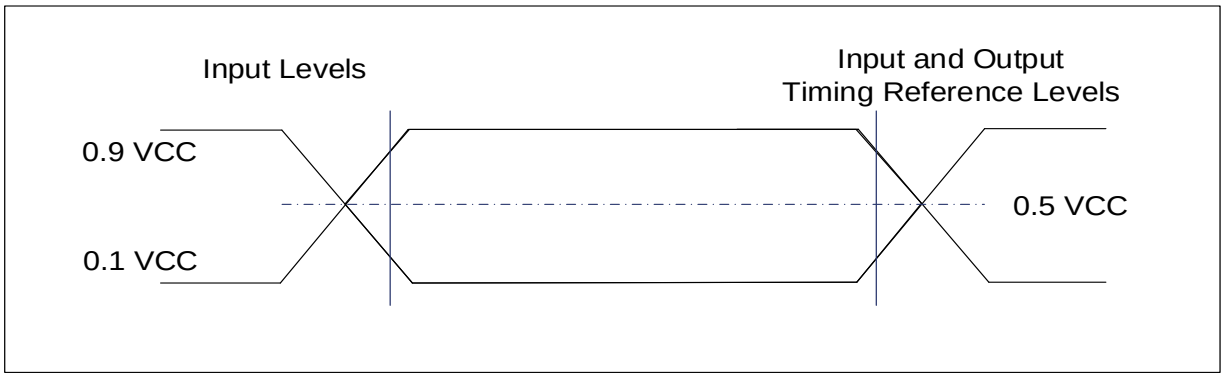
10.3 AC Measurement Conditions[1]

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	CL		30	pF
Input Rise and Fall Times	TR, TF		5	ns
Input Pulse Voltages	VIN	0.1 VCC to 0.9 VCC		V
Input Timing Reference Voltages	IN	0.3 VCC to 0.7 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC to 0.5 VCC		V

Note:

[1] Output Hi-Z is defined as the point where data out is no longer driven.

Figure 10-1 AC Measurement I/O Waveform



10.4 Capacitance

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Input Capacitance	CIN		6	pF
Output Capacitance	COUT		8	pF

10.5 Power-Up and Power-Down Timing[1]

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	tVSL	1.5		ms
Time Delay Before Write Instruction	tPUW	2		ms
Write Inhibit Voltage	VWI	1.5	2.3	V
The minimum duration for ensuring initialization will occur	tPWD	100		us
VCC voltage needed to below VPWD for ensuring initialization will occur	VPWD		1	V

Note:

[1] *These parameters are characterized only.*

Figure 10-2 Power-up Timing and Voltage Levels

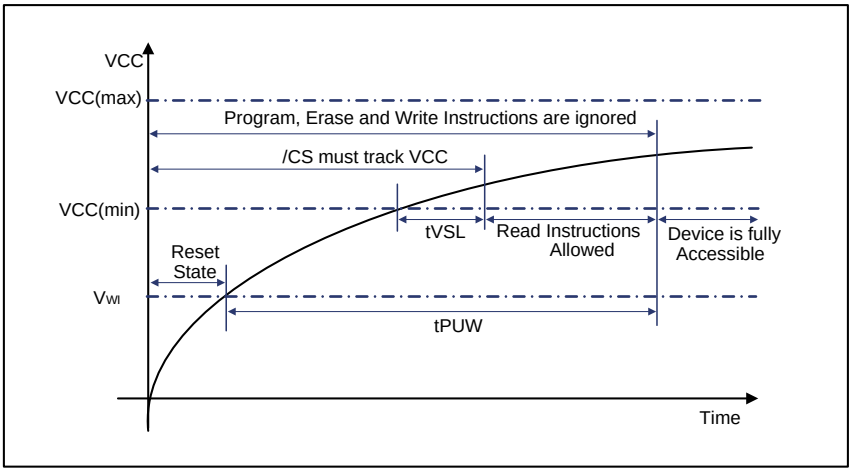
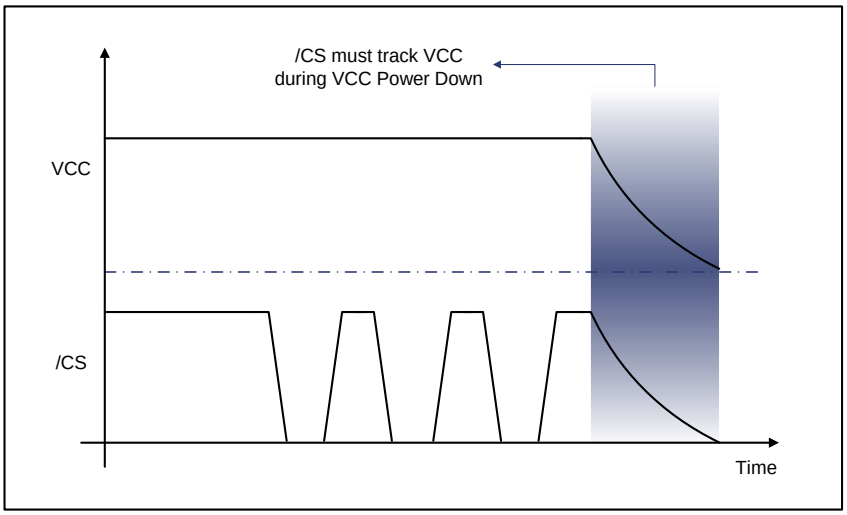


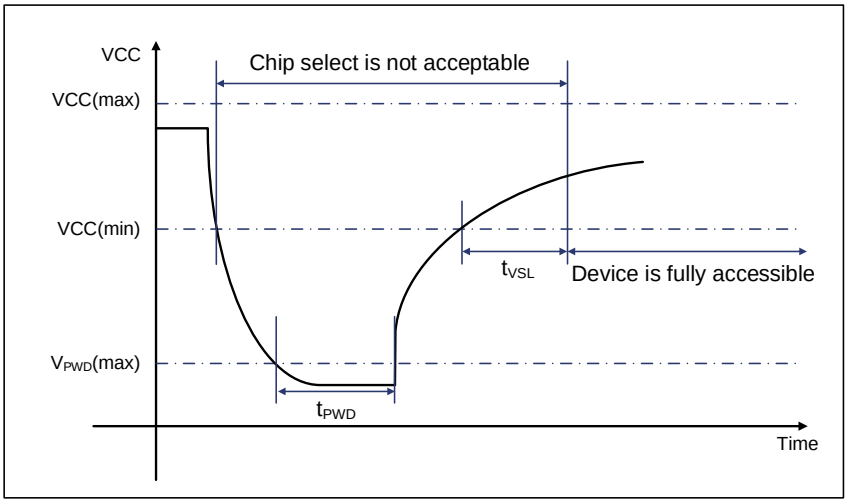
Figure 10-3 Power-Down Timing



Power Down Requirement

During Power-down, the system must initialize the power-up procedure only when Vcc drops below VPWD and hold a tPWD for the device to initialize correctly.

Figure 10-4 Power-Down and Power-up Requirement



10.6 DC Electrical Characteristics[1]

(-40~85℃)

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Leakage	ILI				±2	μA
I/O Leakage	ILO				±2	μA
Standby Current	ICC1	/CS = VCC, VIN = GND or VCC		10	30	μA
Power-down Current	ICC2	/CS = VCC, VIN = GND or VCC		0.2	10	μA
Operating Current (Read) [1]	ICC3	CLK=0.1VCC/0.9VCC at 166MHz, Q=Open (x4 I/O)		6	18	mA
		CLK=0.1VCC/0.9VCCat 80MHz, Q=Open (x4 I/O)		3	10	mA
		CLK=0.1VCC/0.9VCC at 80MHz, Q=Open (x4 I/O) DTR		5	15	mA
Operating Current (PP)	ICC5	/CS = VCC		7	15	mA
Operating Current (WRSR)	ICC6	/CS = VCC		4	12	mA
Operating Current (SE,BE)	ICC7	/CS = VCC		7	15	mA
Operating Current (CE)	ICC7	/CS = VCC		6	15	mA
Input Low Voltage	VIL		–0.5		VCC x 0.3	V
Input High Voltage	VIH		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	VOL	IOL = 100 μA			0.2	V
Output High Voltage	VOH	IOH = –100 μA	VCC – 0.2			V

Note:

[1] *0XFF Pattern.*

(-40~105℃)

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Leakage	ILI				±2	μA
I/O Leakage	ILO				±2	μA
Standby Current	ICC1	/CS = VCC, VIN = GND or VCC		10	40	μA
Power-down Current	ICC2	/CS = VCC, VIN = GND or VCC		0.2	15	μA
Operating Current (Read) [1]	ICC3	CLK=0.1VCC/0.9VCC at 166MHz, Q=Open (x4 I/O)		6	18	mA
		CLK=0.1VCC/0.9VCCat 80MHz, Q=Open (x4 I/O)		3	10	mA
		CLK=0.1VCC/0.9VCC at 80MHz, Q=Open (x4 I/O) DTR		5	15	mA
Operating Current (PP)	ICC5	/CS = VCC		7	15	mA
Operating Current (WRSR)	ICC6	/CS = VCC		4	12	mA
Operating Current (SE,BE)	ICC7	/CS = VCC		7	15	mA
Operating Current (CE)	ICC7	/CS = VCC		6	15	mA
Input Low Voltage	V_{IL}		–0.5		VCC x 0.3	V
Input High Voltage	V_{IH}		VCC x 0.7		VCC + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 μA			0.2	V
Output High Voltage	V_{OH}	I_{OH} = –100 μA	VCC – 0.2			V

Notes:

[1] *0XFF Pattern.*

10.7 AC Electrical Characteristics [5]

(-40~85℃)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Serial Clock Frequency For: all commands except Read (03H) and DTR instructions (2.7~3.6V)	fc	fC1	D.C.		166[1]	MHz
Serial Clock Frequency For: all commands except Read (03H) and DTR instructions (2.3~2.7V)	fc	fC1	D.C.		133[1]	MHz
Serial Clock Frequency For: DTR instructions(2.7~3.6V)	FR	fC2	D.C		166[1]	MHz
Serial Clock Frequency For: DTR instructions(2.3~2.7V)	FR	fC2	D.C		133[1]	MHz
Serial Clock Frequency For: Read (03H) (2.7~3.6V)	fR		D.C.		108	MHz
Serial Clock Frequency For: Read (03H) (2.3~2.7V)	fR		D.C.		80	MHz
Clock High, Low Time	tCLH, tCLL[1]		45% PC			ns
Serial Clock Rise Time (Slew Rate)	tCLCH[3]		0.1			V/ns
Serial Clock Fall Time (Slew Rate)	tCHCL[3]		0.1			V/ns
/CS Active Setup Time relative to CLK	tSLCH	tCSS	5			ns
/CS Not Active Hold Time relative to CLK	tCHSL		5			ns
Data In Setup Time	tDVCH	tDSU	2			ns
Data In Hold Time	tCHDX	tDH	3			ns
/CS Active Hold Time relative to CLK	tCHSH		5			ns
/CS Not Active Setup Time relative to CLK	tSHCH		5			ns
/CS Deselect Time (for Read)	tSHSL1	tCSH	7			ns
/CS Deselect Time (for Erase or Program or write)	tSHSL2	tCSH	30			ns
Output Disable Time	tSHQZ[3]	tDIS			6	ns
Clock Low to Output Valid for 30pF	tCLQV	tV			7	ns
Clock Low to Output Valid for 15pF	tCLQV	tV			6	ns
Output Hold Time	tCLQX	tHO	1			ns
/HOLD Active Setup Time relative to CLK	tHLCH		5			ns
/HOLD Active Hold Time relative to CLK	tCHHH		5			ns
/HOLD Not Active Setup Time relative to CLK	tHHCH		5			ns
/HOLD Not Active Hold Time relative to CLK	tCHHL		5			ns

Continued – next page AC Electrical Characteristics (cont'd)

AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD to Output Low-Z	tHHQX[3]	tLZ			6	ns
/HOLD to Output High-Z	tHLQZ[3]	tHZ			6	ns
Write Protect Setup Time Before /CS Low	tWHSL[4]		20			ns
Write Protect Hold Time After /CS High	tSHWL[4]		100			ns
/CS High to Power-down Mode	tDP[3]				3	µs
/CS High to Standby Mode without ID Read	tRES1[3]				20	µs
/CS High to Standby Mode with ID Read	tRES2[4]				20	µs
/CS High to next Instruction after Suspend	tSUS[3]				22	µs
Latency Between Resume And Next Suspend	tERS[2]		50			µs
/RESET pin Low period to reset the device	tRESET[3] [5]]		1			µs
Write Status Register Time	tW			2	15	ms
Page Program Time	tPP[8]			0.2	2	ms
Sector Erase Time (4KB)	tSE			25	300	ms
Block Erase Time (32KB)	tBE1			50	800	ms
Block Erase Time (64KB)	tBE2			90	1000	ms
Chip Erase Time	tCE [7]			2 [7]	10	s
Reset Latency(BUSY = write operation)	t_{SR}				28	µs
Reset Latency(BUSY = read operation)	t_{SR}				0.3	µs
Reset Latency(BUSY = erase operation)	t_{SR}				12	ms

Note:

[1] For 4 I/O command, the start alignment address should keep [A1,A0]=(0,0);

[2] Clock high or Clock low must be more than or equal to 45% Pc. Pc=1/fc(max);

[3] Value guaranteed by design and/or characterization, not 100% tested in production;

[4] Only applicable as a constraint for a Write Status Register instruction when SRP[1:0]=(0,1);

[5] It's possible to reset the device with shorter tRESET (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation;

[6] The 4-Bytes address alignment for Dual/Qual IO read with default dummy;

[7] For Blank Flash (FFh pattern), the chip erase typical time will be 0.5s.

[8] For 2.7V~3.6V: 0.2ms, 2.3V~2.7V: 0.3ms.

(-40~105℃)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Serial Clock Frequency For: all commands except Read (03H) and DTR instructions (2.7~3.6V)	fc	fC1	D.C.		166[1]	MHz
Serial Clock Frequency For: all commands except Read (03H) and DTR instructions (2.3~2.7V)	fc	fC1	D.C.		133[1]	MHz
Serial Clock Frequency For: DTR instructions(2.7~3.6V)	FR	fC2	D.C		166[1]	MHz
Serial Clock Frequency For: DTR instructions(2.3~2.7V)	FR	fC2	D.C		133[1]	MHz
Serial Clock Frequency For: Read (03H) (2.7~3.6V)	fR		D.C.		108	MHz
Serial Clock Frequency For: Read (03H) (2.3~2.7V)	fR		D.C.		80	MHz
Clock High, Low Time	tCLH, tCLL[2]		45% PC			ns
Serial Clock Rise Time (Slew Rate)	tCLCH[3]		0.1			V/ns
Serial Clock Fall Time (Slew Rate)	tCHCL[3]		0.1			V/ns
/CS Active Setup Time relative to CLK	tSLCH	tCSS	5			ns
/CS Not Active Hold Time relative to CLK	tCHSL		5			ns
Data In Setup Time	tDVCH	tDSU	2			ns
Data In Hold Time	tCHDX	tDH	3			ns
/CS Active Hold Time relative to CLK	tCHSH		5			ns
/CS Not Active Setup Time relative to CLK	tSHCH		5			ns
/CS Deselect Time (for Read)	tSHSL1	tCSH	7			ns
/CS Deselect Time (for Erase or Program or write)	tSHSL2	tCSH	30			ns
Output Disable Time	tSHQZ[3]	tDIS			6	ns
Clock Low to Output Valid for 30pF	tCLQV	tV			7	ns
Clock Low to Output Valid for 15pF	tCLQV	tV			6	ns
Output Hold Time	tCLQX	tHO	1			ns
/HOLD Active Setup Time relative to CLK	tHLCH		5			ns
/HOLD Active Hold Time relative to CLK	tCHHH		5			ns
/HOLD Not Active Setup Time relative to CLK	tHHCH		5			ns
/HOLD Not Active Hold Time relative to CLK	tCHHL		5			ns

Continued – next page AC Electrical Characteristics (cont'd)

AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD to Output Low-Z	tHHQX[3]	tLZ			6	ns
/HOLD to Output High-Z	tHLQZ[3]	tHZ			6	ns
Write Protect Setup Time Before /CS Low	tWHSL[4]		20			ns
Write Protect Hold Time After /CS High	tSHWL[4]		100			ns
/CS High to Power-down Mode	tDP[3]				3	µs
/CS High to Standby Mode without ID Read	tRES1[3]				20	µs
/CS High to Standby Mode with ID Read	tRES2[3]				20	µs
/CS High to next Instruction after Suspend	tSUS[3]				22	µs
Latency Between Resume And Next Suspend	tERS[2]		50			µs
/RESET pin Low period to reset the device	tRESET[3] [5]		1			µs
Write Status Register Time	tW			2	15	ms
Page Program Time	tPP[8]			0.2	2	ms
Sector Erase Time (4KB)	tSE			25	300	ms
Block Erase Time (32KB)	tBE1			50	800	ms
Block Erase Time (64KB)	tBE2			90	1000	ms
Chip Erase Time	tCE			2[7]	10	s
Reset Latency(BUSY = write operation)	t_{SR}				28	µs
Reset Latency(BUSY = read operation)	t_{SR}				0.3	µs
Reset Latency(BUSY = erase operation)	t_{SR}				12	ms

Note:

[1] For 4 I/O command, the start alignment address should keep [A1,A0]=(0,0);

[2] Clock high or Clock low must be more than or equal to 45% Pc. Pc=1/fc(max);

[3] Value guaranteed by design and/or characterization, not 100% tested in production;

[4] Only applicable as a constraint for a Write Status Register instruction when SRP[1:0]=(0,1);

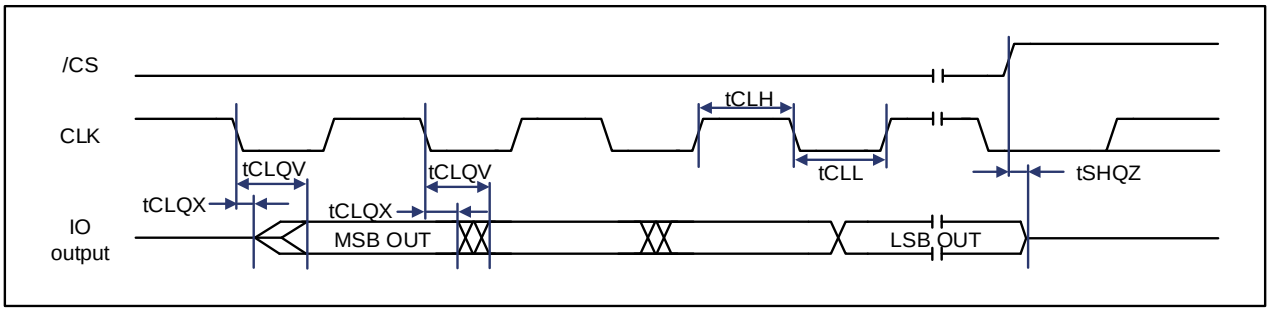
[5] It's possible to reset the device with shorter tRESET (as short as a few hundred ns), a 1us minimum is recommended to ensure reliable operation;

[6] The 4-Bytes address alignment for Dual/Qual IO read with default dummy;

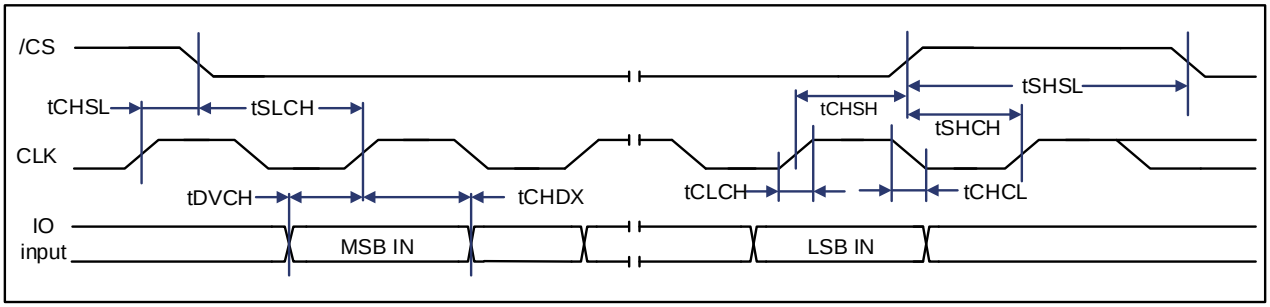
[7] For Blank Flash (FFh pattern),the chip erase typical time will be 0.5s.

[8] For 2.7V~3.6V: 0.2ms, 2.3V~2.7V: 0.3ms.

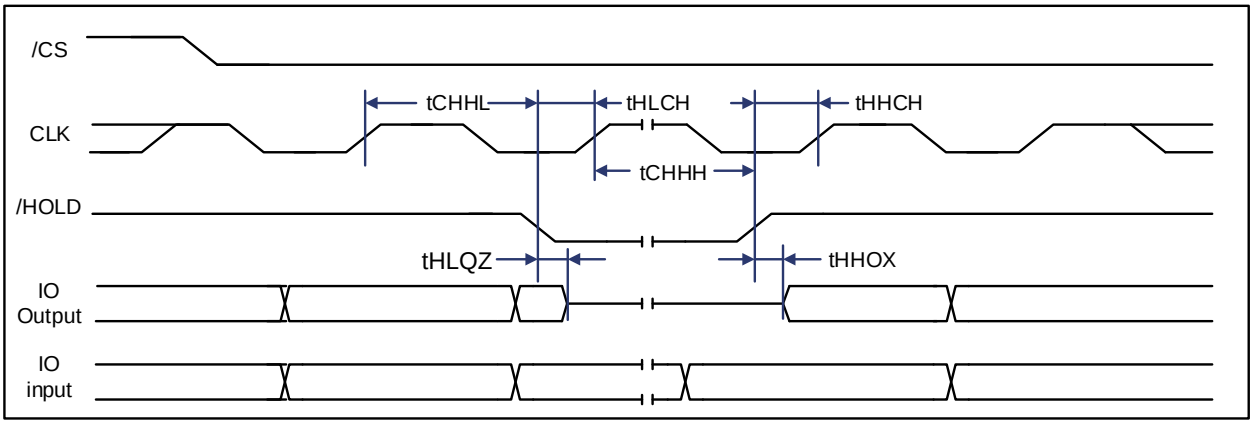
10.8 Serial Output Timing



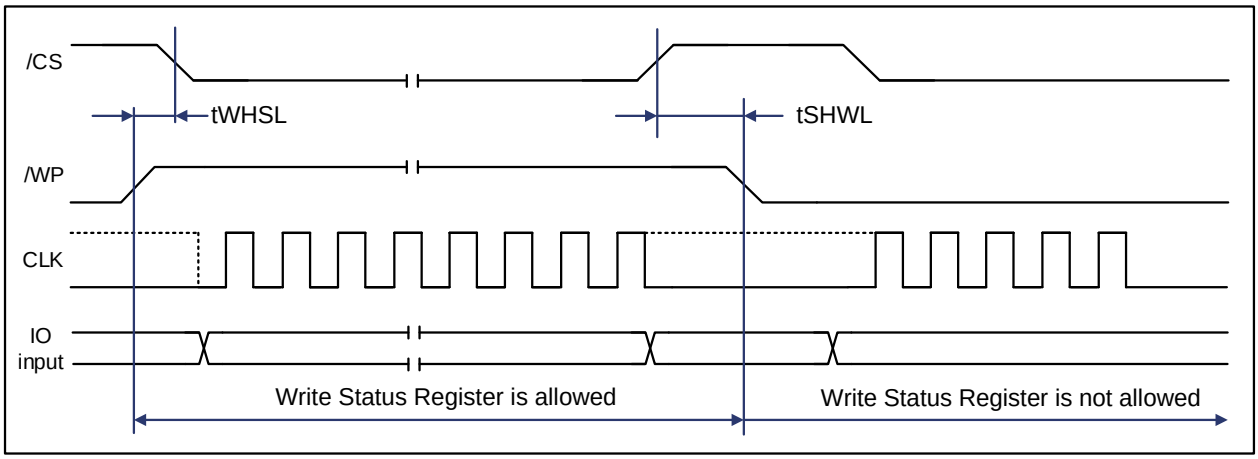
10.9 Serial Input Timing



10.10 /HOLD Timing

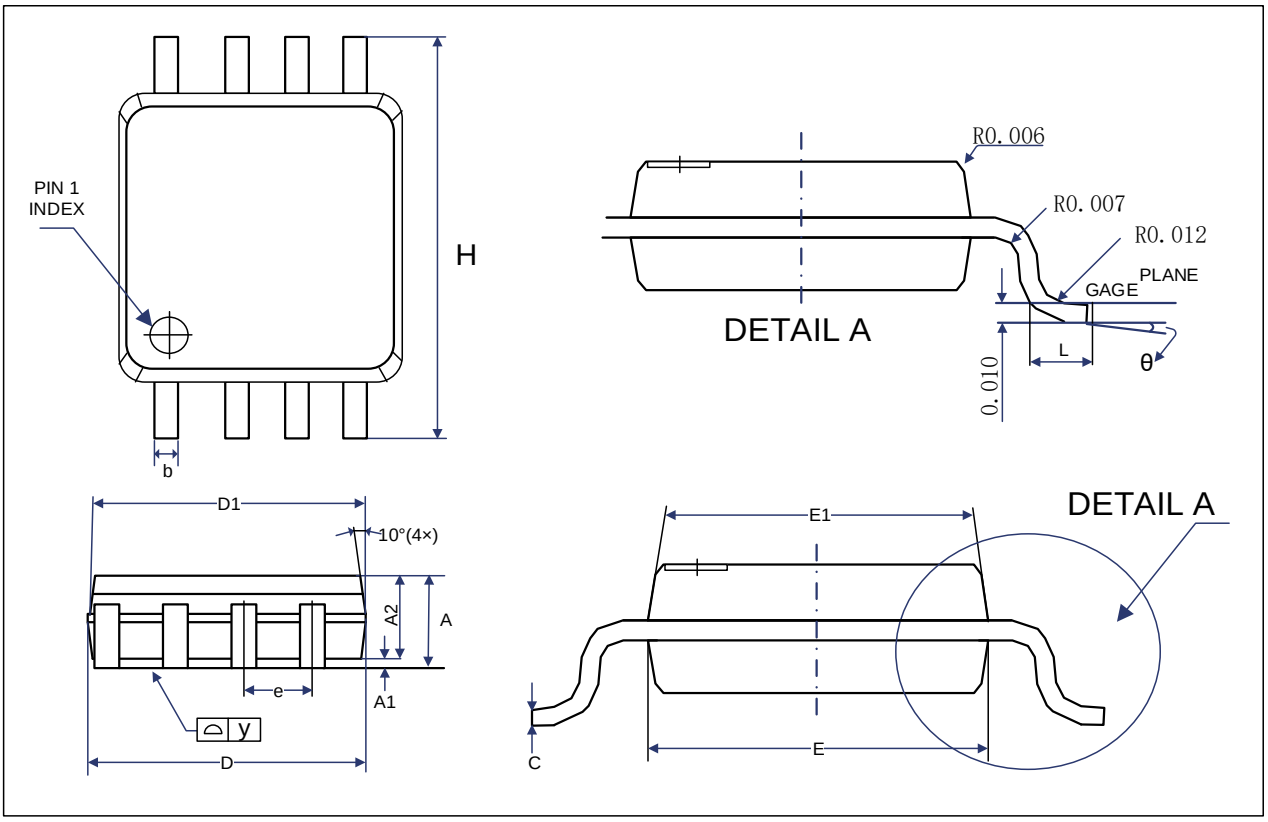


10.11 /WP Timing



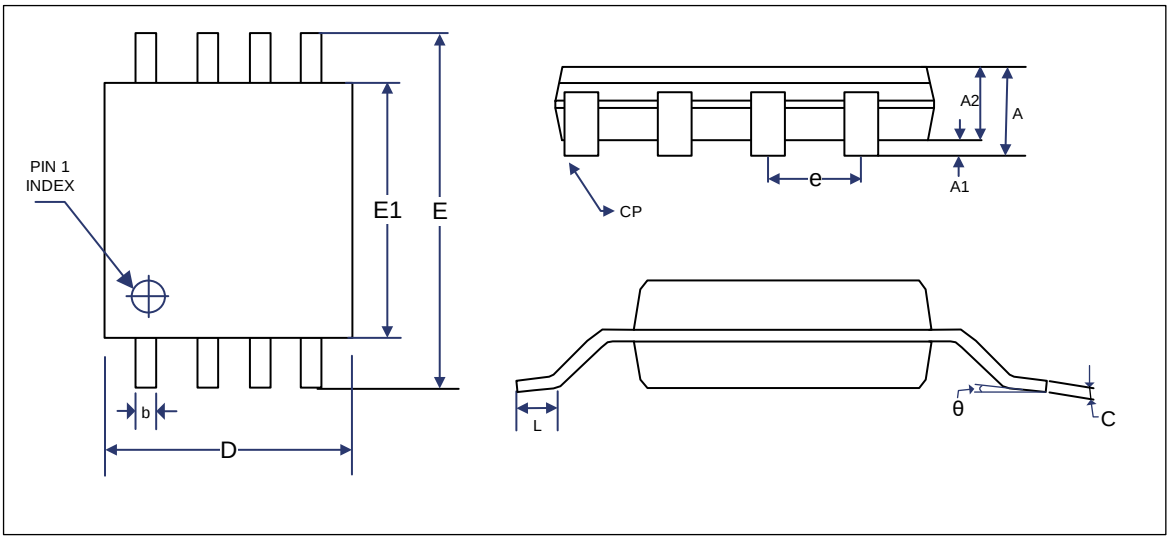
11 PACKAGE SPECIFICATIONS

11.1 SOP 208mil 8L (Package Code H)



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	1.75	1.95	2.16	0.069	0.077	0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
b	0.33	0.42	0.51	0.013	0.017	0.020
C	0.17	0.21	0.25	0.007	0.008	0.010
D	5.13	5.25	5.38	0.202	0.207	0.212
D1	5.07	5.23	5.38	0.200	0.206	0.212
E	5.13	5.25	5.38	0.202	0.207	0.212
E1	5.12	5.25	5.38	0.202	0.207	0.212
e	1.27 BSC			0.05 BSC		
H	7.70	7.90	8.10	0.303	0.311	0.319
L	0.50	0.65	0.80	0.020	0.026	0.031
y	---	---	0.1	---	---	0.004
θ	0°	---	8°	0°	---	8°

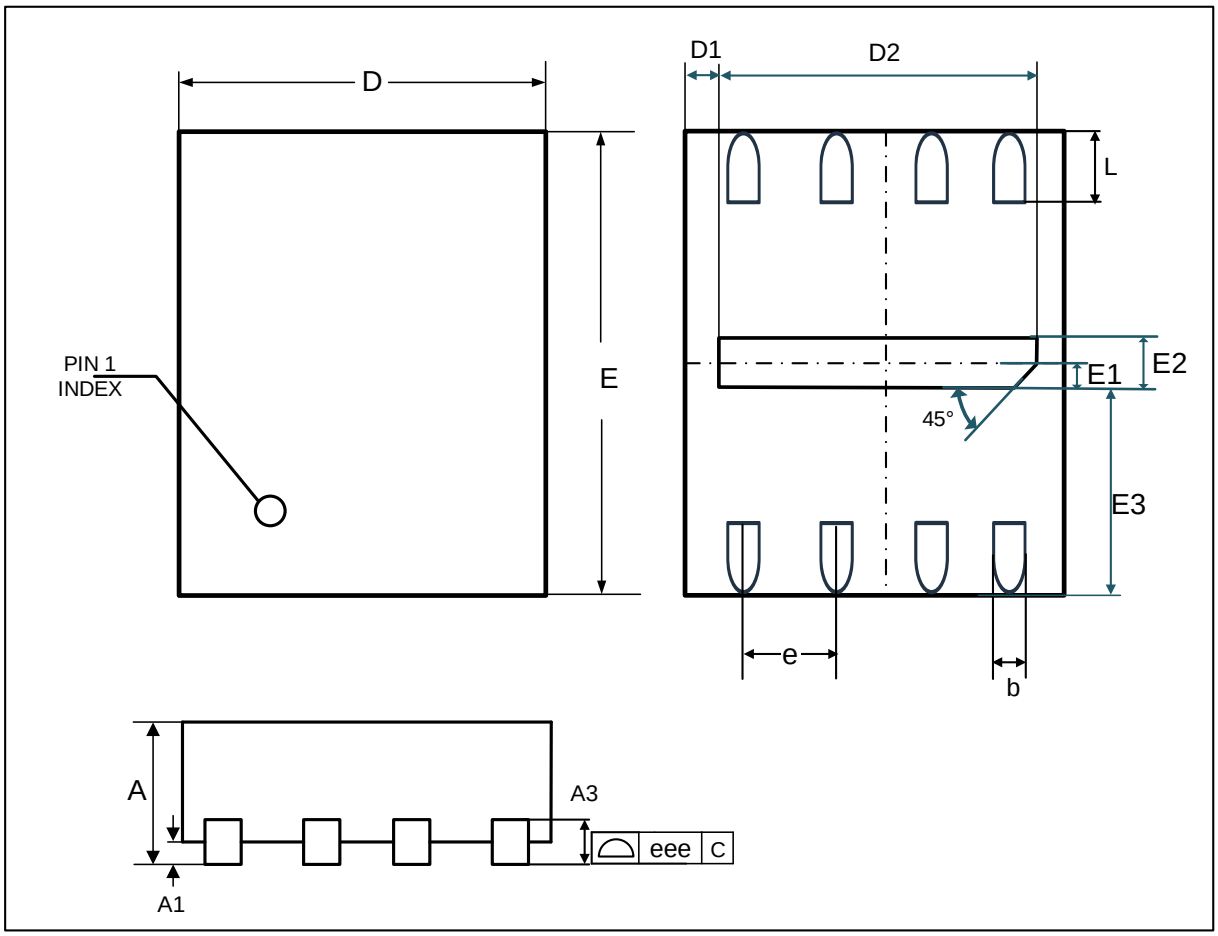
11.2 SOP 150mil 8L (Package Code J)



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	1.25	1.45	1.55	0.049	0.057	0.061
b	0.31	---	0.51	0.012	---	0.020
C	0.17	---	0.25	0.007	---	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	6.00 BSC			0.236 BSC		
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
L	0.40	0.82	1.25	0.016	0.033	0.049
CP	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8

Note: Both the package length and width do not include the mold flash.

11.3 USON 2x3 8L (Package Code U)



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.4	0.48	0.55	0.016	0.019	0.022
A1	0	0.02	0.05	0	0.001	0.002
b	0.2	0.25	0.3	0.008	0.01	0.012
A3	---	0.152REF	---	---	0.006REF	---
D	1.9	2	2.1	0.114	0.118	0.122
D1	0.2			0.008		
D2	1.5	1.6	1.7	0.059	0.063	0.067
E	2.9	3	3.1	0.075	0.079	0.083
E1	0.00	0.10	0.20	0.000	0.004	0.008
E2	0.1	0.2	0.3	0.004	0.008	0.012
E3	1.4			0.055		
e	0.50BSC			0.020BSC		
L	0.35	0.45	0.55	0.014	0.018	0.022
C	0.00	---	0.08	0	---	0.003

12 REVISION LIST

Revision NO	DESCRIPTION	Date
0.1	Preliminary version	2022/11/04
0.5	Add USON 2*3 package	2024/8/19
1.0	Update SFDP 56-58h and 5Bh in P68 and Modify Read performance Comparison Table in P6/17/18	2025/01/15

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