DDR4 SDRAM

512 Mb x 16
DDR4 SDRAM

Feature

- V_{DD} = V_{DDQ} = 1.2V ±60mV
- V_{PP} = 2.5V, -125mV, +250mV
- On-die, internal, adjustable V_{REFDQ} generation
- 1.2V pseudo open-drain I/O
- Refresh time of 8192-cycle at T_C temperature range:
  - 64ms at 0°C to 85°C
  - 32ms at >85°C to 95°C
- 8 internal banks (x16): 2 groups of 4 banks each
- 8*n*-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)[1]
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test
- JEDEC JESD-79-4 compliant
- sPPR and hPPR capability
- MBIST-PPR support
- Operating case temperature range: T_C = 0°C to +95°C

Note: 1. Temperature controlled refresh (TCR) is not supported during extended temperature range (85°C to 95°C).

Table 1. Ordering Information

Product ID	Max Freq.	V_{DD}	Data Rate (CL-tRCD-tRP)	Package	Comments
M16U8G16512A-NLBG2C	1600 MHz	1.2V	DDR4- 3200 (22-22-22)	96 ball BGA	Pb-free
M16U8G16512A-JJBG2C	1333 MHz	1.2V	DDR4- 2666 (18-18-18)	96 ball BGA	Pb-free

Table 2. DDR4 SDRAM Addressing

Configuration		Device
Bank Address	Number of Bank Groups	2
	BG Address	BG0
	Bank count per group	4
	Bank address in bank group	BA[1:0]
Row addressing		64K (A[15:0])
Column addressing		1K (A[9:0])
Page size [*1]		2KB

Note:

1. Page size is per bank, calculated as follows:
   Page size = $2^{COLBITS}$ × ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.

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Figure 1. Pin Configuration – 96 balls BGA Package

< TOP View>

See the balls through the package

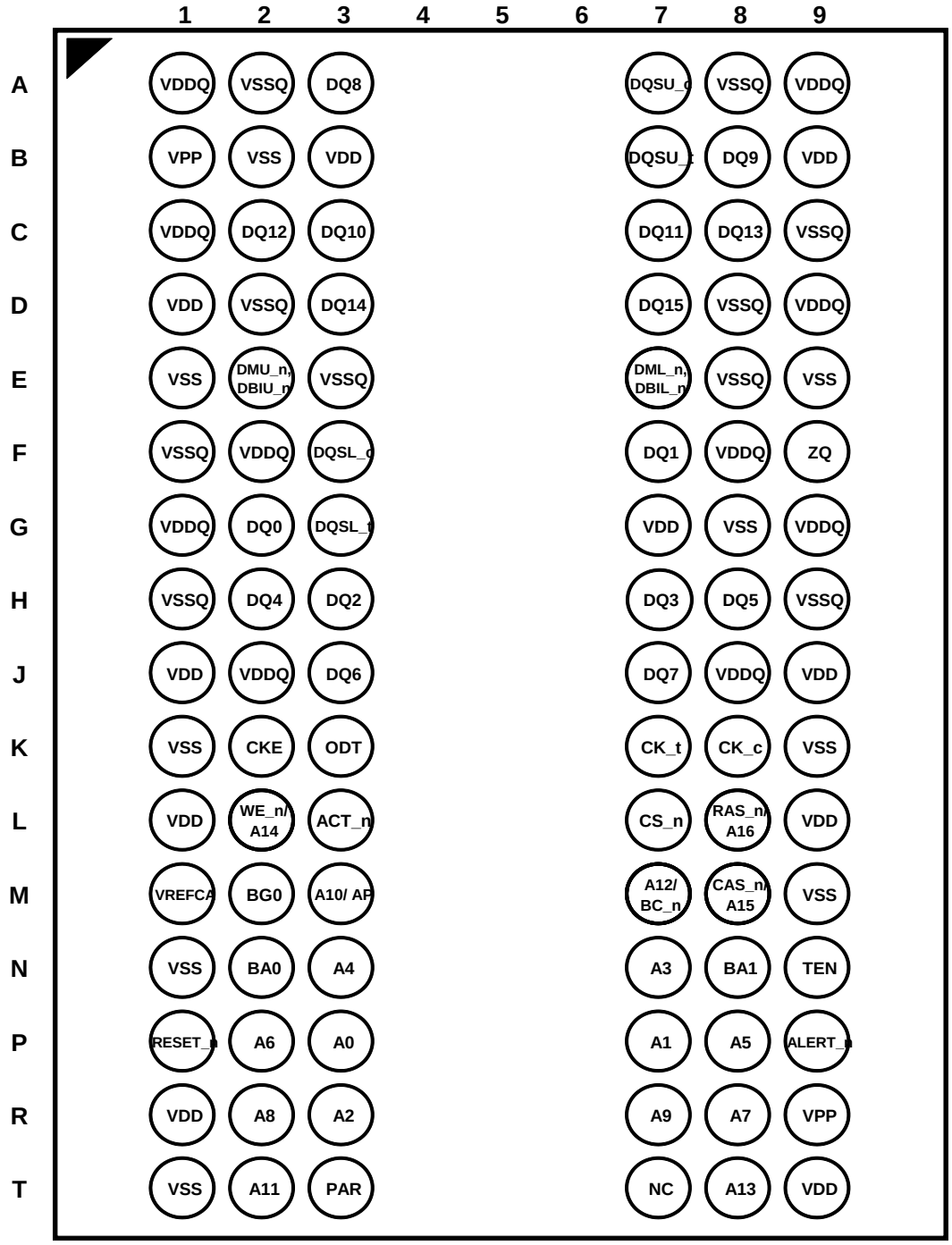


Table 3. Input / Output Functional Description

Symbol	Type	Function
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n	Input	**Chip Select:** All commands are masked when CS_n is registered high. CS_n provides for external rank selection on systems with multiple memory ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	**Chip ID:** Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU and DML signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	**Activation Command Input:** ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	**Command Inputs:** RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM, DBI, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/ Output	**Input Data Mask and Data Bus Inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5.
BG0 - BG1	Input	**Bank Group Inputs:** BG0 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0.
BA0 - BA1	Input	**Bank Address Inputs:** BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	**Address Inputs:** Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16,CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 connection is part-number specific; Contact vendor for more information.

Table 3. Input / Output Functional Description - Continued

Symbol	Type	Function
A10 / AP	Input	**Auto-precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	**Burst Chop:** A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	**Active Low Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
DQ	Input / Output	**Data Input/ Output:** Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, R_{TT} value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS (DQSL, DQSU) are paired with differential signals DQS_c, DQSL_c and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
PAR	Input	**Command and Address Parity Input:** DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1,A17-A0, and C0-C2 (3DS devices). Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK and whenCS_n is low.
ALERT_n	Input/output	**Alert:** It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	**Connectivity Test Mode Enable:** Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC	-	**No Connect:** No internal electrical connection is present.
VDDQ	Supply	**DQ Power Supply:** 1.2 V +/- 0.06V
VSSQ	Supply	**DQ Ground**
VDD	Supply	**Power Supply:** 1.2 V +/- 0.06V
VSS	Supply	**Ground**
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
VREFCA	Supply	**Reference voltage for CA**
ZQ	Supply	**Reference pin for ZQ calibration.**

Note: Input only pins (BG0, BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

General Notes and Description

Description

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM for the x16 configuration and as a 16-bank DRAM for the x4 and x8 configurations.

The DDR4 SDRAM uses an 8*n*-prefetch architecture to achieve high-speed operation. The 8*n*-prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins.

A single READ or WRITE operation for the DDR4 SDRAM consists of a single 8*n*-bit wide, four-clock data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation), unless specifically stated otherwise.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms "_t" and "_c" are used to represent the true and complement of a differential signal pair. These terms replace the previously used notation of "#" and/or overbar characters. For example, differential data strobe pair DQS, DQS# is now referred to as DQS_t, DQS_c.
- The term "_n" is used to represent a signal that is active LOW and replaces the previously used "#" and/or overbar characters. For example: CS# is now referred to as CS_n.
- The terms "DQS" and "CK" found throughout the data sheet are to be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the entire document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated here within is considered undefined, illegal, and not supported, and can result in unknown operation.
- Addressing is denoted as BG[*n*] for bank group, BA[*n*] for bank address, and A[*n*] for row/col address.
- The NOP command is not allowed, except when exiting maximum power savings mode or when entering gear-down mode, and only a DES command should be used.
- Not all features described within this document may be available on the Rev. A (first) version.
- Not all specifications listed are finalized industry standards; best conservative estimates have been provided when an industry standard has not been finalized.
- Although it is implied throughout the specification, the DRAM must be used after V_{DD} has reached the stable power-on level, which is achieved by toggling CKE at least once every 8192 x ^{t}REFI. However, in the event CKE is fixed HIGH, toggling CS_n at least once every 8192 x ^{t}REFI is an acceptable alternative. Placing the DRAM into self refresh mode also alleviates the need to toggle CKE.
- Not all features designated in the data sheet may be supported by earlier die revisions due to late definition by JEDEC.
- A x16 device's DQ bus is comprised of two bytes. If only one of the bytes needs to be used, use the lower byte for data transfers and terminate the upper byte as noted:
- Connect UDQS_t to V_{DDQ} or V_{SS}/ V_{SSQ} via a resistor in the 200Ω range.
- Connect UDQS_c to the opposite rail via a resistor in the same 200Ω range.
- Connect UDM to V_{DDQ} via a large (10,000Ω) pull-up resistor.
- Connect UDBI to V_{DDQ} via a large (10,000Ω) pull-up resistor.
- Connect DQ [15:8] individually to V_{DDQ} via a large (10,000Ω) resistors, or float DQ [15:8].

Definitions of the Device-Pin Signal Level

- HIGH: A device pin is driving the logic 1 state.
- LOW: A device pin is driving the logic 0 state.
- High-Z: A device pin is tri-state.
- ODT: A device pin terminates with the ODT setting, which could be terminating or tri-state depending on the mode register setting.

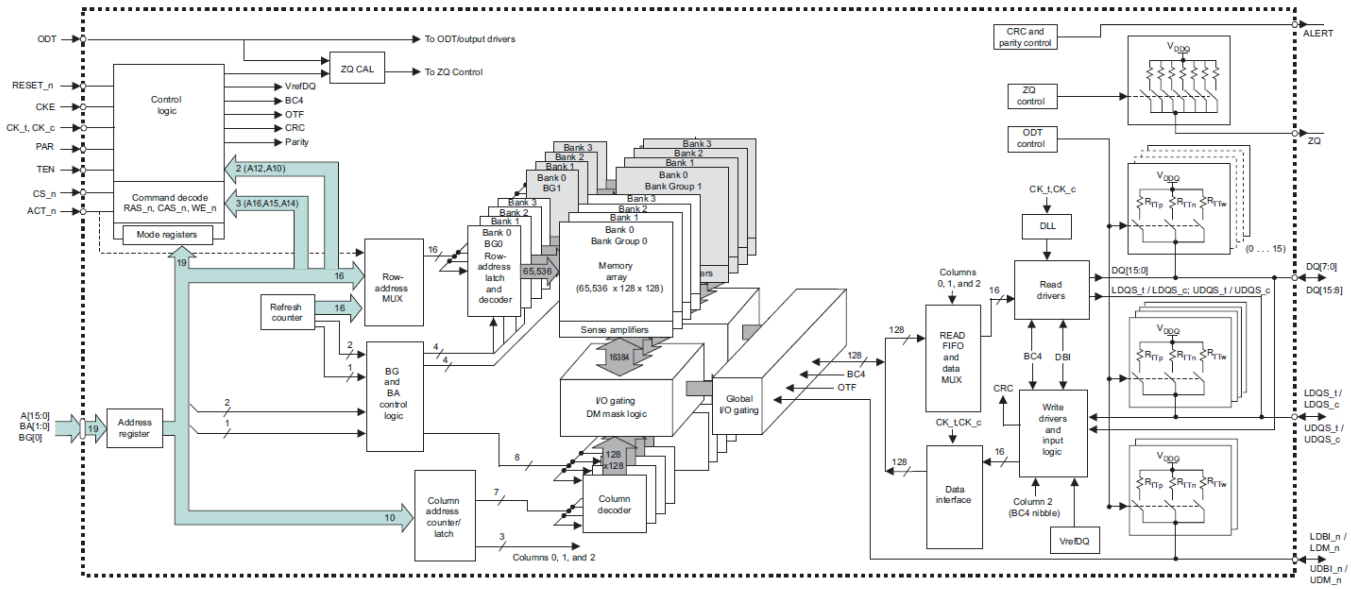
Definitions of the Bus Signal Level

- HIGH: One device on the bus is HIGH, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally V_{DDQ}.
- LOW: One device on the bus is LOW, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally $V_{OL(DC)}$ if ODT was enabled, or V_{SSQ} if High-Z.
- High-Z: All devices on the bus are High-Z. The voltage level on the bus is undefined as the bus is floating.
- ODT: At least one device on the bus is ODT, and all others are High-Z. The voltage level on the bus is nominally V_{DDQ}.
- The specification requires 8,192 refresh commands within 64ms between 0°C and 85°C. This allows for a ^{t}REFI of 7.8125µs (the use of "7.8µs" is truncated from 7.8125µs). The specification also requires 8,192 refresh commands within 32ms between 85oC and 95oC. This allows for a ^{t}REFI of 3.90625µs (the use of "3.9µs" is truncated from 3.90625µs).

Functional Block Diagrams

DDR4 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 16-bank (4-banks per Bank Group) DRAM.

Figure 2. 512 Meg x 16 Functional Block Diagram



State Diagram

This simplified state diagram provides an overview of the possible state transitions and the commands to control them. Situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

Figure 3. Simplified State Diagram

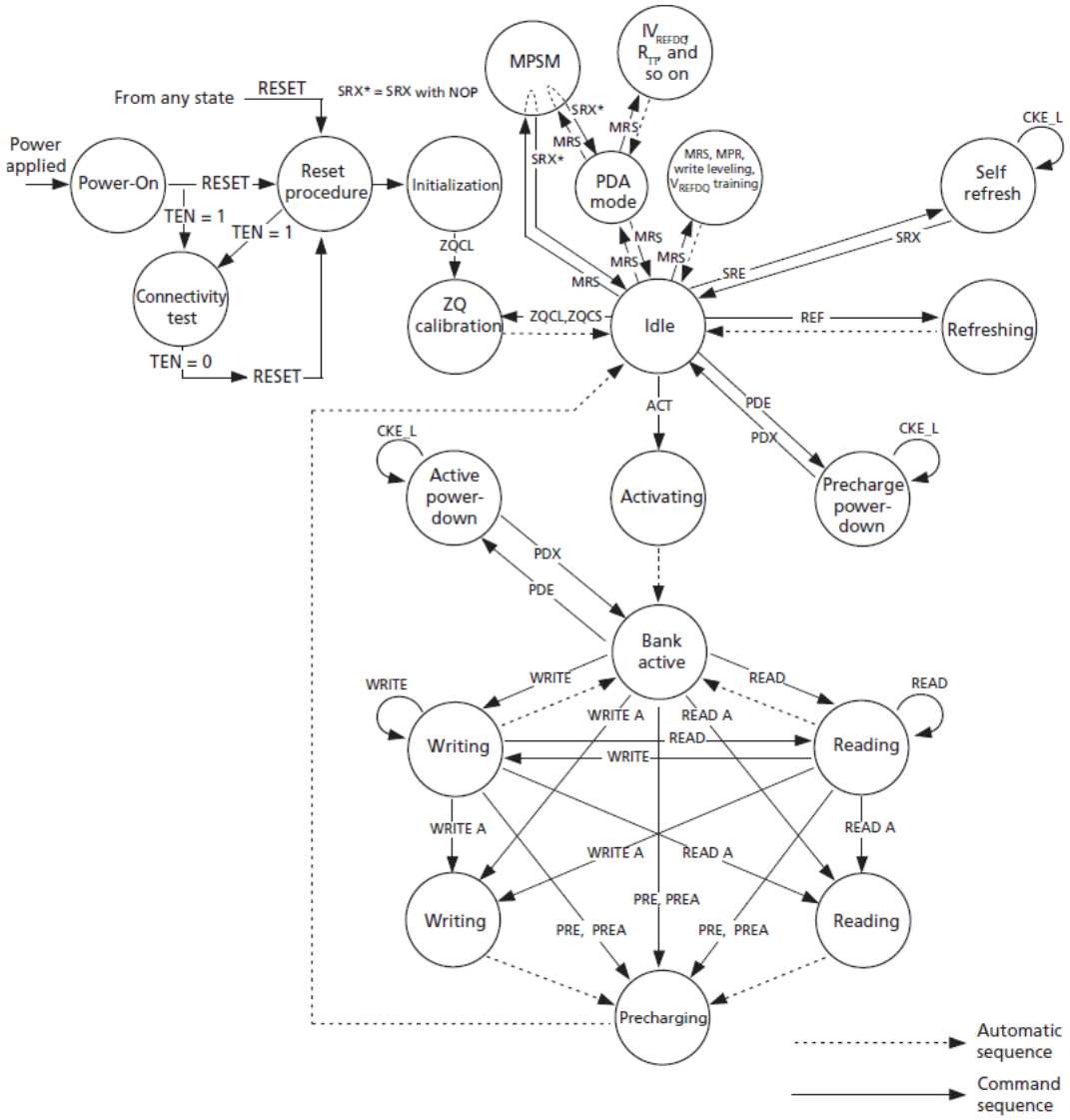


Table 4. State Diagram Command Definitions

Command	Description
ACT	Active
MPR	Multipurpose register
MRS	Mode register set
PDE	Enter power-down
PDX	Exit power-down
PRE	Precharge
PREA	Precharge all
READ	RD, RDS4, RDS8
READ A	RDA, RDAS4, RDAS8
REF	Refresh, fine granularity refresh
RESET	Start reset procedure
SRE	Self refresh entry
SRX	Self refresh exit
TEN	Boundary scan mode enable
WRITE	WR, WRS4, WRS8 with/without CRC
WRITE A	WRA, WRAS4, WRAS8 with/without CRC
ZQCL	ZQ calibration long
ZQCS	ZQ calibration short

Notes: 1. See the Command Truth Table for more details.

Functionality Description

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen banks (4 bank groups with 4 banks for each bank group) for x4/x8 devices, and as eight banks for each bank group (2 bank groups with 4 banks each) for x16 devices. The device uses double data rate (DDR) architecture to achieve high-speed operation. DDR4 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for a device module effectively consists of a single 8*n*-bit-wide, four-clock-cycle-data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the device are burst-oriented. Accesses start at a selected location and continue for a burst length of eight or a chopped burst of four in a programmed sequence. Operation begins with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BG[1:0] select the bank group for x4/x8, and BG0 selects the bank group for x16; BA[1:0] select the bank, and A[17:0] select the row. See the Addressing section for more details).

The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst operation, determine if the auto PRECHARGE command is to be issued (via A10), and select BC4 or BL8 mode on-the-fly (OTF) (via A12) if enabled in the mode register.

Prior to normal operation, the device must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

Note: The use of the NOP command is allowed only when exiting maximum power saving mode or when entering gear-down mode.

RESET and Initialization Procedure

To ensure proper device function, the power-up and reset initialization default values for the following mode register (MR) settings are defined as:

- Gear-down mode (MR3 A[3]): 0 = 1/2 rate
- Per-DRAM addressability (MR3 A[4]): 0 = disable
- Maximum power-saving mode (MR4 A[1]): 0 = disable
- CS to command/address latency (MR4 A[8:6]): 000 = disable
- CA parity latency mode (MR5 A[2:0]): 000 = disable
- Hard post package repair mode (MR4 A[13]): 0 = disable
- Soft post package repair mode (MR4 A[5]): 0 = disable

Power-up Initialization sequence

The Following sequence is required for power up and Initialization:

(1). Apply power (RESET_n and TEN should be maintained below 0.2 x V_{DD} while supplies ramp up; all other inputs may be undefined). When supplies have ramped to a valid stable level, RESET_n must be maintained below 0.2 x V_{DD} for a minimum of tPW_RESET_L and TEN must be maintained below 0.2 x V_{DD} for a minimum of 700 s. CKE is pulled LOW anytime before RESET_n is de-asserted (minimum time of 10ns). The power voltage ramp time between 300mV to $V_{DD,min}$ must be no greater than 200ms, and during the ramp, V_{DD} must be greater than or equal to V_{DDQ} and (V_{DD} - V_{DDQ}) < 0.3V. V_{PP} must ramp at the same time or up to 10 minutes prior to V_{DD}, and V_{PP} must be equal to or higher than V_{DD} at all times. The total time for which V_{PP} is powered and V_{DD} is unpowered should not exceed 360 cumulative hours. After V_{DD} has ramped and reached a stable level, RESET_n must go high within 10 minutes. After RESET_n goes high, the initialization sequence must be started within 3 seconds. For debug purposes, the 10 minute and 3 second delay limits may be extended to 60 minutes each provided the DRAM is operated in this debug mode for no more than 360 cumulative hours.

During power-up, the supply slew rate is governed by the limits stated in the table below and either condition A or condition B listed below must be met.

Table 5. Supply Power-up Slew Rate

Symbol	Min	Max	Unit	Comment
V_{DD}_SL, V_{DDQ}_SL, V_{PP}_SL	0.004	600	V/ms	Measured between 300mV and 80% of supply minimum
V_{DD}_ona	N/A	200	ms	V_{DD} maximum ramp time from 300mV to V_{DD} minimum
V_{DDQ}_ona	N/A	200	ms	V_{DDQ} maximum ramp time from 300mV to V_{DDQ} minimum

Note:

1. 20 MHz band-limited measurement.

- Condition A:
- Apply V_{PP} without any slope reversal before or at the same time as V_{DD} and V_{DDQ}.
- V_{DD} and V_{DDQ} are driven from a single-power converter output and apply V_{DD}/V_{DDQ} without any slope reversal before or at the same time as V_{TT} and V_{REFCA}.
- The voltage levels on all balls other than V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be greater than or equal to V_{SSQ} and V_{SS} on the other side.
- V_{TT} is limited to 0.76V MAX when the power ramp is complete.
- V_{REFCA} tracks V_{DD}/2.

- Condition B:
- Apply V_{PP} without any slope reversal before or at the same time as V_{DD}.
- Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}.
- Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} and V_{REFCA}.
- The voltage levels on all pins other than V_{PP}, V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.

(1). After RESET_n is de-asserted, wait for a minimum of 500µs, but no longer than 3 seconds, before allowing CKE to be registered HIGH at clock edge Td. During this time, the device will start internal state initialization; this will be done independently of external clocks. A reasonable attempt was made in the design to power up with the following default MR settings: gear-down mode (MR3 A[3]): 0 = 1/2 rate; per-DRAM addressability (MR3 A[4]): 0 = disable; maximum power-down (MR4 A[1]): 0 = disable; CS to command/address latency (MR4 A[8:6]): 000 = disable; CA parity latency mode (MR5 A[2:0]): 000 = disable. However, it should be assumed that at power up the MR settings are undefined and should be programmed as shown below.

(2). Clocks (CK_t, CK_c) need to be started and stabilized for at least 10ns or 5 ^{t}CK (whichever is larger) before CKE is registered HIGH at clock edge Td. Because CKE is a synchronous signal, the corresponding setup time to clock (^{t}IS) must be met. Also, a DESELECT command must be registered (with tIS setup time to clock) at clock edge Td. After the CKE is registered HIGH after RESET, CKE needs to be continuously registered HIGH until the initialization sequence is finished, including expiration of ^{t}DLLK and ^{t}ZQinit.

(3). The device keeps its ODT in High-Z state as long as RESET_n is asserted. Further, the SDRAM keeps its ODT in High-Z state after RESET_n de-assertion until CKE is registered HIGH. The ODT input signal may be in an undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held either LOW or HIGH. If $R_{TT(NOM)}$ is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power-up initialization sequence is finished, including the expiration of ^{t}DLLK and ^{t}ZQinit.

(4). After CKE is registered HIGH, wait a minimum of RESET CKE EXIT time, ^{t}XPR, before issuing the first MRS command to load mode register (^{t}XPR = MAX (^{t}XS, 5 x ^{t}CK).

(5). Issue MRS command to load MR3 with all application settings, wait ^{t}MRD.

(6). Issue MRS command to load MR6 with all application settings, wait ^{t}MRD.

(7). Issue MRS command to load MR5 with all application settings, wait ^{t}MRD.

(8). Issue MRS command to load MR4 with all application settings, wait ^{t}MRD.

(9). Issue MRS command to load MR2 with all application settings, wait ^{t}MRD.

(10). Issue MRS command to load MR1 with all application settings, wait ^{t}MRD.

(11). Issue MRS command to load MR0 with all application settings, wait ^{t}MOD.

(12). Issue a ZQCL command to start ZQ calibration.

(13). Wait for ^{t}DLLK and ^{t}ZQinit to complete.

(14). The device will be ready for normal operation. Once the DRAM has been initialized, if the DRAM is in an idle state longer than 960ms, then either (a) REF commands must be issued within ^{t}REFI constraints (specification for posting allowed) or (b) CKE or CS_n must toggle once within every 960ms interval of idle time. For debug purposes, the 960ms delay limit maybe extended to 60 minutes provided the DRAM is operated in this debug mode for no more than 360 cumulative hours.

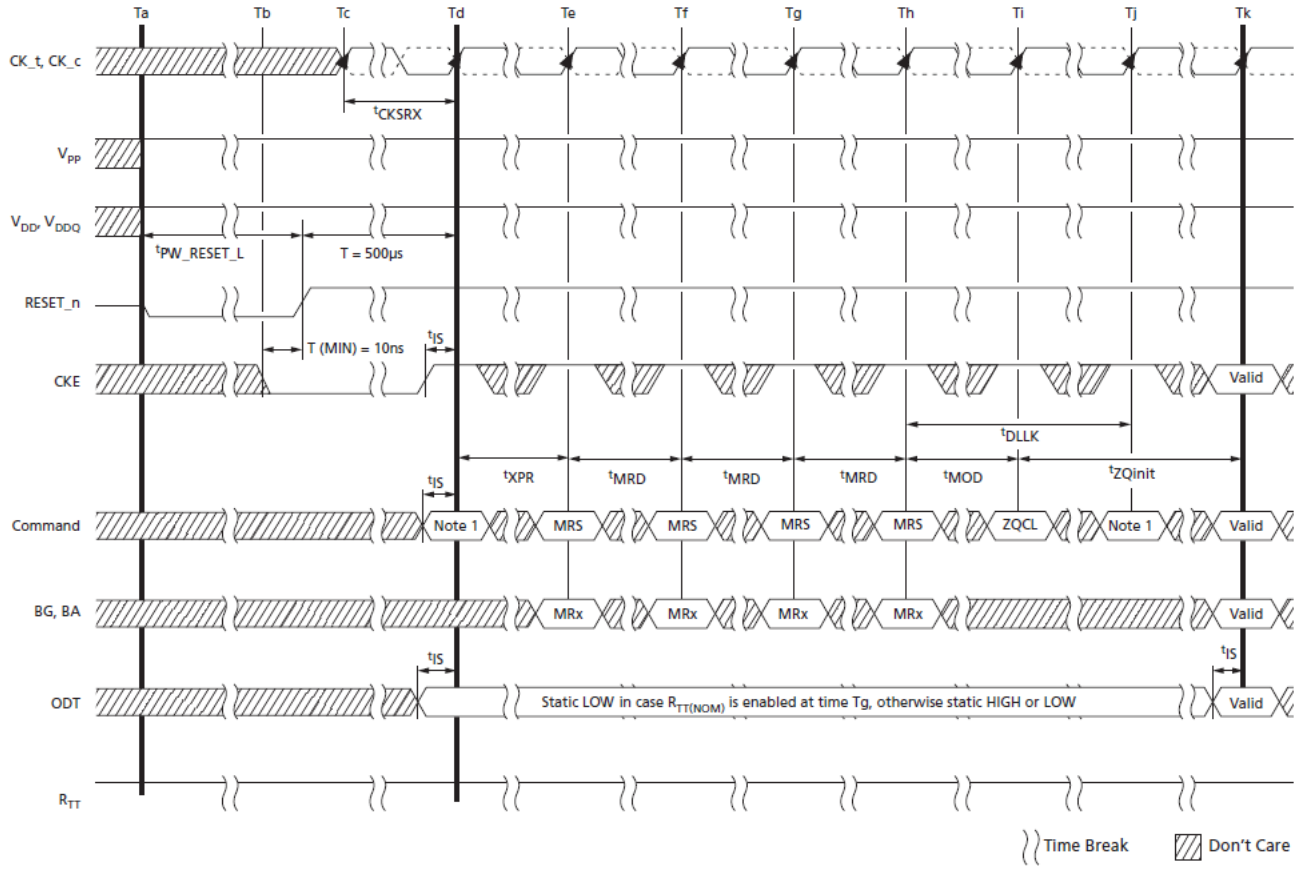
(15). Optional MBIST-PPR mode can be entered by setting MR4:A0 to 1, followed by subsequent MR0 guard key sequences, then DRAM will drive ALERT_n to LOW. DRAM will drive ALERT_n to HIGH to indicate that this operation is completed. MBIST-PPR mode can take place anytime after Tk. Note that no exit sequence or re-initialization is needed after MBIST completes; As soon as ALERT_N goes HIGH and ^{t}IS is satisfied, MR0 must be re-written to the pre guard key state, then and the DRAM is immediately ready to receive valid commands.

A stable valid V_{DD} level is a set DC level (0Hz to 250 KHz) and must be no less than $V_{DD,min}$ and no greater than $V_{DD,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ±60mV (greater than 250 KHz) is allowed on VDD provided the noise doesn't alter VDD to less than $V_{DD,min}$ or greater than $V_{DD,max}$.

A stable valid V_{DDQ} level is a set DC level (0Hz to 250 KHz) and must be no less than $V_{DDQ,min}$ and no greater than $V_{DDQ,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ±60mV (greater than 250 KHz) is allowed on V_{DDQ} provided the noise doesn't alter V_{DDQ} to less than $V_{DDQ,min}$ or greater than $V_{DDQ,max}$.

A stable valid V_{PP} level is a set DC level (0Hz to 250 KHz) and must be no less than $V_{PP,min}$ and no greater than $V_{PP,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ±120mV (greater than 250 KHz) is allowed on V_{PP} provided the noise doesn't alter V_{PP} to less than $V_{PP,min}$ or greater than $V_{PP,max}$.

Figure 4. RESET_n and Initialization Sequence at Power- on Ramping



Note:

1. From time point Td until Tk, DES commands must be applied between MRS and ZQCL commands.
2. MRS Commands must be issued to all Mode Registers that have defined settings.
3. In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
4. TEN is not shown; however, it is assumed to be held LOW.
5. Optional MBIST-PPR may be entered any time after Tk.

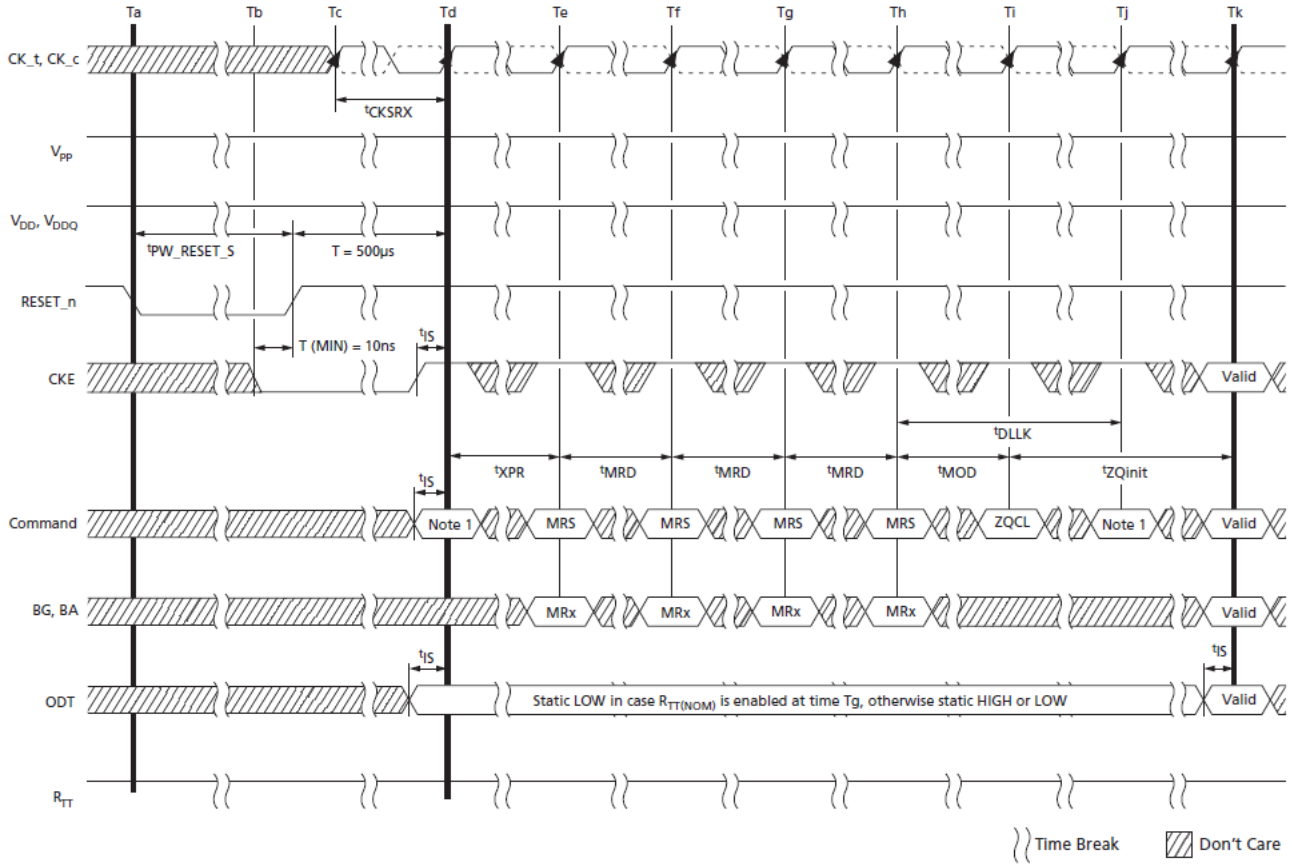
Reset Initialization with Stable Power Sequence

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below 0.2 x VDD any time when reset is needed (all other inputs may be undefined). RESET_n needs to be maintained for minimum tPW_RESET. CKE is pulled LOW before RESET_n being de-asserted (minimum time 10ns).
2. Follow Steps 2 through 10 in the Reset and Initialization Sequence at Power-On Ramping procedure.

When the reset sequence is complete, all counters except the refresh counters have been reset and the device is ready for normal operation.

Figure 5. RESET Procedure at Power Stable Condition



Note:

1. From time point Td until Tk, DES commands must be applied between MRS and ZQCL commands
2. MRS Commands must be issued to all Mode Registers that have defined settings.
3. In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
4. TEN is not shown; however, it is assumed to be held LOW.

Uncontrolled Power-Down Sequence

In the event of an uncontrolled ramping down of V_{PP} supply, V_{PP} is allowed to be less than V_{DD} provided the following conditions are met:

- Condition A: V_{PP} and V_{DD}/V_{DDQ} are ramping down (as part of turning off) from normal operating levels.
- Condition B: The amount that V_{PP} may be less than V_{DD}/V_{DDQ} is less than or equal to 500mV.
- Condition C: The time V_{PP} may be less than V_{DD} is ≤10ms per occurrence with a total accumulated time in this state ≤100ms.
- Condition D: The time V_{PP} may be less than 2.0V and above V_{SS} while turning off is ≤15ms per occurrence with a total accumulated time in this state ≤150ms.

Programming Mode Registers

For application flexibility, various functions, features, and modes are programmable in seven mode registers (MR*n*) provided by the device as user defined variables that must be programmed via a MODE REGISTER SET (MRS) command. Because the default values of the mode registers are not defined, contents of mode registers must be fully initialized and/or re-initialized; that is, they must be written after power-up and/or reset for proper operation. The contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS and DLL RESET commands do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

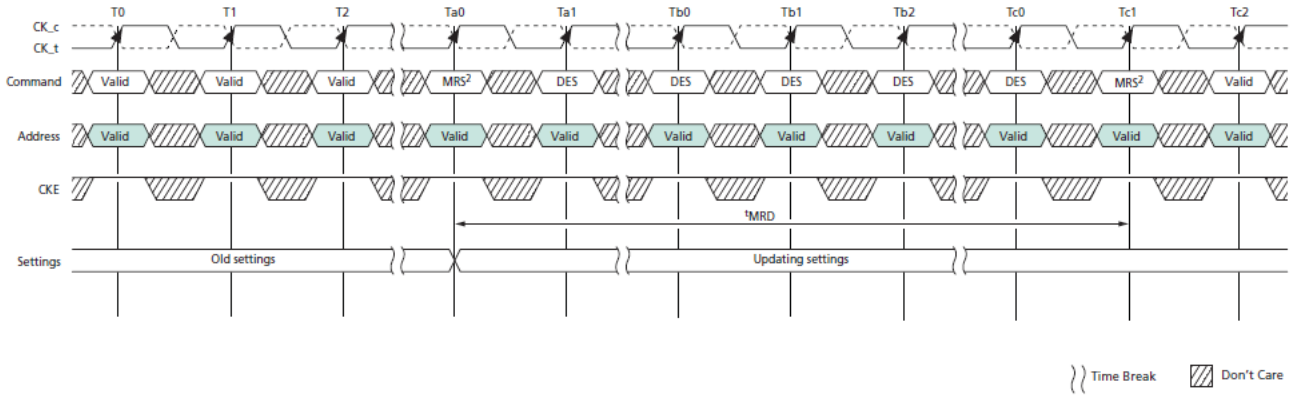
The MRS command cycle time, ^{t}MRD, is required to complete the WRITE operation to the mode register and is the minimum time required between the two MRS commands shown in the ^{t}MRD Timing figure.

Some of the mode register settings affect address/command/control input functionality. In these cases, the next MRS command can be allowed when the function being updated by the current MRS command is completed. These MRS command don't apply ^{t}MRD timing to the next MRS command; however, the input cases have unique MR setting procedures, so refer to individual function descriptions:

- Gear-down mode
- Per-DRAM addressability
- CMD address latency
- CA parity latency mode
- V_{REFDQ} training value
- V_{REFDQ} training mode
- V_{REFDQ} training range

Some mode register settings may not be supported because they are not required by certain speed bins.

Figure 6. ^{t}MRD Timing

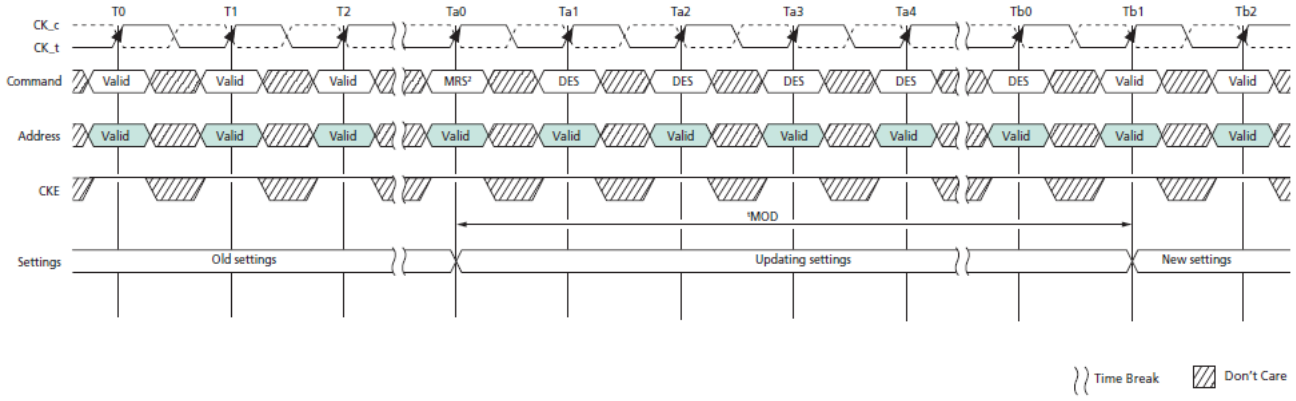


Note:

1. This timing diagram shows CA Parity Latency mode is "disable" case.
2. ^{t}MRD applies to all MRS commands with the following exceptions:
   - Gear down mode
   - CA parity latency mode
   - CMD address latency
   - Per-DRAM addressability mode
   - V_{REFDQ} training value, V_{REFDQ} training mode, and V_{REFDQ} training range

The MRS command to nonMRS command delay, tMOD, is required for the DRAM to update features, except for those noted in note 2 in figure below where the individual function descriptions may specify a different requirement. ^{t}MOD is the minimum time required from an MRS command to a nonMRS command, excluding DES, as shown in the ^{t}MOD Timing figure.

Figure 7. ^{t}MOD Timing



Note:

1. This timing diagram shows CA Parity Latency mode is “disable” case.
2. ^{t}MOD applies to all MRS commands with the following exceptions:
   - DLL Enable, DLL Reset
   - DLL enable, DLL RESET, Gear-down mode
   - V_{REFDQ} training value, internal V_{REF} training monitor, V_{REFDQ} training mode, and V_{REFDQ} training range
   - Maximum power savings mode, Per-DRAM addressability mode, and CA parity latency mode

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the device is in idle state; that is, all banks are in the precharged state with ^{t}RP satisfied, all data bursts are completed, and CKE is HIGH prior to writing into the mode register. If the $R_{TT(NOM)}$ feature is enabled in the mode register prior to and/or after an MRS command, the ODT signal must continuously be registered LOW, ensuring R_{TT} is in an off state prior to the MRS command.

The ODT signal may be registered HIGH after ^{t}MOD has expired. If the $R_{TT(NOM)}$ feature is disabled in the mode register prior to and after an MRS command, the ODT signal can be registered either LOW or HIGH before, during, and after the MRS command. The mode registers are divided into various fields depending on functionality and modes.

In some mode register setting cases, function updating takes longer than ^{t}MOD. This type of MRS does not apply ^{t}MOD timing to the next valid command, excluding DES. These MRS command input cases have unique MR setting procedures, so refer to individual function descriptions.

Mode Register 0

Mode register 0 (MR0) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR0 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR0 Register Definition table.

Table 6. Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 7. MR0 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 ; 1 = Reserved
20:18	**MR select** **000 = MR0** ; 001 = MR1 ; 010 = MR2 ; 011 = MR3 ; 100 = MR4 ; 101 = MR5 ; 110 = MR6 ; 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 ; 1 = Reserved
13, 11:9	**WR (WRITE recovery) / RTP (READ-to-PRECHARGE)** 0000 = 10 / 5 clocks1 ; 0001 = 12 / 6 clocks ; 0010 = 14 / 7 clocks1 ; 0011 = 16 / 8 / clocks 0100 = 18 / 9 clocks1 ; 0101 = 20 /10 clocks ; 0110 = 24 / 12 clocks ; 0111 = 22 / 11 clocks1 1000 = 26 / 13 clocks1 ; 1001 = 28 / 14 clocks2 ; 1010 through 1111 = Reserved
8	**DLL reset** 0 = No ; 1 = Yes
7	**Test mode (TM) - Manufacturer use only** 0 = Normal operating mode, must be programmed to 0
12, 6:4, 2	CAS latency (CL) – Delay in clock cycles from the internal Read command to first data-out 00000 = 9 clocks [*1] ; 00001 = 10 clocks ; 00010 = 11 clocks [*1] ; 00011 = 12 clocks ; 00100 = 13 clocks [*1] ; 00101 = 14 clocks ; 00110 = 15 clocks [*1] ; 00111 = 16 clocks 01000 = 18 clocks ; 01001 = 20 clocks ; 01010 = 22 clocks ; 01011 = 24 clocks 01100 = 23 clocks [*1] ; 01101 = 17 clocks [*1] ; 01110 = 19 clocks [*1] ; 01111 = 21 clocks [*1] 10000 = 25 clocks ; 10001 = 26 clocks ; 10011 = 28 clocks ; 10100 = 29 clocks [*1] 10101 = 30 clocks ; 10110 = 31 clocks [*1] ; 10111 = 32 clocks
3	**Burst type (BT) – Data burst ordering within a READ or WRITE busrt access** 0 = Nibble sequential ; 1 = Interleave
1:0	**Burst length (BL) – Data burst size associated with each READ or WRITE busrt access** 00 = BL8 (fixed) ; 01 = BC4 or BL8 (on-the-fly) ; 10 = BC4 (fixed) ; 11 = Reserved

Note:

1. Not allowed when 1/4 rate gear-down mode is enabled.
2. If WR requirement exceeds 28 clocks or RTP exceeds 14 clocks, WR should be set to 28 clocks and RTP should be set to 14 clocks.

Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selected coincidentally with the registration of a READ or WRITE command via A12/BC_n.

Table 8. Burst Type and Burst Order

Note 1 applies to the entire table

Burst Length	Read / Write	Starting Column Address (A2,A1,A0)	Burst type: Sequential (decimal)	Burst type: Interleaved (decimal)	Note
BC4	Read	0,0,0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	2,3
		0,0,1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	
		0,1,0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	
		0,1,1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	
		1,0,0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	
		1,0,1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	
		1,1,0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	
		1,1,1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	
	Write	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	
BL8	Read	0,0,0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	
		0,0,1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	
		0,1,0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	
		0,1,1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	
		1,0,0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	
		1,0,1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	
		1,1,0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	
		1,1,1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	
	Write	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	3

Note:

1. 0...7 bit number is the value of CA[2:0] that causes this bit to be the first read during a burst.
2. When setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode, meaning the starting point for ^{t}WR and ^{t}WTR will be pulled in by two clocks. When setting burst length to OTF in MR0, the internal WRITE operation starts at the same time as a BL8 (even if BC4 was selected during column time using A12/BC4_n) meaning that if the OTF MR0 setting is used, the starting point for ^{t}WR and ^{t}WTR will not be pulled in by two clocks as described in the BC4 (fixed) case.
3. T = Output driver for data and strobes are in High-Z.
   V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins.
   X = “Don’t care.”

Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a value of 1 places the device into a DRAM manufacturer-defined test mode to be used only by the manufacturer, not by the end user. No operations or functionality is specified if MR0[7] = 1.

Write Recovery (WR)/READ-to-PRECHARGE

The programmed write recovery (WR) value is used for the auto precharge feature along with tRP to determine tDAL. WR for auto precharge (MIN) in clock cycles is calculated by dividing ^{t}WR (in ns) by ^{t}CK (in ns) and rounding to the next integer using the rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section. The WR value must be programmed to be equal to or larger than ^{t}WR (MIN). When both DM and write CRC are enabled in the mode register, the device calculates CRC before sending the write data into the array; ^{t}WR values will change when enabled. If there is a CRC error, the device blocks the WRITE operation and discards the data.

Internal READ-to-PRECHARGE (RTP) command delay for auto precharge (MIN) in clock cycles is calculated by dividing ^{t}RTP (in ns) by ^{t}CK (in ns) and rounding to the next integer using the rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section.

The RTP value in the mode register must be programmed to be equal to or larger than RTP (MIN). The programmed RTP value is used with tRP to determine the ACT timing to the same bank.

DLL RESET

The DLL reset bit is self-clearing, meaning that it returns to the value of 0 after the DLL RESET function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time the DLL RESET function is used, ^{t}DLLK must be met before functions requiring the DLL can be used. Such as READ commands or synchronous ODT operations, for example.

Mode Register 1

Mode register 1 (MR1) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR1 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR1 Register Definition table.

Table 9. Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 10. MR1 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 ; 1 = Reserved
20:18	**MR select** 000 = MR0 ; **001 = MR1** ; 010 = MR2 ; 011 = MR3 ; 100 = MR4 ; 101 = MR5 ; 110 = MR6 ; 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 ; 1 = Reserved
12	**Data output disable (Qoff) – Output buffer disable** 0 = Enabled (normal operation) ; 1 = Disabled (both ODI and R_{TT})
11	**Termination data strobe (TDQS) – Additional termination pins (x8 configuration only)** 0 = TDQS disabled ; 1 = TDQS enabled
10:8	**Nominal ODT ($R_{TT(NOM)}$) – Data bus termination setting** 000 = $R_{TT(NOM)}$ disabled ; 001 = R_{ZQ}/4 (60 ohm) ; 010 = R_{ZQ}/2 (120 ohm) ; 011 = R_{ZQ}/6 (40 ohm) 100 = R_{ZQ}/1 (240 ohm) ; 101 = R_{ZQ}/5 (48 ohm) ; 110 = R_{ZQ}/3 (80 ohm) ; 111 = R_{ZQ}/7 (34 ohm)
7	Write leveling (WL) – Write leveling mode 0 = Disabled (normal operation) ; 1 = Enabled (enter WL mode)
13, 6:5	**Rx CTLE Control** 000 = Vendor Default ; 001 = Vendor Defined ; 010 = Vendor Defined ; 011 = Vendor Defined 100 = Vendor Defined ; 101 = Vendor Defined ; 110 = Vendor Defined ; 111 = Vendor Defined
4:3	**Additive latency (AL) – Command additive latency setting** 00 = 0 (AL disabled) ; 01 = CL – 1[*1] ; 10 = CL – 2 ; 11 = Reserved
2:1	**Output driver impedance (ODI) – Output driverimpedance setting** 00 = R_{ZQ}/7 (34 ohm) 01 = R_{ZQ}/5 (48 ohm) 10 = Reserved (Although not JEDEC-defined and not tested, this setting will provide R_{ZQ}/6 or 40 ohm) 11 = Reserved
0	**DLL enable – DLL enable feature** 0 = DLL disabled 1 = DLL enabled (normal operation)

Notes: 1. Not allowed when 1/4 rate gear-down mode is enabled.

DLL Enable / DLL Disable

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation (DLL enabled with MR1[0]) the DLL is automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled upon exit of the SELF REFRESH operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a READ or SYNCHRONOUS ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}DQSCK, ^{t}AON, or ^{t}AOF parameters.

During ^{t}DLLK, CKE must continuously be registered HIGH. The device does not require DLL for any WRITE operation, except when $R_{TT(WR)}$ is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL off mode. The ODT resistors must be disabled by continuously registering the ODT pin LOW and/or by programming the RTT(NOM) bits MR1[9,6,2] = 000 via an MRS command during DLL off mode.

The dynamic ODT feature is not supported in DLL off mode; to disable dynamic ODT externally, use the MRS command to set $R_{TT(WR)}$, MR2[10:9] = 00.

Output Driver Impedance Control

The output driver impedance of the device is selected by MR1[2,1], as shown in the MR1 Register Definition table.

ODT $R_{TT(NOM)}$ Values

The device is capable of providing three different termination values: $R_{TT(Park)}$, $R_{TT(NOM)}$, and $R_{TT(WR)}$.
The nominal termination value, $R_{TT(NOM)}$, is programmed in MR1. A separate value, $R_{TT(WR)}$, may be programmed in MR2 to enable a unique R_{TT} value when ODT is enabled during WRITE operations. The $R_{TT(WR)}$ value can be applied during WRITE commands even when $R_{TT(NOM)}$ is disabled. A third R_{TT} value, $R_{TT(Park)}$, is programed in MR5. $R_{TT(Park)}$ provides a termination value when the ODT signal is LOW.

Additive Latency

The ADDITIVE LATENCY (AL) operation is supported to make command and data buses efficient for sustainable bandwidths in the device. In this operation, the device allows a READ or WRITE command (either with or without auto precharge) to be issued immediately after the ACTIVATE command. The command is held for the time of AL before it is issued inside the device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. WRITE latency (WL) is controlled by the sum of the AL and CAS WRITE latency (CWL) register settings.

Table 11. Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Notes: 1. AL has a value of CL - 1 or CL - 2 based on the CL values programmed in the MR0 register.

Rx CTLE Control

The Mode Register for Rx CTLE Control MR1[A13,A6,A5] is vendor specific. Since CTLE circuits can not be typically bypassed a disable option is not provided. Instead, a vendor optimized setting is given. It should be noted that the settings are not specifically linear in relationship to the vendor optimized setting, so the host may opt to instead walk through all the provided options and use the setting that works best in their environment.

Write Leveling

For better signal integrity, the device uses fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology benefits from a reduced number of stubs and their lengths, but it causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain ^{t}DQSS, ^{t}DSS, and ^{t}DSH specifications. Therefore, the device supports a write leveling feature that allows the controller to compensate for skew.

Output Disable

The device outputs may be enabled/disabled by MR1[12] as shown in the MR1 Register Definition table. When MR1[12] is enabled (MR1[12] = 1) all output pins (such as DQ and DQS) are disconnected from the device, which removes any loading of the output drivers. For example, this feature may be useful when measuring module power. For normal operation, set MR1[12] to 0.

Mode Register 2

Mode register 2 (MR2) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR2 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR2 Register Definition table.

Table 12. Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 13. MR2 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 ; 1 = Reserved
20:18	**MR select** 000 = MR0 ; 001 = MR1 ; 010 = **MR2** ; 011 = MR3 ; 100 = MR4 ; 101 = MR5 ; 110 = MR6 ; 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 ; 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 ; 1 = Reserved
12	**WRITE data bus CRC** 0 = Disabled ; 1 = Enabled
11:9	**Dynamic ODT ($R_{TT(WR)}$) – Data bus termination setting during WRITEs** 000 = $R_{TT(WR)}$ disabled (WRITE does not affect R_{TT} value) ; 001 = R_{ZQ}/2 (120 ohm) ; 010 = R_{ZQ}/1 (240 ohm) ; 011 = High-Z ; 100 = R_{ZQ}/3 (80 ohm) 101 = Reserved ; 110 = Reserved ; 111 = Reserved
7:6	**Low power auto self refresh (LPASR) – Mode summary** 00 = Manual mode - Normal operating temperature range (T_C: 0°C ~85°C) 01 = Manual mode - Reduced operating temperature range (T_C: 0°C ~45°C) 10 = Manual mode - Extended operating temperature range (T_C: 0°C ~95°C) 11 = ASR mode - Automatically switching among all modes
5:3	**CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 1^{t}CK WRITE preamble** 000 = 9 (DDR4-1600) [*1] ; 001 = 10 (DDR4-1866) ; 010 = 11 (DDR4-2133/1600) [*1] ; 011 = 12 (DDR4-2400/1866) ; 100 = 14 (DDR4-2666/2133) ; 101 = 16 (DDR4-2933,3200/2400) ; 110 = 18 (DDR4-2666) ; 111 = 20 (DDR4-2933, 3200)
	CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 2^{t}CK WRITE preamble 000 = N/A ; 001 = N/A ; 010 = N/A ; 011 = N/A ; 100 = 14 (DDR4-2400) ; 101 = 16 (DDR4-2666/2400) ; 110 = 18 (DDR4-2933, 3200/2666) ; 111 = 20 (DDR4-2933, 3200)
8,2	**RFU** 0 = Must be programmed to 0 ; 1 = Reserved
1:0	**RFU** 0 = Must be programmed to 0 ; 1 = Reserved

Notes: 1. Not allowed when 1/4 rate gear-down mode is enabled.

CAS WRITE Latency

CAS WRITE latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. The device does not support any half-clock latencies. The overall WRITE latency (WL) is defined as additive latency (AL) + parity latency (PL) + CAS WRITE latency (CWL): WL = AL +PL + CWL.

Low-Power Auto Self Refresh

Low-power auto self refresh (LPASR) is supported in the device. Applications requiring SELF REFRESH operation over different temperature ranges can use this feature to optimize the IDD6 current for a given temperature range as specified in the MR2 Register Definition table.

Dynamic ODT

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the device without issuing an MRS command. This may be done by configuring the dynamic ODT ($R_{TT(WR)}$) settings in MR2[11:9]. In write leveling mode, only $R_{TT(NOM)}$ is available.

Write Cyclic Redundancy Check Data Bus

The write cyclic redundancy check (CRC) data bus feature during writes has been added to the device.

When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra two UIs are used for the CRC information.

Mode Register 3

Mode register 3 (MR3) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR3 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR3 Register Definition table.

Table 14. Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 15. MR3 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 ; 1 = Reserved
20:18	**MR select** 000 = MR0 ; 001 = MR1 ; 010 = MR2 ; 011 = **MR3** ; 100 = MR4 ; 101 = MR5 ; 110 = MR6 ; 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 ; 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 ; 1 = Reserved
12:11	**Multipurpose register (MPR) – Read format** 00 = Serial ; 01 = Parallel ; 10 = Staggered ; 11 = Reserved
10:9	**WRITE CMD latency when CRC/DM enabled** 00 = 4CK (DDR4-1600) ; 01 = 5CK (DDR4-1866/2133/2400/2666) ; 10 = 6CK (DDR4-2933/3200) 11 = Reserved
8:6	**Fine granularity refresh mode** 000 = Normal mode (fixed 1x) ; 001 = Fixed 2x ; 010 = Fixed 4x ; 011 = Reserved 100 = Reserved ; 101 = On-the-fly 1x/2x ; 110 = On-the-fly 1x/4x ; 111 = Reserved
5	**Temperature sensor status** 0 = Disabled ; 1 = Enabled
4	**Per-DRAM addressability** 0 = Normal operation (disabled) ; 1 = Enable
3	**Gear-down mode – Ratio of internal clock to external data rate** 0 = [1:1]; (1/2 rate data) ; 1 = [2:1]; (1/4 rate data)
2	**Multipurpose register (MPR) access** 0 = Normal operation ; 1 = Data flow from MPR
1:0	**MPR page select** 00 = Page 0 ; 01 = Page 1 ; 10 = Page 2 ; 11 = Page 3 (restricted for DRAM manufacturer use only)

Multipurpose Register

The multipurpose register (MPR) is used for several features:

- Readout of the contents of the MR*n* registers
- WRITE and READ system patterns used for data bus calibration
- Readout of the error frame when the command address parity feature is enabled

To enable MPR, issue an MRS command to MR3[2] = 1. MR3[12:11] define the format of read data from the MPR. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register.

The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power-down mode, SELF REFRESH, and any other nonRD/RDA or nonWR/WRA commands are not allowed during MPR mode.

The RESET function is supported during MPR mode, which requires device re-initialization.

WRITE Command Latency When CRC/DM is Enabled

The WRITE command latency (WCL) must be set when both write CRC and DM are enabled for write CRC persistent mode. This provides the extra time required when completing a WRITE burst when write CRC and DM are enabled. This means at data rates less than or equal to 1600 MT/s then 4nCK is used, 5nCK or 6nCK are not allowed; at data rates greater than 1600 MT/s and less than or equal to 2666 MT/s then 5nCK is used, 4nCK or 6nCK are not allowed; and at data rates greater than 2666 MT/s and less than or equal to 3200 MT/s then 6nCK is used; 4nCK or 5nCK are not allowed.

Fine Granularity Refresh Mode

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening ^{t}RFC and decreasing cycle time allows more accesses to the chip and allows for increased scheduling flexibility.

Temperature Sensor Status

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; when an MPR read of the temperature sensor status bits occurs, the temperature sensor status should be no older than 32ms.

Per-DRAM Addressability

This mode allows commands to be masked on a per device basis providing any device in a rank (devices sharing the same command and address signals) to be programmed individually. As an example, this feature can be used to program different ODT or VREF values on DRAM devices within a given rank.

Gear-Down Mode

The device defaults in 1/2 rate (1N) clock mode and uses a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS_n, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode, no MRS command or sync pulse is required.

Mode Register 4

Mode register 4 (MR4) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR4 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR4 Register Definition table.

Table 16. Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 17. MR4 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 ; 1 = Reserved
20:18	**MR select** 000 = MR0 ; 001 = MR1 ; 010 = MR2 ; 011 = MR3 ; 100 = **MR4** ; 101 = MR5 ; 110 = MR6 ; 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 ; 1 = Reserved
13	**Hard Post Package Repair (hPPR mode)** 0 = Disabled ; 1 = Enabled
12	**WRITE preamble setting** 0 = 1^{t}CK toggle1 1 = 2^{t}CK toggle (When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.)
11	**READ preamble setting** 0 = 1^{t}CK toggle [*1] ; 1 = 2^{t}CK toggle
10	**READ preamble training** 0 = Disabled ; 1 = Enabled
9	**Self refresh abort mode** 0 = Disabled ; 1 = Enabled
8:6	**CMD (CAL) address latency** 000 = 0 clocks (disabled) ; 001 =3 clocks [*1] ; 010 = 4 clocks ; 011 = 5 clocks [*1] ; 100 = 6 clocks ; 101 = 8 clocks ; 110 = Reserved ; 111 = Reserved
5	**soft Post Package Repair (sPPR mode)** 0 = Disabled ; 1 = Enabled
4	**Internal V_{REF} monitor** 0 = Disabled ; 1 = Enabled
3	**Temperature controlled refresh mode** 0 = Disabled ; 1 = Enabled
2	**Temperature controlled refresh range** 0 = Normal temperature mode ; 1 = Reserved
1	**Maximum power savings mode** 0 = Normal operation ; 1 = Enabled
0	**MBIST-PPR** 0 = Disabled ; 1 = Enabled

Notes: 1. Not allowed when 1/4 rate gear-down mode is enabled.

Hard Post Package Repair Mode

The hard post package repair (hPPR) mode feature is JEDEC optional for 4Gb DDR4 memories. Performing an MPR read to page 2 MPR0 [7] indicates whether hPPR mode is available (A7 = 1) or not available (A7 = 0). hPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank can be repaired. The repair process is irrevocable so great care should be exercised when using.

Soft Post Package Repair Mode

The soft post package repair (sPPR) mode feature is JEDEC optional for 4Gb and 8Gb DDR4 memories.

Performing an MPR read to page 2 MPR0 [6] indicates whether sPPR mode is available (A6 = 1) or not available (A6 = 0). sPPR mode provides a simple and easy repair method of the device after placed in the system. One row per bank can be repaired. The repair process is revocable by either doing a reset or power-down or by rewriting a new address in the same bank.

WRITE Preamble

Programmable WRITE preamble, ^{t}WPRE, can be set to 1^{t}CK or 2^{t}CK via the MR4 register. The 1^{t}CK setting is similar to DDR3. However, when operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.

Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

READ Preamble

Programmable READ preamble tRPRE can be set to 1^{t}CK or 2^{t}CK via the MR4 register. Both the 1^{t}CK and 2^{t}CK DDR4 preamble settings are different from that defined for the DDR3 SDRAM. Both DDR4 READ preamble settings may require the memory controller to train (or read level) its data strobe receivers using the READ preamble training.

READ Preamble Training

Programmable READ preamble training can be set to 1^{t}CK or 2^{t}CK. This mode can be used by the memory controller to train or READ level its data strobe receivers.

Temperature-Controlled Refresh

When temperature-controlled refresh mode is enabled, the device may adjust the internal refresh period to be longer than tREFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45°C. Normal temperature mode covers the range of 0°C to 85°C. Noted that temperature controlled refresh (TCR) is not supported during extended temperature range (85°C to 95°C).

Command Address Latency

COMMAND ADDRESS LATENCY (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles (^{t}CAL) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register according to the ^{t}CAL(ns)/^{t}CK(ns) rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section.

Internal V_{REF} Monitor

This mode enables output of internally generated V_{REFDQ} for monitoring on DQ0, DQ1, DQ2, and DQ3. May be used during V_{REFDQ} training and test. While in this mode, R_{TT} should be set to High-Z. V_{REF_time} must be increased by 10ns if DQ load is 0pF, plus an additional 15ns per pF of loading. This measurement is for verification purposes and is NOT an external voltage supply pin.

Maximum Power Savings Mode

This mode provides the lowest power mode where data retention is not required. When the device is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal LOW).

MBIST-PPR

This mode is JEDEC optional and allows for a self-contained DRAM test and repair. Please refer to the Features list on page 1 for a list of die revisions that support MBIST-PPR.

Mode Register 5

Mode register 5 (MR5) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR5 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR5 Register Definition table.

Table 18. Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 19. MR5 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 ; 1 = Reserved
20:18	**MR select** 000 = MR0 ; 001 = MR1 ; 010 = MR2 ; 011 = MR3 ; 100 = MR4 ; 101 = **MR5** ; 110 = MR6 ; 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 ; 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 ; 1 = Reserved
12	**Data bus inversion (DBI) – READ DBI enable** 0 = Disabled ; 1 = Enabled
11	**Data bus inversion (DBI) – WRITE DBI enable** 0 = Disabled ; 1 = Enabled
10	**Data mask (DM)** 0 = Disabled ; 1 = Enabled
9	**CA parity persistent error mode** 0 = Disabled ; 1 = Enabled
8:6	**Parked ODT value ($R_{TT(Park)}$)** 000 = $R_{TT(Park)}$ disabled ; 001 = R_{ZQ}/4 (60 ohm) ; 010 = R_{ZQ}/2 (120 ohm) ; 011 = R_{ZQ}/6 (40 ohm) 100 = R_{ZQ}/1 (240 ohm) ; 101 = R_{ZQ}/5 (48 ohm) ; 110 = R_{ZQ}/3 (80 ohm) ; 111 = R_{ZQ}/7 (34 ohm)
5	**ODT input buffer for power-down** 0 = Buffer enabled ; 1 = Buffer disabled
4	**CA parity error status** 0 = Clear ; 1 = Error
3	**CRC error status** 0 = Clear ; 1 = Error
2:0	**CA parity latency mode** 000 = Disable ; 001 = 4 clocks (DDR4-1600/1866/2133) ; 010 = 5 clocks (DDR4-2400/2666) [*1] ; 011 = 6 clocks (DDR4-2933/3200) ; 100 = Reserved ; 101 = Reserved ; 110 = Reserved ; 111 = Reserved

Notes: 1. Not allowed when 1/4 rate gear-down mode is enabled.

Data Bus Inversion

The DATA BUS INVERSION (DBI) function has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DBI function shares a common pin with the DM and TDQS functions. The DBI function applies to both READ and WRITE operations; Write DBI cannot be enabled at the same time the DM function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI). DBI is not allowed during MPR READ operation; during an MPR read, the DRAM ignores the read DBI enable setting in MR5 bit A12.

DBI is not supported for 3DS devices and should be disabled in MR5.

Data Mask

The DATA MASK (DM) function, also described as a partial write, has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DM function shares a common pin with the DBI and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the write DBI function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

CA Parity Persistent Error Mode

Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

ODT Input Buffer for Power-Down

This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during power-down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide $R_{TT(NOM)}$ termination. However, the device may provide $R_{TT(Park)}$ termination depending on the MR settings. This is primarily for additional power savings.

CA Parity Error Status

The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CRC Error Status

The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CA Parity Latency Mode

CA parity is enabled when a latency value, dependent on tCK, is programmed; this accounts for parity calculation delay internal to the device. The normal state of CA parity is to be disabled. If CA parity is enabled, the device must ensure there are no parity errors before executing the command. CA parity signal (PAR) covers ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT, and CS_n are not included in the parity calculation.

Mode Register 6

Mode register 6 (MR6) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR6 is written by issuing the MRS command while controlling the states of the BG*x*, BA*x*, and A*x* address pins. The mapping of address pins during the MRS command is shown in the following MR6 Register Definition table..

Table 20. Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Notes: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 21. MR6 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 ; 1 = Reserved
20:18	**MR select** 000 = MR0 ; 001 = MR1 ; 010 = MR2 ; 011 = MR3 ; 100 = MR4 ; 101 = MR5 ; 110 = **MR6** ; 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 ; 1 = Reserved
12:10	**Data rate** 000 = Data rate ≦1333 Mb/s (1333 Mb/s) 001 = 1333 Mb/s < Data rate ≦1866 Mb/s (1600, 1866 Mb/s) 010 = 1866 Mb/s < Data rate ≦2400 Mb/s (2133, 2400 Mb/s) 011 = 2400 Mb/s < Data rate ≦2666 Mb/s (2666 Mb/s) 100 = 2666 Mb/s < Data rate ≦3200 Mb/s (2933, 3200 Mb/s) 101 = Reserved ; 110 = Reserved ; 111 = Reserved
13, 9:8	**RFU** Default = 000; Must be programmed to 000 ; 001 = Reserved ; 010 = Reserved ; 011 = Reserved ; 100 = Reserved ; 101 = Reserved ; 110 = Reserved ; 111 = Reserved
7	**V_{REF} Calibration Enable** 0 = Disable ; 1 = Enable
6	**V_{REF} Calibration Range** 0 = Range 1 ; 1 = Range 2
5:0	**V_{REF} Calibration Value** See the V_{REFDQ} Range and Levels table in the V_{REFDQ} Calibration section

Notes: 1. Not allowed when 1/4 rate gear-down mode is enabled.

Data Rate Programming

The device controller must program the correct data rate according to the operating frequency.

V_{REFDQ} Calibration Enable

V_{REFDQ} calibration is where the device internally generates its own V_{REFDQ} to be used by the DQ input receivers. The V_{REFDQ} value will be output on any DQ of DQ[3:0] for evaluation only. The device controller is responsible for setting and calibrating the internal V_{REFDQ} level using an MRS protocol (adjust up, adjust down, and so on). It is assumed that the controller will use a series of writes and reads in conjunction with V_{REFDQ} adjustments to optimize and verify the data eye. Enabling V_{REFDQ} calibration must be used whenever values are being written to the MR6[6:0] register.

V_{REFDQ} Calibration Range

The device defines two V_{REFDQ} calibration ranges: Range 1 and Range 2. Range 1 supports V_{REFDQ} between 60% and 92% of V_{DDQ} while Range 2 supports V_{REFDQ} between 45% and 77% of V_{DDQ}, as seen in V_{REFDQ} Specification table. Although not a restriction, Range 1 was targeted for module-based designs and Range 2 was added to target point-to-point designs.

V_{REFDQ} Calibration Value

Fifty settings provide approximately 0.65% of granularity steps sizes for both Range 1 and Range 2 of V_{REFDQ}, as seen in V_{REFDQ} Range and Levels table in the V_{REFDQ} Calibration section.

Truth Tables

Table 22. Truth Tables – Command

Notes 1-5 apply to the entire table; Note 6 applies to all READ/WRITE commands

Function	Symbol	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n /A14	BG0-BG1	BA0-BA1	C2-C0	A12/BC_n	A13, A11	A10/AP	A0-A9	Notes
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				7
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	8-10
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	8-11
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
Reserved for future use	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	12
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	13
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	10,14
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	10,14
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	X	X	X	X	X	H	X	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	X	X	X	X	X	L	X	

Notes:

1. BG = Bank group address ; BA = Bank address ; RA = Row address ; CA = Column address ; BC_n = Burst chop ; X = “Don’t Care” ; V = Valid
2. All DDR4 SDRAM commands are defined by states of CS_n, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, and CKE at the rising edge of the clock.
   The MSB of BG, BA, RA, and CA are device density- and configuration-dependent. When ACT_n = H, pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as command pins RAS_n, CAS_n, and WE_n, respectively. When ACT_n = L, pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as address pins A16, A15, and A14, respectively.
3. RESET_n is enabled LOW and is used only for asynchronous reset and must be maintained HIGH during any function.
4. Bank group addresses (BG) and bank addresses (BA) determine which bank within a bank group is being operated upon. For MRS commands, the BG and BA selects the specific mode register location.
5. V means HIGH or LOW (but a defined logic level), and X means either defined or undefined (such as floating) logic level.
6. READ or WRITE bursts cannot be terminated or interrupted, and fixed/on-the-fly (OTF) BL will be defined by MRS.
7. During an MRS command, A17 is RFU and is device density- and configuration-dependent.
8. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh.
9. V_{PP} and V_{REF} (V_{REFCA}) must be maintained during SELF REFRESH operation.
10. Refer to the Truth Table - CKE table for more details about CKE transition.
11. Controller guarantees self refresh exit to be synchronous. DRAM implementation has the choice of either synchronous or asynchronous.
12. The NO OPERATION (NOP) command may be used only when exiting maximum power saving mode or when entering gear-down mode.
13. The NOP command may not be used in place of the DESELECT command.
14. The power-down mode does not perform any REFRESH operation.

Table 23. Truth Tables – CKE

Notes 1-7, 9, and 20 apply to the entire table

Current State	CKE		Command (n)	Action (n)	Notes
	Previous Cycle (n - 1)	Previous Cycle (n)			
Power-down	L	L	X	Maintain power-down	8,10,11
	L	H	DES	Power-down exit	8,10,12
Self refresh	L	L	X	Maintain self refresh	11,13
	L	H	DES	Self refresh exit	8,13,14,15
Bank(s) active	H	L	DES	Active power-down entry	8,10,12,16
Reading	H	L	DES	Power-down entry	8,10,12,16,17
Writing	H	L	DES	Power-down entry	8,10,12,16,17
Precharging	H	L	DES	Power-down entry	8,10,12,16,17
Refreshing	H	L	DES	Precharge power-down entry	8,12
All banks idle	H	L	DES	Precharge power-down entry	8,10,12,16,18
	H	L	REFRESH	Self refresh	16,18,19

Notes:

1. Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge n.
2. CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.
3. COMMAND (n) is the command registered at clock edge n, and ACTION (n) is a result of COMMAND (n); ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh.
6. During any CKE transition (registration of CKE H→L or CKE H→L), the CKE level must be maintained until 1 nCK prior to ^{t}CKE (MIN) being satisfied (at which time CKE may transition again).
7. DESELECT and NOP are defined in the Truth Table - Command table.
8. For power-down entry and exit parameters, see the Power-Down Modes section.
9. CKE LOW is allowed only if ^{t}MRD and ^{t}MOD are satisfied.
10. The power-down mode does not perform any REFRESH operations.
11. X = "Don't Care" (including floating around V_{REF}) in self refresh and power-down. X also applies to address pins.
12. The DESELECT command is the only valid command for power-down entry and exit.
13. VPP and V_{REFCA} must be maintained during SELF REFRESH operation.
14. On self refresh exit, the DESELECT command must be issued on every clock edge occurring during the ^{t}XS period. READ or ODT commands may be issued only after ^{t}XSDLL is satisfied.
15. The DESELECT command is the only valid command for self refresh exit.
16. Self refresh cannot be entered during READ or WRITE operations. For a detailed list of restrictions see the SELF REFRESH Operation and Power-Down Modes sections.
17. If all banks are closed at the conclusion of the READ, WRITE, or PRECHARGE command, then precharge power-down is entered; otherwise, active power-down is entered.
18. Idle state is defined as all banks are closed (^{t}RP, ^{t}DAL, and so on, satisfied), no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied (^{t}MRD, ^{t}MOD, ^{t}RFC, ^{t}ZQinit, ^{t}ZQoper, ^{t}ZQCS, and so on), as well as all self refresh exit and power-down exit parameters are satisfied (^{t}XS, ^{t}XP, ^{t}XSDLL, and so on).
19. Self refresh mode can be entered only from the all banks idle state.
20. For more details about all signals, see the Truth Table - Command table; must be a legal command as defined in the table.

NOP Command

The NO OPERATION (NOP) command was originally used to instruct the selected DDR4 SDRAM to perform a NOP (CS_n = LOW and ACT_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 = HIGH). This prevented unwanted commands from being registered during idle or wait states. NOP command general support has been removed and the command should not be used unless specifically allowed, which is when exiting maximum power-saving mode or when entering gear-down mode.

DESELECT Command

The deselect function (CS_n HIGH) prevents new commands from being executed; therefore, with this command, the device is effectively deselected. Operations already in progress are not affected.

DLL-Off Mode

DLL-off mode is entered by setting MR1 bit A0 to 0, which will disable the DLL for subsequent operations until the A0 bit is set back to 1. The MR1 A0 bit for DLL control can be switched either during initialization or during self refresh mode. Refer to the Input Clock Frequency Change section for more details.

The maximum clock frequency for DLL-off mode is specified by the parameter ^{t}CKDLL_OFF.

Due to latency counter and timing restrictions, only one CL value and CWL value (in MR0 and MR2 respectively) are supported. The DLL-off mode is only required to support setting both CL = 10 and CWL = 9.

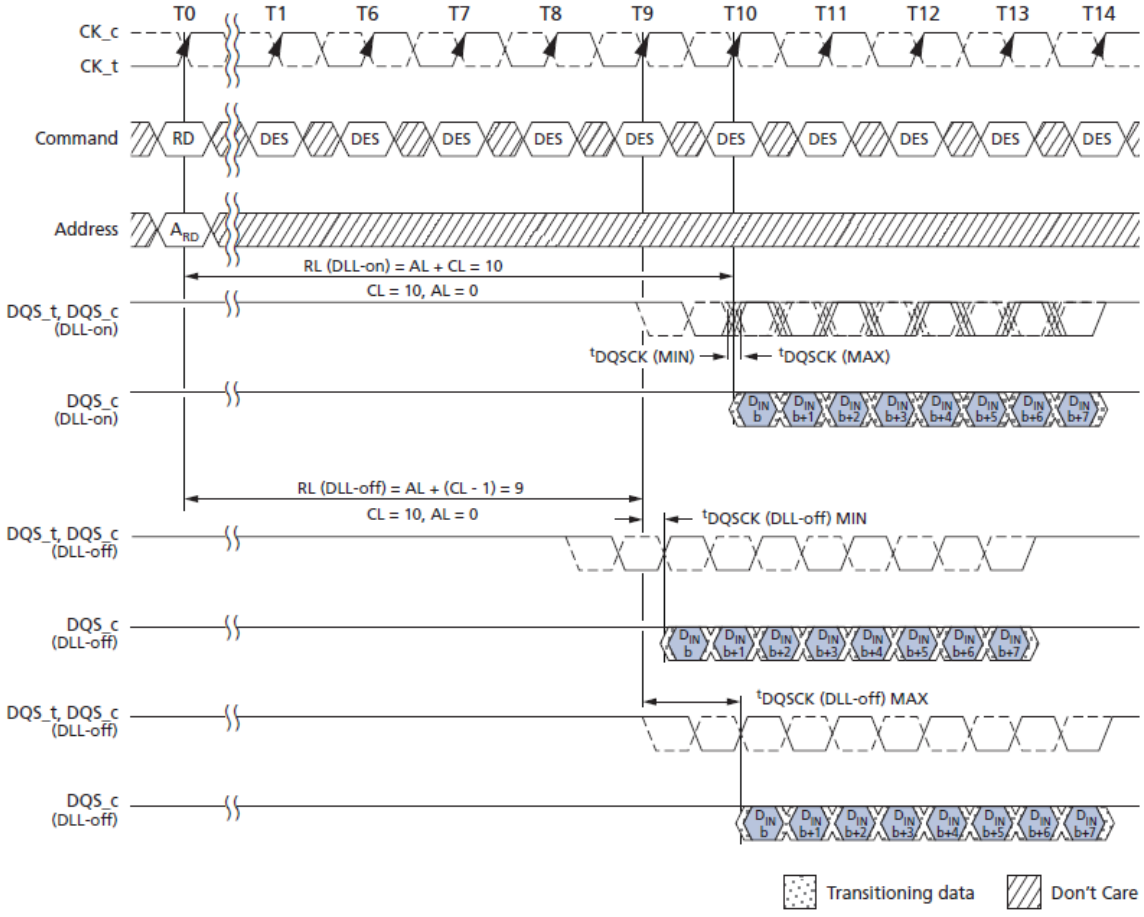
DLL-off mode will affect the read data clock-to-data strobe relationship (^{t}DQSCK), but not the data strobe-to-data relationship (^{t}DQSQ, ^{t}QH). Special attention is needed to line up read data to the controller time domain.

Compared with DLL-on mode, where ^{t}DQSCK starts from the rising clock edge (AL + CL) cycles after the READ command, the DLL-off mode ^{t}DQSCK starts (AL + CL - 1) cycles after the READ command.

Another difference is that ^{t}DQSCK may not be small compared totCK (it might even be larger than ^{t}CK), and the difference between ^{t}DQSCK (MIN) and ^{t}DQSCK (MAX) is significantly larger than in DLL-on mode. The ^{t}DQSCK (DLL-off) values are undefined and the user is responsible for training to the data-eye.

The timing relations on DLL-off mode READ operation are shown in the following diagram, where CL = 10, AL = 0, and BL = 8.

Figure 8. DLL-Off Mode Read Timing Operation



DLL-On/Off Switching Procedures

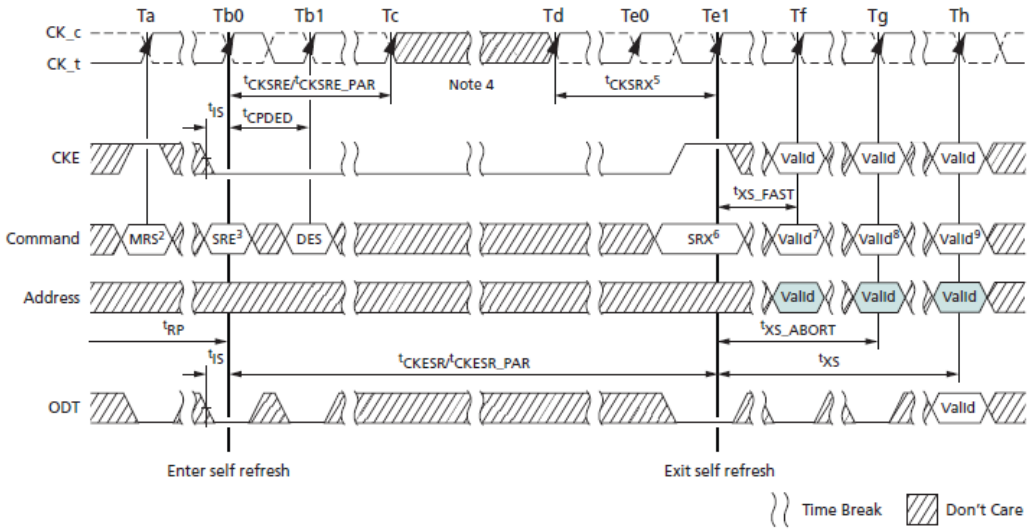
The DLL-off mode is entered by setting MR1 bit A0 to 0; this will disable the DLL for subsequent operations until the A0 bit is set back to 1.

DLL Switch Sequence from DLL-On to DLL-Off

To switch from DLL-on to DLL-off requires the frequency to be changed during self refresh, as outlined in the following procedure:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and, to disable the DLL, the DRAM on-die termination resistors, $R_{TT(NOM)}$, must be in High-Z before MRS to MR1.)
2. Set MR1 bit A0 to 1 to disable the DLL.
3. Wait ^{t}MOD.
4. Enter self refresh mode; wait until ^{t}CKSRE/^{t}CKSRE_PAR is satisfied.
5. Change frequency, following the guidelines in the Input Clock Frequency Change section.
6. Wait until a stable clock is available for at least tCKSRX at device inputs.
7. Starting with the SELF REFRESH EXIT command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If $R_{TT(NOM)}$ was disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
8. Wait ^{t}XS_FAST, ^{t}XS_ABORT, or ^{t}XS, and then set mode registers with appropriate values (an update of CL, CWL, and WR may be necessary; a ZQCL command can also be issued after ^{t}XS_FAST).
   - ^{t}XS_FAST: ZQCL, ZQCS, and MRS commands. For MRS commands, only CL and WR/RTP registers in MR0, the CWL register in MR2, and gear-down mode in MR3 may be accessed provided the device is not in per-DRAM addressability mode. Access to other device mode registers must satisfy ^{t}XS timing.
   - ^{t}XS_ABORT: If MR4 [9] is enabled, then the device aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of ^{t}XS_ABORT.
     Upon exiting from self refresh, the device requires a minimum of one extra REFRESH command before it is put back into self refresh mode. This requirement remains the same regardless of the MRS bit setting for self refresh abort.
   - ^{t}XS: ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, and RDAS8.
9. Wait ^{t}MOD to complete.
   The device is ready for the next command.

Figure 9. DLL Switch Sequence from DLL-On to DLL-Off



Notes:

1. Starting in the idle state. R_{TT} in stable state.
2. Disable DLL by setting MR1 bit A0 to 0.
3. Enter SR.
4. Change frequency.
5. Clock must be stable ^{t}CKSRX.
6. Exit SR.
7. Update mode registers allowed with DLL-off settings met.

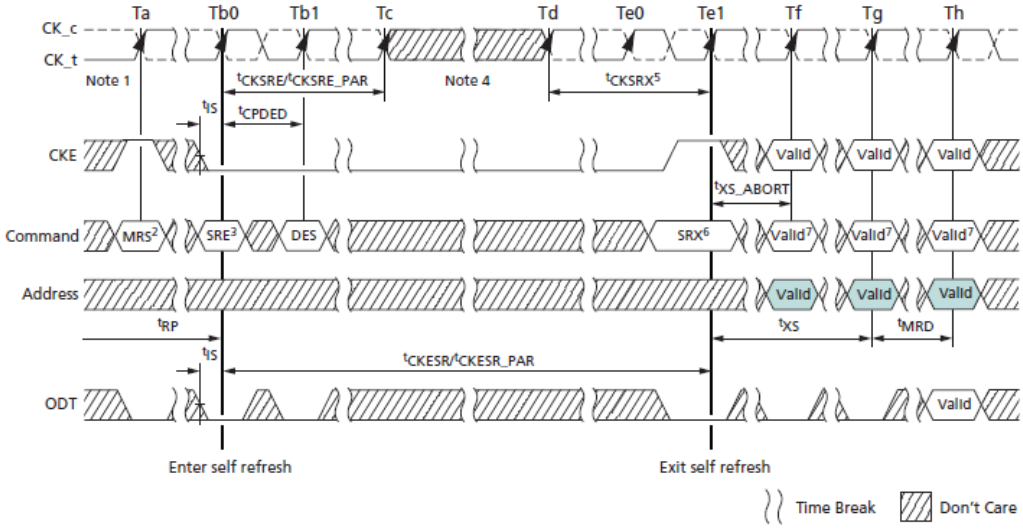
DLL-Off to DLL-On Procedure

To switch from DLL-off to DLL-on (with required frequency change) during self refresh:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and DRAM ODT resistors ($R_{TT(NOM)}$) must be in High-Z before self refresh mode is entered.)
2. Enter self refresh mode; wait until tCKSRE/tCKSRE_PAR are satisfied.
3. Change frequency (following the guidelines in the Input Clock Frequency Change section).
4. Wait until a stable clock is available for at least ^{t}CKSRX at device inputs.
5. Starting with the SELF REFRESH EXIT command, CKE must continuously be registered HIGH until ^{t}DLLK timing from the subsequent DLL RESET command is satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW or HIGH until ^{t}DLLK timing from the subsequent DLL RESET command is satisfied. If $R_{TT(NOM)}$ disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
6. Wait ^{t}XS or ^{t}XS_ABORT, depending on bit 9 in MR4, then set MR1 bit A0 to 0 to enable the DLL.
7. Wait ^{t}MRD, then set MR0 bit A8 to 1 to start DLL reset.
8. Wait ^{t}MRD, then set mode registers with appropriate values; an update of CL, CWL, and WR may be necessary. After ^{t}MOD is satisfied from any proceeding MRS command, a ZQCL command can also be issued during or after ^{t}DLLK.
9. Wait for ^{t}MOD to complete. Remember to wait ^{t}DLLK after DLL RESET before applying any command requiring a locked DLL. In addition, wait for ^{t}ZQoper in case a ZQCL command was issued.

The device is ready for the next command.

Figure 10. DLL Switch Sequence from DLL-Off to DLL-On



Notes:

1. Starting in the idle state.
2. Enter SR.
3. Change frequency.
4. Clock must be stable ^{t}CKSRX.
5. Exit SR.
6. Set DLL to on by setting MR1 to A0 = 0.
7. Update mode registers.
8. Issue any valid command.

Input Clock Frequency Change

After the device is initialized, it requires the clock to be stable during almost all states of normal operation.

This means that after the clock frequency has been set and is in the stable state, the clock period is not allowed to deviate except for what is allowed by the clock jitter and spread spectrum clocking (SSC) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate only when in self refresh mode. Outside of self refresh mode, it is illegal to change the clock frequency.

After the device has been successfully placed in self refresh mode and ^{t}CKSRE/^{t}CKSRE_PAR have been satisfied, the state of the clock becomes a “Don’t care.” Following a “Don’t care,” changing the clock frequency is permissible, provided the new clock frequency is stable prior to ^{t}CKSRX. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met as outlined in SELF REFRESH Operation.

For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4, MR5, and MR6 may need to be issued to program appropriate CL, CWL, gear-down mode, READ and WRITE preamble, Command Address Latency, and data rate values.

When the clock rate is being increased (faster), the MR settings that require additional clocks should be updated prior to the clock rate being increased. In particular, the PL latency must be disabled when the clock rate changes, ie. while in self refresh mode. For example, if changing the clock rate from DDR4-2133 to DDR4-2933 with CA parity mode enabled, MR5[2:0] must first change from PL = 4 to PL = disable prior to PL = 6. The correct procedure would be to (1) change PL = 4 to disable via MR5 [2:0], (2) enter self refresh mode, (3) change clock rate from DDR4-2133 to DDR4-2933, (4) exit self refresh mode, (5) Enable CA parity mode setting PL = 6 vis MR5 [2:0].

If the MR settings that require additional clocks are updated after the clock rate has been increased, for example. after exiting self refresh mode, the required MR settings must be updated prior to removing the DRAM from the IDLE state, unless the DRAM is RESET. If the DRAM leaves the IDLE state to enter self refresh mode or ZQ Calibration, the updating of the required MR settings may be deferred to the next time the DRAM enters the IDLE state.

If MR6 is issued prior to self refresh entry for the new data rate value, DLL will relock automatically at self refresh exit. However, if MR6 is issued after self refresh entry, MR0 must be issued to reset the DLL.

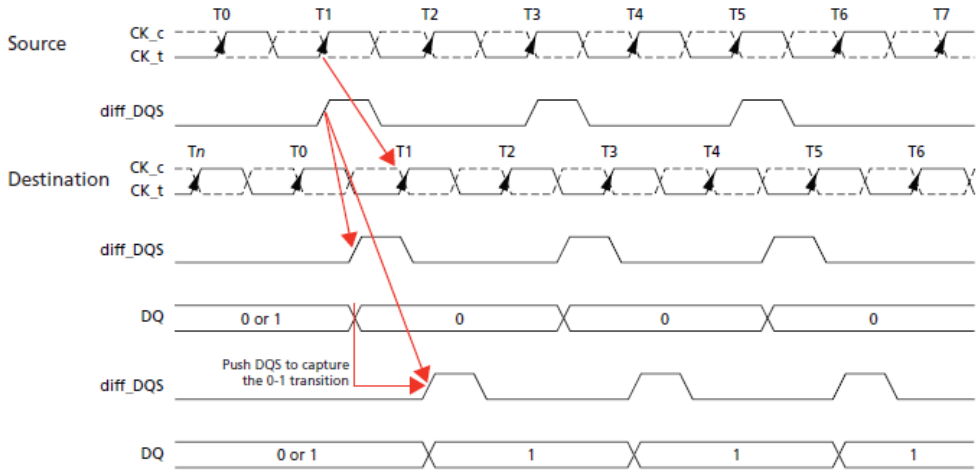
The device input clock frequency can change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL-on mode to DLL-off mode transition sequence (see DLL-On/Off Switching Procedures).

Write Leveling

For better signal integrity, DDR4 memory modules use fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology has benefits from the reduced number of stubs and their length, but it also causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain ^{t}DQSS, ^{t}DSS, and ^{t}DSH specifications. Therefore, the device supports a write leveling feature to allow the controller to compensate for skew. This feature may not be required under some system conditions, provided the host can maintain the ^{t}DQSS, ^{t}DSS, and ^{t}DSH specifications.

The memory controller can use the write leveling feature and feedback from the device to adjust the DQS (DQS_t, DQS_c) to CK (CK_t, CK_c) relationship. The memory controller involved in the leveling must have an adjustable delay setting on DQS to align the rising edge of DQS with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK, sampled with the rising edge of DQS, through the DQ bus. The controller repeatedly delays DQS until a transition from 0 to 1 is detected. The DQS delay established though this exercise would ensure the ^{t}DQSS specification. Besides ^{t}DQSS, ^{t}DSS and ^{t}DSH specifications also need to be fulfilled. One way to achieve this is to combine the actual ^{t}DQSS in the application with an appropriate duty cycle and jitter on the DQS signals. Depending on the actual ^{t}DQSS in the application, the actual values for ^{t}DQSL and ^{t}DQSH may have to be better than the absolute limits provided in the AC Timing Parameters section in order to satisfy ^{t}DSS and ^{t}DSH specifications. A conceptual timing of this scheme is shown below.

Figure 11. Write Leveling Concept, Example 1

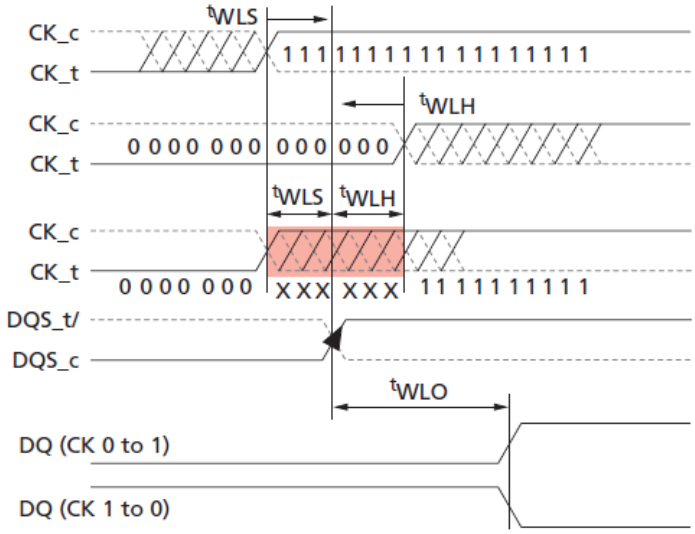


DQS driven by the controller during leveling mode must be terminated by the DRAM based on the ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits carry the leveling feedback to the controller across the DRAM configurations: x4, x8, and x16. On a x16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS (diff_UDQS)-to-clock relationship; the lower data bits would indicate the lower diff_DQS (diff_LDQS)-to-clock relationship.

The figure below is another representative way to view the write leveling procedure. Although it shows the clock varying to a static strobe, this is for illustrative purpose only; the clock does not actually change phase, the strobe is what actually varies. By issuing multiple WL bursts, the DQS strobe can be varied to capture with fair accuracy the time at which the clock edge arrives at the DRAM clock input buffer.

Figure 12. Write Leveling Concept, Example 1



DRAM Setting for Write Leveling and DRAM TERMINATION Function in that Mode

The DRAM enters into write leveling mode if A7 in MR1 is HIGH. When leveling is finished, the DRAM exits write leveling mode if A7 in MR1 is LOW (see the MR Leveling Procedures table). Note that in write leveling mode, only DQS terminations are activated and deactivated via the ODT pin, unlike normal operation (see DRAM DRAM TERMINATION Function in Leveling Mode table).

Table 24. MR Settings for Leveling Procedures

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Q off)	A12	0	1

Table 25. DRAM TERMINATION Function in Leveling Mode

ODT Pin at DRAM	DQS_t/DQS_c Termination	DQ Termination
$R_{TT(NOM)}$ with ODT HIGH	On	Off
$R_{TT(Park)}$ with ODT LOW	On	Off

Notes:

1. In write leveling mode, with the mode's output buffer either disabled (MR1[bit7] = 1 and MR1[bit12] = 1) or with its output buffer enabled (MR1[bit7] = 1 and MR1[bit12] = 0), all $R_{TT(NOM)}$ and $R_{TT(Park)}$ settings are supported.
2. $R_{TT(WR)}$ is not allowed in write leveling mode and must be set to disable prior to entering write leveling mode.

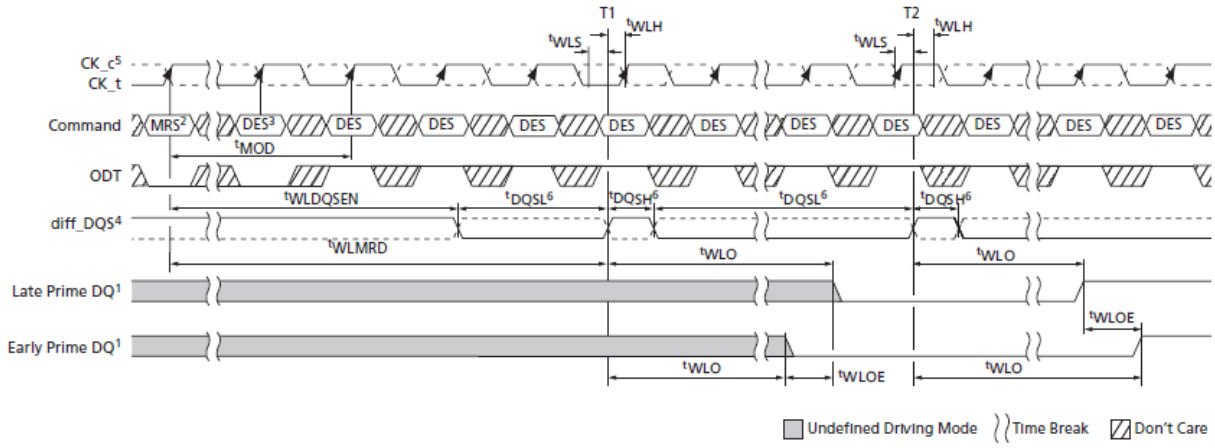
Procedure Description

The memory controller initiates the leveling mode of all DRAM by setting bit 7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only the DESELECT command is supported, other than MRS commands to change the Qoff bit (MR1[A12]) and to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7] = 0) may also change the other MR1 bits. Because the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal, unless DODTLon or DODTLoff have been altered (the ODT internal pipe delay is increased when increasing WRITE latency [WL] or READ latency [RL] by the previous MR command), then ODT assertion should be delayed by DODTLon after ^{t}MOD is satisfied, which means the delay is now ^{t}MOD + DODTLon.

The controller may drive DQS_t LOW and DQS_c HIGH after a delay of ^{t}WLDQSEN, at which time the DRAM has applied ODT to these signals. After ^{t}DQSL and ^{t}WLMRD, the controller provides a single DQS_t, DQS_c edge, which is used by the DRAM to sample CK driven from the controller. ^{t}WLMRD (MAX) timing is controller dependent.

The DRAM samples CK status with the rising edge of DQS and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of ^{t}WLOE defined to allow mismatch on DQ bits. The ^{t}WLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS_t, DQS_c) needed for these DQs. The controller samples incoming DQ and either increments or decrements DQS delay setting and launches the next DQS pulse after some time, which is controller dependent. After a 0-to-1 transition is detected, the controller locks the DQS delay setting, and write leveling is achieved for the device. The following figure shows the timing diagram and parameters for the overall write leveling procedure.

Figure 13. Write Leveling Sequence (DQS Capturing CK LOW at T1 and CK HIGH at T2)



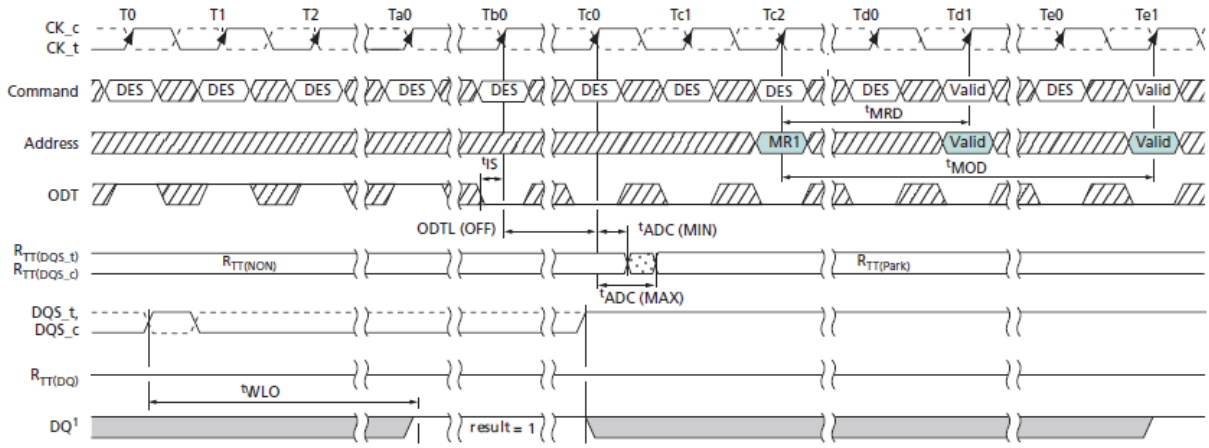
Notes:

1. The device drives leveling feedback on all DQs.
2. MRS: Load MR1 to enter write leveling mode.
3. diff_DQS is the differential data strobe. Timing reference points are the zero crossings. DQS_t is shown with a solid line; DQS_c is shown with a dotted line.
4. CK_t is shown with a solid dark line; CK_c is shown with a dotted line.
5. DQS needs to fulfill minimum pulse width requirements, ^{t}DQSH (MIN) and ^{t}DQSL (MIN), as defined for regular WRITEs; the maximum pulse width is system dependent.
6. ^{t}WLDQSEN must be satisfied following equation when using ODT:
   - DLL = Enable, then ^{t}WLDQSEN > ^{t}MOD (MIN) + DODTLon + ^{t}ADC
   - DLL = Disable, then ^{t}WLDQSEN > ^{t}MOD (MIN) + ^{t}AONAS

Write Leveling Mode Exit

Write leveling mode should be exited as follows:
1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note that from this point on, DQ pins are in undefined driving mode and will remain undefined, until tMOD after the respective MR command (Te1).
2. Drive ODT pin LOW (^{t}IS must be satisfied) and continue registering LOW (see Tb0).
3. After R_{TT} is switched off, disable write leveling mode via the MRS command (see Tc2).
4. After ^{t}MOD is satisfied (Te1), any valid command can be registered. (MR commands can be issued after ^{t}MRD [Td1]).

Figure 14. Write Leveling Exit

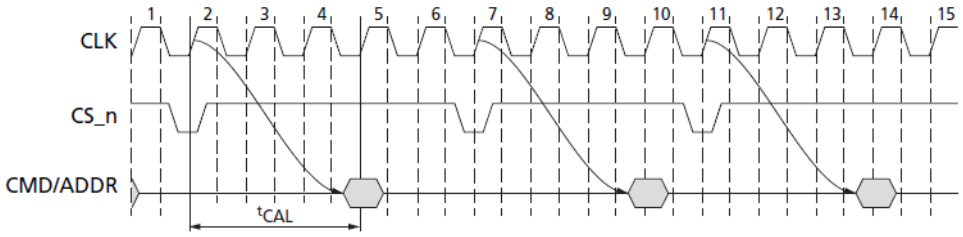


Notes:
1. The DQ result = 1 between Ta0 and Tc0 is a result of the DQS signals capturing CK_t HIGH just after the T0 state.
2. See previous figure for specific ^{t}WLO timing.

Command Address Latency

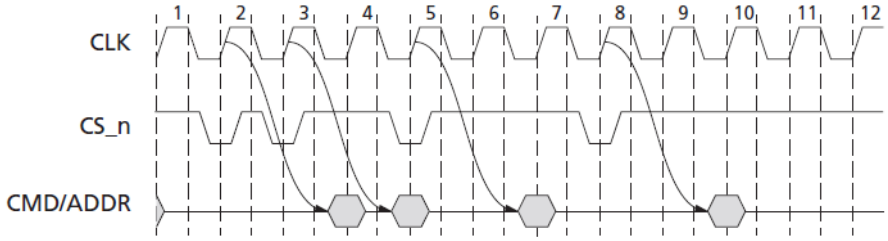
DDR4 supports the command address latency (CAL) function as a power savings feature. This feature can be enabled or disabled via the MRS setting. CAL timing is defined as the delay in clock cycles (^{t}CAL) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL in clocks must be programmed into the mode register (see MR1 Register Definition table) and is based on the ^{t}CAL(ns)/^{t}CK(ns) rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section.

Figure 15. CAL Timing Definition



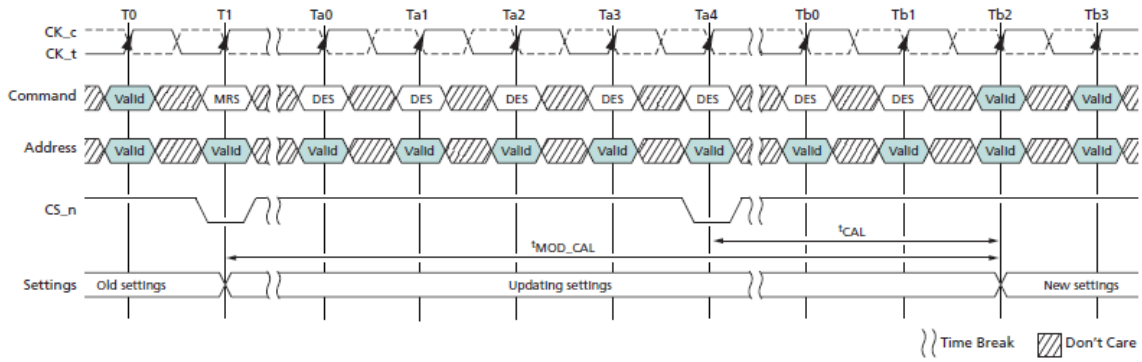
CAL gives the DRAM time to enable the command and address receivers before a command is issued.
After the command and the address are latched, the receivers can be disabled if CS_n returns to HIGH.
For consecutive commands, the DRAM will keep the command and address input receivers enabled for the duration of the command sequence.

Figure 16. CAL Timing Example (Consecutive CS_n = LOW)



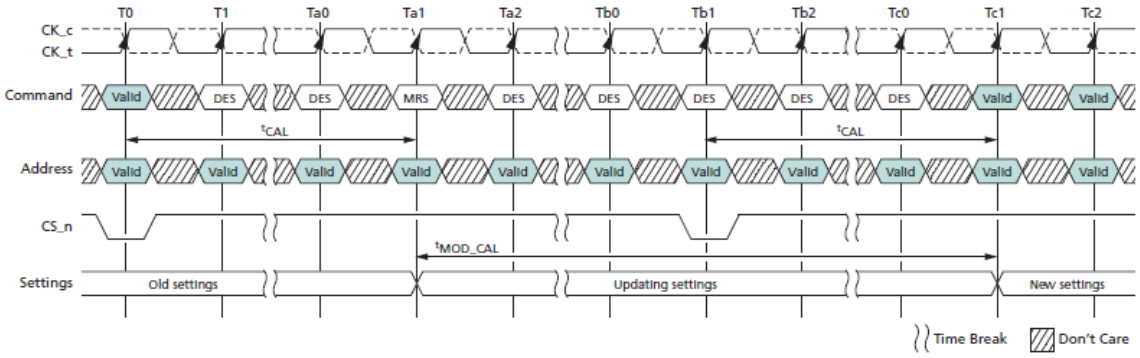
When the CAL mode is enabled, additional time is required for the MRS command to complete. The earliest the next valid command can be issued is ^{t}MOD_CAL, which should be equal to ^{t}MOD + ^{t}CAL.
The two following figures are examples.

Figure 17. CAL Enable Timing - ^{t}MOD_CAL



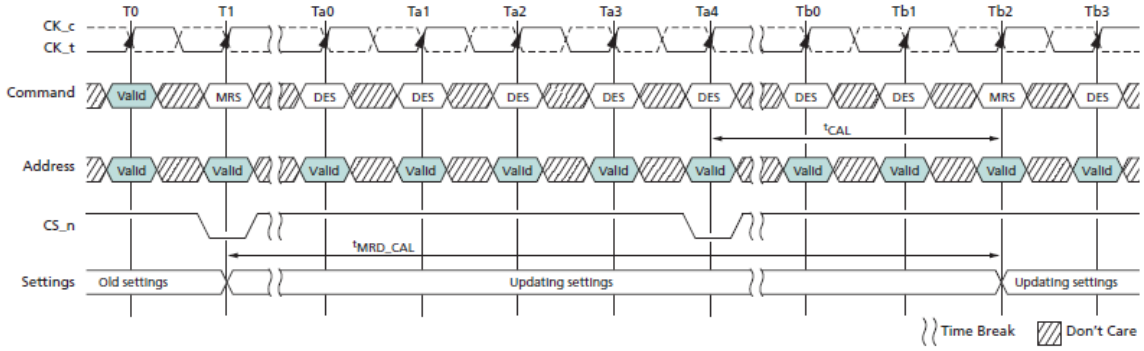
Notes: 1. CAL mode is enabled at T1.

Figure 18. ^{t}MOD_CAL, MRS to Valid Command Timing with CAL Enabled



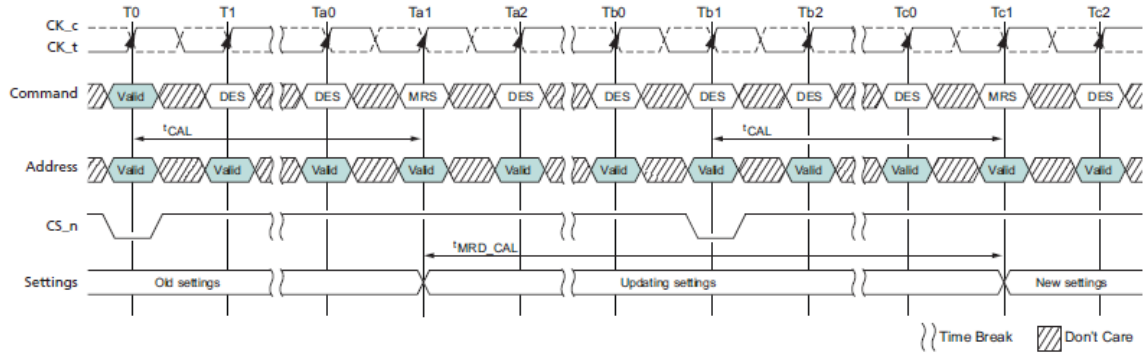
Note: 1. MRS at Ta1 may or may not modify CAL, ^{t}MOD_CAL is computed based on new ^{t}CAL setting if modified. When the CAL mode is enabled or being enabled, the earliest the next MRS command can be issued is ^{t}MRD_CAL is equal to ^{t}MOD + ^{t}CAL. The two following figures are examples.

Figure 19. CAL Enabling MRS to Next MRS Command, ^{t}MRD_CAL



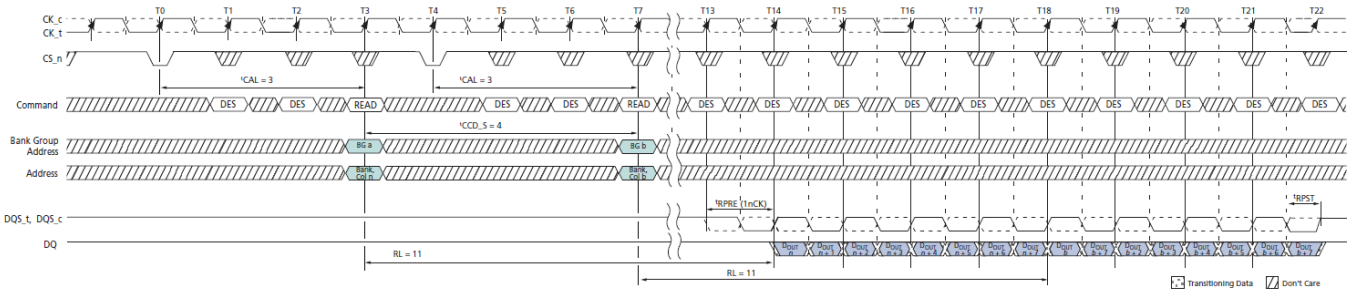
Note: 1. Command address latency mode is enabled at T1.

Figure 20. ^{t}MRD_CAL, Mode Register Cycle Time With CAL Enabled



Note: 1. MRS at Ta1 may or may not modify CAL, ^{t}MRD_CAL is computed based on new ^{t}CAL setting if modified. CAL Examples: Consecutive READ BL8 with two different CALs and 1^{t}CK preamble in different bank group shown in the following figures.

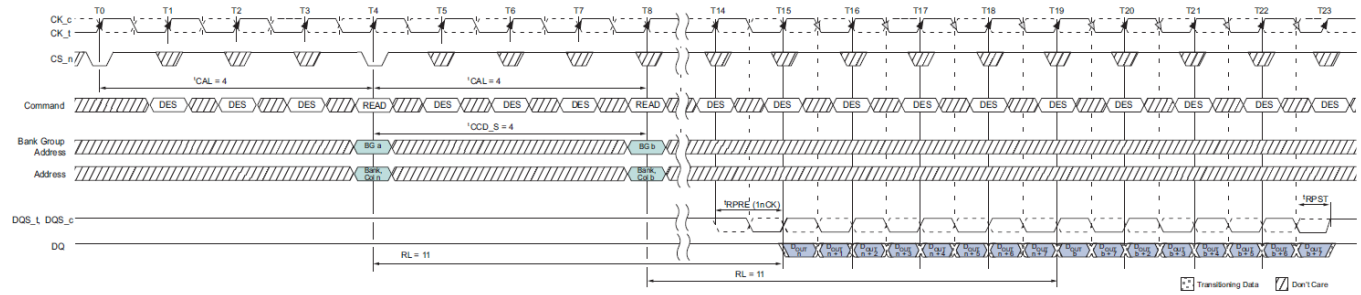
Figure 21. Consecutive READ BL8, CAL3, 1tCK Preamble, Different Bank Group



Notes:

1. BL = 8, AL = 0, CL = 11, CAL = 3, Preamble = 1tCK.
2. D_{OUT} n = data-out from column n; D_{OUT} b = data-out from column b.
3. DES commands are shown for ease of illustration, other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T3 and T7.
5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable.
6. Enabling CAL mode does not impact ODT control timings. ODT control timings should be maintained with the same timing relationship relative to the command/address bus as when CAL is disabled.

Figure 22. Consecutive READ BL8, CAL4, 1tCK Preamble, Different Bank Group



Notes:

1. BL = 8, AL = 0, CL = 11, CAL = 4, Preamble = 1tCK.
2. D_{OUT} n = data-out from column n; D_{OUT} b = data-out from column b.
3. DES commands are shown for ease of illustration, other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T4 and T8.
5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable.
6. Enabling CAL mode does not impact ODT control timings. ODT control timings should be maintained with the same timing relationship relative to the command/address bus as when CAL is disabled.

Low-Power Auto Self Refresh Mode

An auto self refresh mode is provided for application ease. Auto self refresh mode is enabled by setting MR2[6] = 1 and MR2[7] = 1. The device will manage self refresh entry over the supported temperature range of the DRAM. In this mode, the device will change its self refresh rate as the DRAM operating temperature changes, going lower at low temperatures and higher at high temperatures.

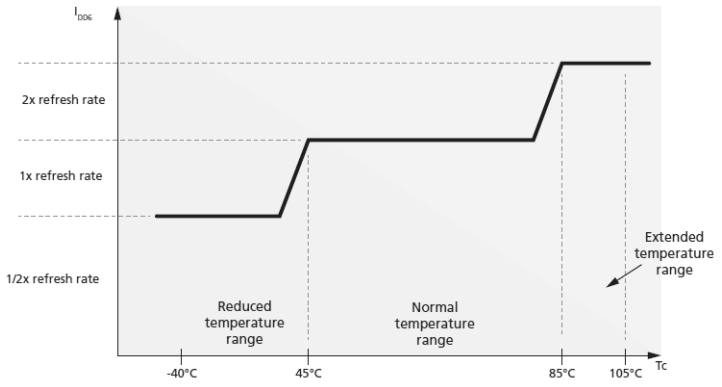
Manual Self Refresh Mode

If auto self refresh mode is not enabled, the low-power auto self refresh mode register must be manually programmed to one of the three self refresh operating modes. This mode provides the flexibility to select a fixed self refresh operating mode at the entry of the self refresh, according to the system memory temperature conditions. The user is responsible for maintaining the required memory temperature condition for the mode selected during the SELF REFRESH operation. The user may change the selected mode after exiting self refresh and before entering the next self refresh. If the temperature condition is exceeded for the mode selected, there is a risk to data retention resulting in loss of data.

Table 26. Auto Self Refresh Mode

MR2[7]	MR2[6]	Low-Power Auto Self Refresh Mode	Self Refresh Operation	Operating Temperature Range for Self Refresh Mode (DRAM T_{CASE})
0	0	Normal	Variable or fixed normal self refresh rate maintains data retention at the normal operating temperature. User is required to ensure that 85°C DRAM T_{CASE} (MAX) is not exceeded to avoid any risk of data loss.	(0°C to 85°C)
1	0	Extended Temperature range	Variable or fixed high self refresh rate optimizes data retention to support the extended temperature range.	(0°C to 95°C)
0	1	Reduced Temperature range	Variable or fixed self refresh rate or any other DRAM power consumption reduction control for the reduced temperature range. User is required to ensure 45°C DRAM T_{CASE} (MAX) is not exceeded to avoid any risk of data loss.	(0°C to 45°C)
1	1	Auto Self Refresh	Auto self refresh mode enabled. Self refresh power consumption and data retention are optimized for any given operating temperature condition.	All of the above

Figure 23. Auto Self Refresh Ranges



Multipurpose Register

The MULTIPURPOSE REGISTER (MPR) function, MPR access mode, is used to write/read specialized data to/from the DRAM. The MPR consists of four logical pages, MPR Page 0 through MPR Page 3, with each page having four 8-bit registers, MPR0 through MPR3. Page 0 can be read by any of three readout modes (serial, parallel, or staggered) while Pages 1, 2, and 3 can be read by only the serial readout mode. Page 3 is for DRAM vendor use only. MPR mode enable and page selection is done with MRS commands. Data bus inversion (DBI) is not allowed during MPR READ operation.

Once the MPR access mode is enabled (MR3[2] = 1), only the following commands are allowed: MRS, RD, RDA WR, WRA, DES, REF, and RESET; RDA/WRA have the same functionality as RD/WR which means the auto precharge part of RDA/WRA is ignored. Power-down mode and SELF REFRESH command are not allowed during MPR enable mode. No other command can be issued within tRFC after a REF command has been issued; 1x refresh (only) is to be used during MPR access mode. While in MPR access mode, MPR read or write sequences must be completed prior to a REFRESH command.

Figure 24. MPR Block Diagram

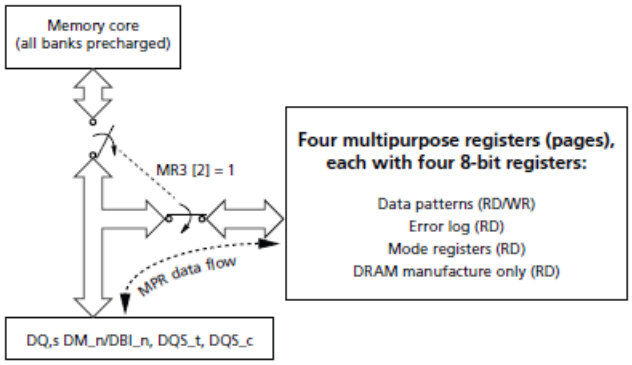


Table 27. MR3 Setting for the MPR Access Mode

Address	Operation Mode	Description
A[12:11]	MPR data read format	00 = Serial ..... 01 = Parallel 10 = Staggered .... 11 = Reserved
A2	MPR access	0 = Standard operation (MPR not enabled) 1 = MPR data flow enabled
A[1:0]	MPR page selection	00 = Page 0 .... 01 = Page 1 10 = Page 2 .... 11 = Page 3

Table 28. DRAM Address to MPR UI Translation

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DRAM address - Ax	A7	A6	A5	A4	A3	A2	A1	A0
MPR UI - UIx	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

Table 29. MPR Page and MPR*x* Definitions

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
MPR Page 0 – Read or Write (Data Patterns)										
BA[1:0]	00 = MPR0	0	1	0	1	0	1	0	1	Read/ Write (default value listed)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	
MPR Page 1 – Read only (Error Log)										
BA[1:0]	00 = MPR0	A7	A6	A5	A4	A3	A2	A1	A0	Read-only
	01 = MPR1	CAS_n /A15	WE_n /A14	A13	A12	A11	A10	A9	A8	
	10 = MPR2	PAR	ACT_n	BG1	BG0	BA1	BA0	A17	RAS_n /A16	
	11 = MPR3	CRC error status	CA parity error status	CA parity latency: [5] = MR5[2], [4] = MR5[1], [3] = MR5[0]			C2	C1	C0	
MPR Page 2 – Read only (MRS Readout)										
BA[1:0]	00 = MPR0	hPPR support	sPPR support	$R_{TT(WR)}$ MR2[11]	Temperature sensor status *2		CRC write enable MR2[12]	$R_{TT(WR)}$ MR2[10:9]		Read-only
	01 = MPR1	V_{REFDQ} trainging range MR6[6]	V_{REFDQ} training value: [6:1] = MR6[5:0]						Gear-down enable MR3[3]	
	10 = MPR2	CAS latency: [7:3] = MR0[6:4,2,12]						CAS write latency [2:0] = MR2[5:3]		
	11 = MPR3	$R_{TT(NOM)}$: [7:5] = MR1[10:8]			$R_{TT(Park)}$: [4:2] = MR5[8:6]			R_{ON}: [1:0] = MR1[2:1]		
MPR Page 3 – Read only (Restricted, except for MPR3 [3:0])										
BA[1:0]	00 = MPR0	DC	DC	DC	DC	DC	DC	DC	DC	Read-only
	01 = MPR1	DC	DC	DC	DC	DC	DC	DC	DC	
	10 = MPR2	DC	DC	DC	DC	DC	DC	DC	DC	
	11 = MPR3	MBIST-PPR Support	DC	MBIST-PPR Transparency		MAC	MAC	MAC	MAC	

Notes:

1. DC = "Don't Care"
2. MPR[4:3] 00 = Sub 1X refresh; MPR[4:3] 01 = 1X refresh; MPR[4:3] 10 = 2X refresh; MPR[4:3] 11 = Reserved.

MPR Reads

MPR reads are supported using BL8 and BC4 modes. Burst length on-the-fly is not supported for MPR reads. Data bus inversion (DBI) is not allowed during MPR READ operation; the device will ignore the Read DBI enable setting in MR5 [12] when in MPR mode. READ commands for BC4 are supported with a starting column address of A[2:0] = 000 or 100. After power-up, the content of MPR Page 0 has the default values, which are defined in MPR Page and MPRx Definitions. MPR page 0 can be rewritten via an MPR WRITE command. The device maintains the default values unless it is rewritten by the DRAM controller. If the DRAM controller does overwrite the default values (Page 0 only), the device will maintain the new values unless re-initialized or there is power loss.

Timing in MPR mode:

- Reads (back-to-back) from Page 0 may use ^{t}CCD_S or ^{t}CCD_L timing between READ commands
- Reads (back-to-back) from Pages 1, 2, or 3 may not use ^{t}CCD_S timing between READ commands; ^{t}CCD_L must be used for timing between READ commands

The following steps are required to use the MPR to read out the contents of a mode register (MPR Page *x*, MPR*y*).

1. The DLL must be locked if enabled.
2. Precharge all; wait until tRP is satisfied.
3. MRS command to MR3[2] = 1 (Enable MPR data flow), MR3[12:11] = MPR read format, and MR3[1:0] MPR page.
   a) MR3[12:11] MPR read format:
      i) 00 = Serial read format
      ii) 01 = Parallel read format
      iii) 10 = staggered read format
      iv) 11 = RFU

   b) MR3[1:0] MPR page:
      i) 00 = MPR Page 0
      ii) 01 = MPR Page 1
      iii) 10 = MPR Page 2
      iv) 11 = MPR Page 3
4. ^{t}MRD and ^{t}MOD must be satisfied.
5. Redirect all subsequent READ commands to specific MPR*x* location.
6. Issue RD or RDA command.
   a) BA1 and BA0 indicate MPR*x* location:
      i) 00 = MPR0
      ii) 01 = MPR1
      iii) 10 = MPR2
      iv) 11 = MPR3
   b) A12/BC = 0 or 1; BL8 or BC4 fixed-only, BC4 OTF not supported.
      i) If BL = 8 and MR0 A[1:0] = 01, A12/BC must be set to 1 during MPR READ commands.
   c) A2 = burst-type dependant:
      i) BL8: A2 = 0 with burst order fixed at 0, 1, 2, 3, 4, 5, 6, 7
      ii) BL8: A2 = 1 not allowed
      iii) BC4: A2 = 0 with burst order fixed at 0, 1, 2, 3, T, T, T, T
      iv) BC4: A2 = 1 with burst order fixed at 4, 5, 6, 7, T, T, T, T
   d) A[1:0] = 00, data burst is fixed nibble start at 00.
   e) Remaimimg address inputs, including A10, and BG1 and BG0 are “Don’t Care.”
7. After RL = AL + CL, DRAM bursts data from MPR*x* location; MPR readout format determined by MR3[A12,11,1,0].
8. Steps 5 through 7 may be repeated to read additional MPR*x* locations.
9. After the last MPR*x* READ burst, ^{t}MPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3[2] = 0.
11. After the tMOD sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

MPR Readout Format

The MPR read data format can be set to three different settings: serial, parallel, and staggered.

MPR Readout Serial Format

The serial format is required when enabling the MPR function to read out the contents of an MR*x*, temperature sensor status, and the command address parity error frame. However, data bus calibration locations (four 8-bit registers) can be programmed to read out any of the three formats. The DRAM is required to drive associated strobes with the read data similar to normal operation (such as using MRS preamble settings).
Serial format implies that the same pattern is returned on all DQ lanes, as shown the table below, which uses values programmed into the MPR via [7:0] as 0111 1111.

Table 30. MPR Readout Serial Format

Serial (x16 device)	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

MPR Readout Parallel Format

Parallel format implies that the MPR data is returned in the first data UI and then repeated in the remaining UIs of the burst, as shown in the table below. Data pattern location 0 is the only location used for the parallel format. RD/RDA from data pattern locations 1, 2, and 3 are not allowed with parallel data return mode. In this example, the pattern programmed in the data pattern location 0 is 0111 1111. The x4 configuration only outputs the first four bits (0111 in this example). For the x16 configuration, the same pattern is repeated on both the upper and lower bytes.

Table 31. MPR Readout – Parallel Format

Parallel (x16 device)	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
DQ8	0	0	0	0	0	0	0	0
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

MPR Readout Staggered Format

Staggered format of data return is defined as the staggering of the MPR data across the lanes. In this mode, an RD/RDA command is issued to a specific data pattern location and then the data is returned on the DQ from each of the different data pattern locations. For the x4 configuration, an RD/RDA to data pattern location 0 will result in data from location 0 being driven on DQ0, data from location 1 being driven on DQ1, data from location 2 being driven on DQ2, and so on, as shown below. Similarly, an RD/RDA command to data pattern location 1 will result in data from location 1 being driven on DQ0, data from location 2 being driven on DQ1, data from location 3 being driven on DQ2, and so on.

Examples of different starting locations are also shown.

It is expected that the DRAM can respond to back-to-back RD/RDA commands to the MPR for all DDR4 frequencies so that a sequence (such as the one that follows) can be created on the data bus with no bubbles or clocks between read data. In this case, the system memory controller issues a sequence of RD(MPR0), RD(MPR1), RD(MPR2), RD(MPR3), RD(MPR0), RD(MPR1), RD(MPR2), and RD(MPR3).

For the x8 configuration, the same pattern is repeated on the lower nibble as on the upper nibble. READs to other MPR data pattern locations follow the same format as the x4 case. A read example to MPR0 for x8 and x16 configurations is shown below.

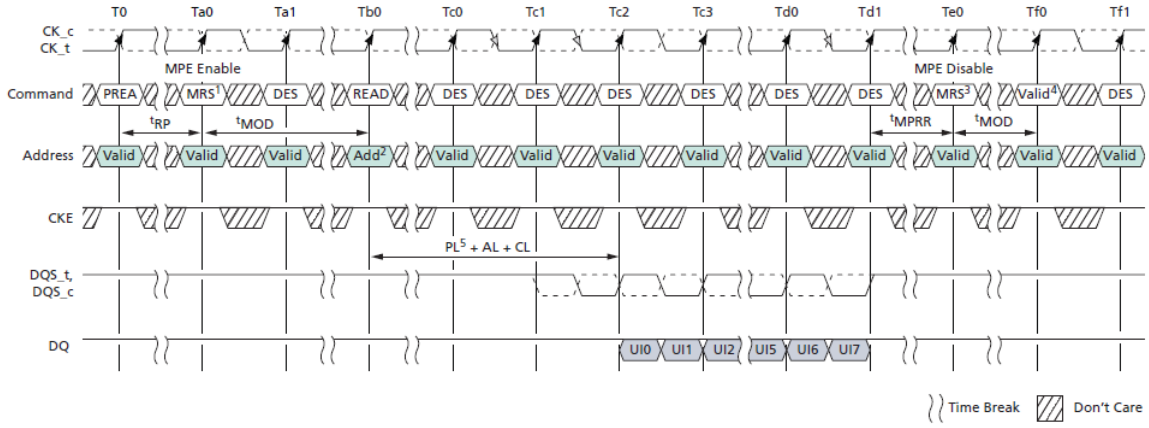
Table 32. MPR Readout Staggered Format

x16 READ MPR0 Command	
Stagger	**UI[7:0]**
DQ0	MPR0
DQ1	MPR1
DQ2	MPR2
DQ3	MPR3
DQ4	MPR0
DQ5	MPR1
DQ6	MPR2
DQ7	MPR3
DQ8	MPR0
DQ9	MPR1
DQ10	MPR2
DQ11	MPR3
DQ12	MPR0
DQ13	MPR1
DQ14	MPR2
DQ15	MPR3

MPR READ Waveforms

The following waveforms show MPR read accesses.

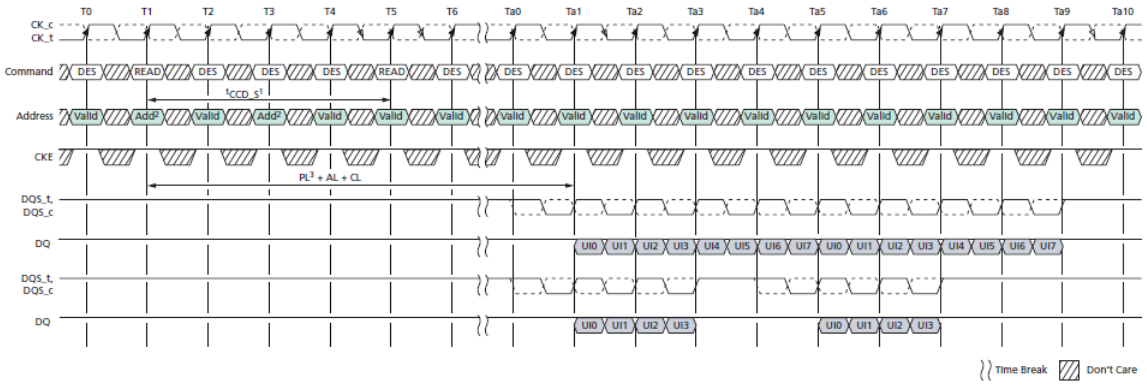
Figure 25. MPR READ Timing



Notes:

1. ^{t}CCD_S = 4^{t}CK, Read Preamble = 1^{t}CK.
2. Address setting:
   A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
   A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are “Don’t Care,” including BG1 and BG0. A12 is “Don’t Care.” when MR0 A[1:0] = 00 or 10 and must be 1b when MR0 A[1:0] = 01
3. Multipurpose registers read/write disable (MR3 A2 = 0).
4. Continue with regular DRAM command.
5. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

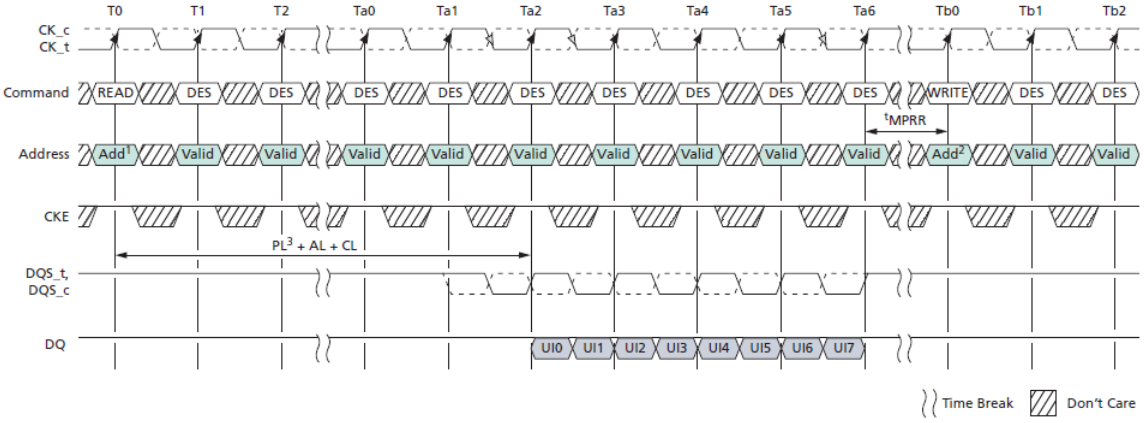
Figure 26. MPR Back-to-Back READ Timing



Notes:

1. ^{t}CCD_S = 4^{t}CK, Read Preamble = 1^{t}CK.
2. Address setting:
   A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
   A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7; for BC = 4, burst order is fixed at 0, 1, 2, 3, T, T, T, T)
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are “Don’t Care,” including BG1 and BG0. A12 is “Don’t Care.” when MR0 A[1:0] = 00 or 10 and must be 1b when MR0 A[1:0] = 01
3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

Figure 27. MPR READ-to-WRITE Timing



Notes:

1. Address setting:
   A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
   A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are “Don’t Care,” including BG1 and BG0. A12 is “Don’t Care.” when MR0 A[1:0] = 00 and must be 1b when MR0 A[1:0] = 01
2. Address setting:
   BA1 and BA0 indicate the MPR location
   A[7:0] = data for MPR
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are “Don’t Care”
3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

MPR Writes

MPR access mode allows 8-bit writes to the MPR Page 0 using the address bus A[7:0]. Data bus inversion (DBI) is not allowed during MPR WRITE operation. The DRAM will maintain the new written values unless re-initialized or there is power loss.

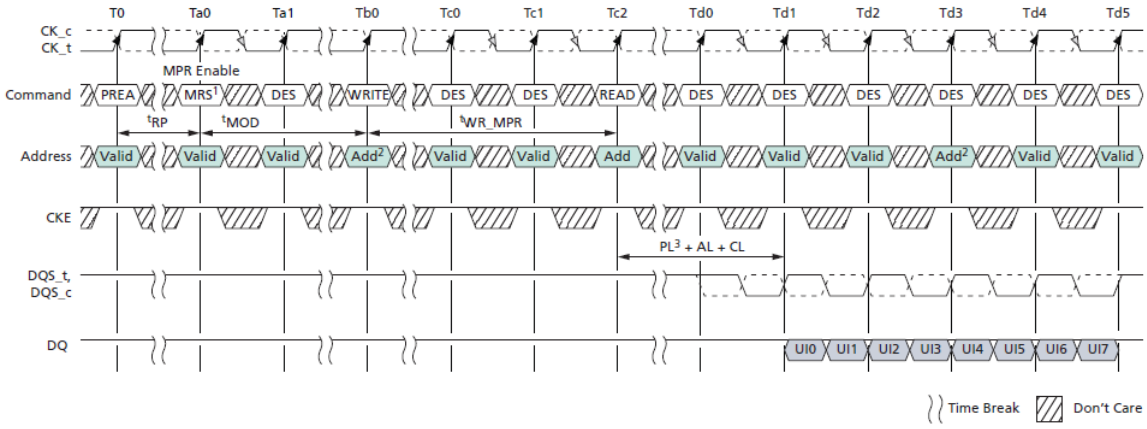
The following steps are required to use the MPR to write to mode register MPR Page 0.

1. The DLL must be locked if enabled.
2. Precharge all; wait until tRP is satisfied.
3. MRS command to MR3[2] = 1 (enable MPR data flow) and MR3[1:0] = 00 (MPR Page 0); writes to 01, 10, and 11 are not allowed.
4. ^{t}MRD and ^{t}MOD must be satisfied.
5. Redirect all subsequent WRITE commands to specific MPR*x* location.
6. Issue WR or WRA command:
   a) BA1 and BA0 indicate MPR*x* location
      i) 00 = MPR0
      ii) 01 = MPR1
      iii) 10 = MPR2
      iv) 11 = MPR3
   b) A[7:0] = data for MPR Page 0, mapped A[7:0] to UI[7:0].
   c) Remaimimg address inputs, including A10, and BG1 and BG0 are “Don’t Care.”
7. ^{t}WR_MPR must be satisfied to complete MPR WRITE.
8. Steps 5 through 7 may be repeated to write additional MPR*x* locations.
9. After the last MPR*x* WRITE, ^{t}MPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3[2] = 0.
11. When the ^{t}MOD sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

MPR WRITE Waveforms

The following waveforms show MPR write accesses.

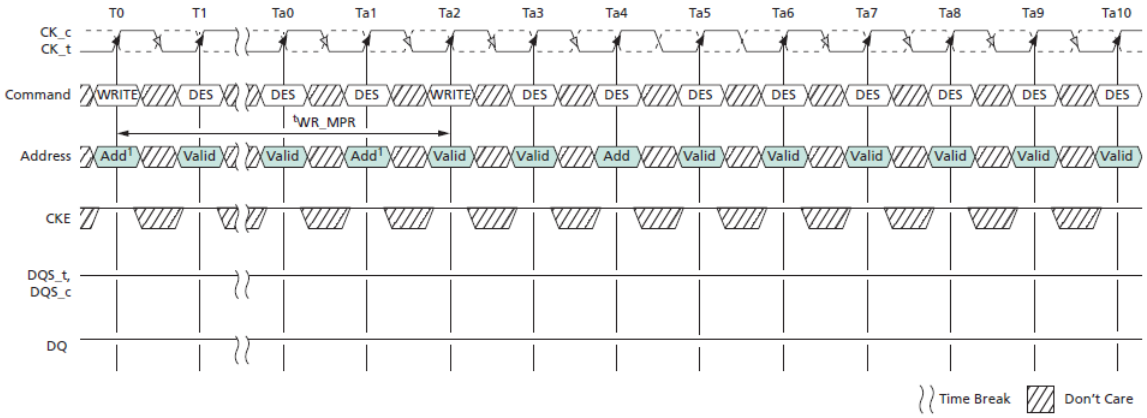
Figure 28. MPR WRITE and WRITE-to-READ Timing



Notes:

1. Multipurpose registers read/write enable (MR3 A2 = 1).
2. Address setting:
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are “Don’t Care”
3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

Figure 29. MPR Back-to-Back WRITE Timing



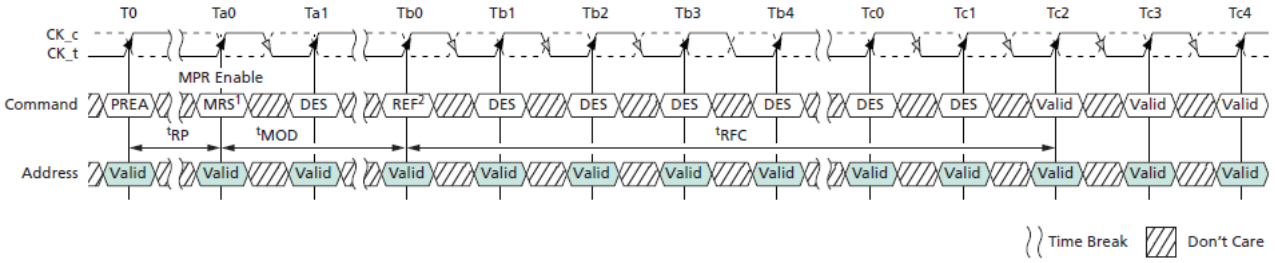
Notes:

1. Address setting:
   BA1 and BA0 indicate the MPR location
   A[7:0] = data for MPR
   A10 and other address pins are “Don’t Care”

MPR REFRESH Waveforms

The following waveforms show MPR accesses interaction with refreshes.

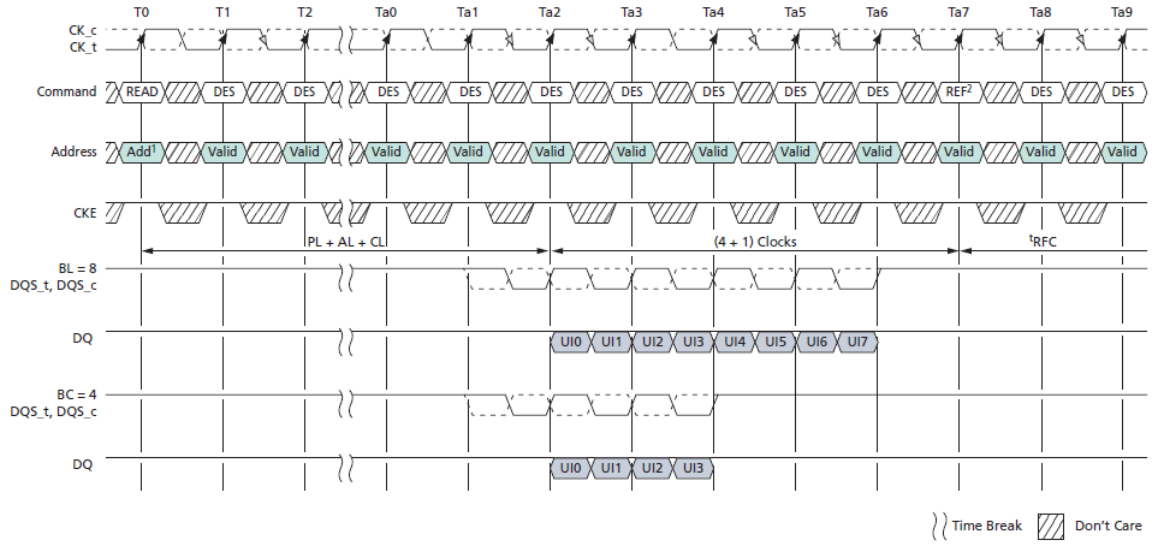
Figure 30. REFRESH Timing



Notes:

1. Multipurpose registers read/write enable (MR3 A2 = 1). Redirect all subsequent read and writes to MPR locations.
2. 1x refresh is only allowed when MPR mode is enabled.

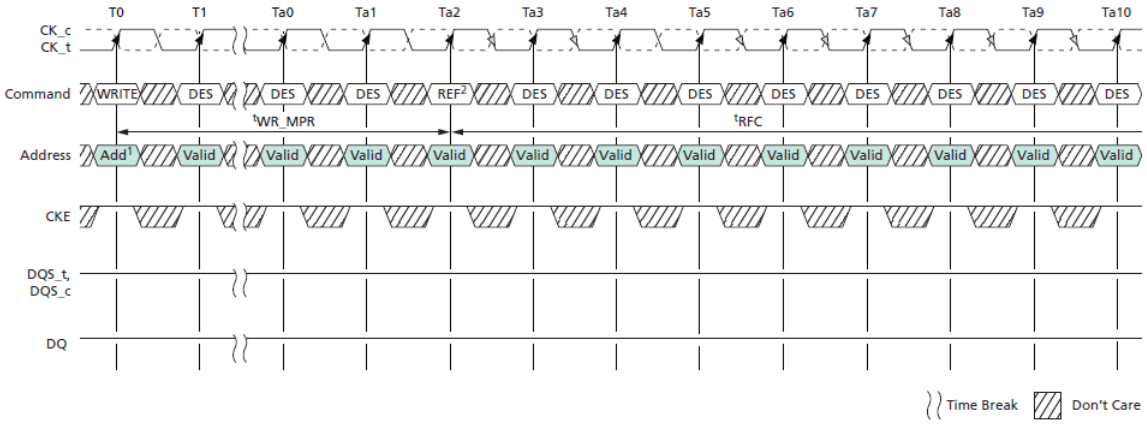
Figure 31. READ-to-REFRESH Timing



Notes:

1. Address setting:
   A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
   A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care." when MR0 A[1:0] = 00 or 10, and must be 1b when MR0 A[1:0] = 01
2. 1x refresh is only allowed when MPR mode is enabled.

Figure 32. WRITE-to-REFRESH Timing



Notes:

1. Address setting:
   BA1 and BA0 indicate the MPR location
   A[7:0] = data for MPR
   A10 and other address pins are “Don’t Care”
2. 1x refresh is only allowed when MPR mode is enabled.

Gear-Down Mode

The DDR4 SDRAM defaults in 1/2 rate (1N) clock mode and uses a low-frequency MRS command (the RS command has relaxed setup and hold) followed by a sync pulse (first CS pulse after MRS setting) to align the proper clock edge for operating the control lines CS_n, CKE, and ODT when in 1/4 rate (2N) mode. Gear-down mode is only supported at DDR4-2666 and faster. For operation in 1/2 rate mode, neither an MRS command or a sync pulse is required. Gear-down mode may only be entered during initialization or self refresh exit and may only be exited during self refresh exit. CAL mode and CA parity mode must be disabled prior to gear-down mode entry. The two modes may be enabled after ^{t}SYNC_ GEAR and ^{t}CMD_GEAR periods have been satisfied. The general sequence for operation in 1/4 rate during initialization is as follows:

1. The device defaults to a 1N mode internal clock at power-up/reset.
2. Assertion of reset.
3. Assertion of CKE enables the DRAM.
4. MRS is accessed with a low-frequency N tCK gear-down MRS command. (N^{t}CK static MRS command is qualified by 1N CS_n.)
5. The memory controller will send a 1N sync pulse with a low-frequency N x ^{t}CK NOP command. ^{t}SYNC_GEAR is an even number of clocks. The sync pulse is on an even edge clock boundary from the MRS command.
6. Initialization sequence, including the expiration of ^{t}DLLK and ^{t}ZQinit, starts in 2N mode after ^{t}CMD_GEAR from 1N sync pulse.

The device resets to 1N gear-down mode after entering self refresh. The general sequence for operation in gear-down after self refresh exit is as follows:

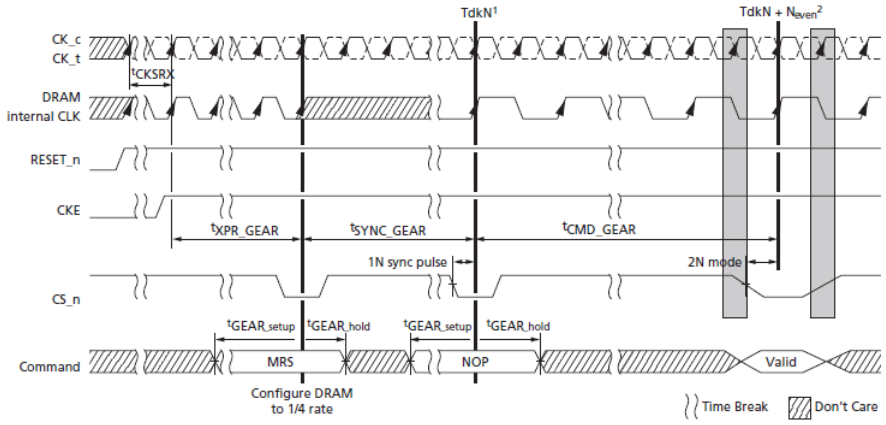
1. MRS is set to 1, via MR3[3], with a low-frequency N tCK gear-down MRS command.
   a) The N^{t}CK static MRS command is qualified by 1N CS_n, which meets ^{t}XS or ^{t}XS_ABORT.
   b) Only a REFRESH command may be issued to the DRAM before the N^{t}CK static MRS command.
2. The DRAM controller sends a 1N sync pulse with a low-frequency N x ^{t}CK NOP command.
   a) ^{t}SYNC_GEAR is an even number of clocks.
   b) The sync pulse is on even edge clock boundary from the MRS command.
3. A valid command not requiring locked DLL is available in 2N mode after ^{t}CMD_GEAR from the 1N sync pulse.
   a) A valid command requiring locked DLL is available in 2N mode after ^{t}XSDLL or ^{t}DLLK from the 1N sync pulse.
4. If operation is in 1N mode after self refresh exit, N x ^{t}CK MRS command or sync pulse is not required during self refresh exit. The minimum exit delay to the first valid command is ^{t}XS, or ^{t}XS_ABORT.

The DRAM may be changed from 2N to 1N by entering self refresh mode, which will reset to 1N mode.
Changing from 2N to by any other means can result in loss of data and make operation of the DRAM uncertain.

When operating in 2N gear-down mode, the following MR settings apply:

- CAS latency (MR0[6:4,2]): Even number of clocks
- Write recovery and read to precharge (MR0[11:9]): Even number of clocks
- Additive latency (MR1[4:3]): CL - 2
- CAS WRITE latency (MR2 A[5:3]): Even number of clocks
- CS to command/address latency mode (MR4[8:6]): Even number of clocks
- CA parity latency mode (MR5[2:0]): Even number of clocks

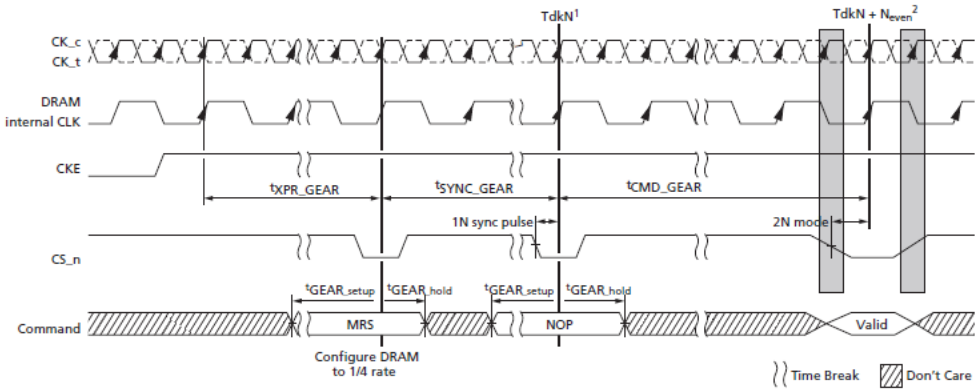
Figure 33. Clock Mode Change from 1/2 Rate to 1/4 Rate (Initialization)



Notes:

1. After ^{t}SYNC_GEAR from GEAR-DOWN command, internal clock rate is changed at TdkN.
2. After ^{t}SYNC_GEAR + ^{t}CMD_GEAR from GEAR-DOWN command, both internal clock rate and command cycle are changed at TdkN + Neven.

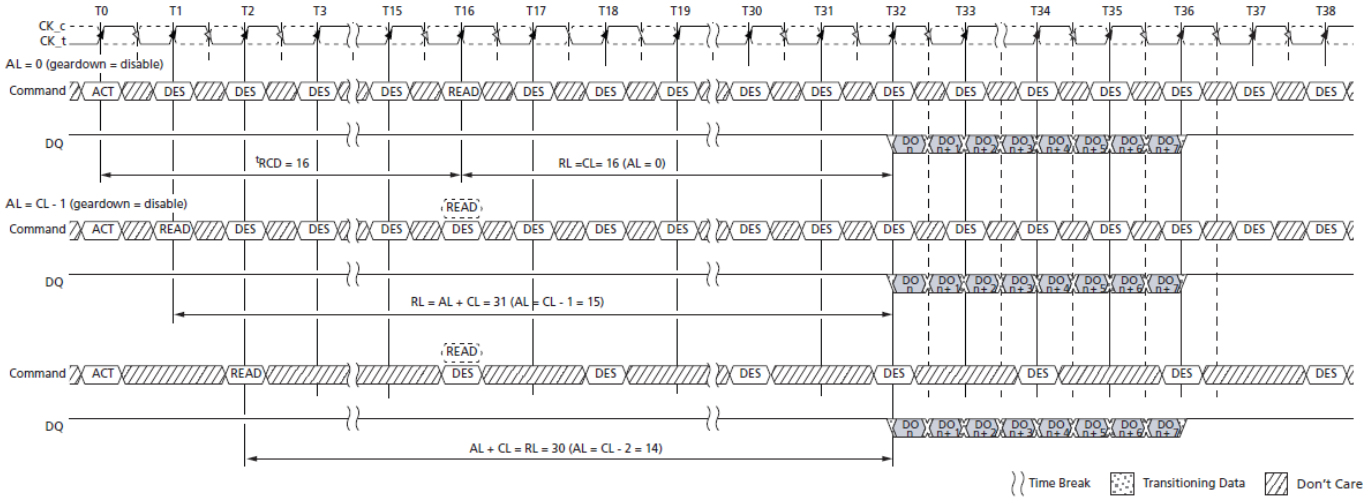
Figure 34. Clock Mode Change After Exiting Self Refresh



Notes:

1. After ^{t}SYNC_GEAR from GEAR-DOWN command, internal clock rate is changed at TdkN.
2. After ^{t}SYNC_GEAR + ^{t}CMD_GEAR from GEAR-DOWN command, both internal clock rate and command cycle are changed at TdkN + Neven.

Figure 35. Comparison Between Gear-Down Disable and Gear-Down Enable



Maximum Power-Saving Mode

Maximum power-saving mode provides the lowest power mode where data retention is not required.

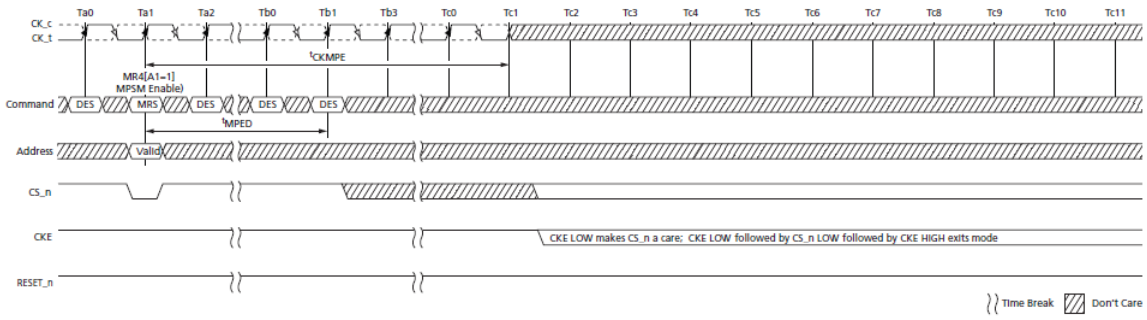
When the device is in the maximum power-saving mode, it does not maintain data retention or respond to any external command, except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal Low. This mode is more like a “hibernate mode” than a typical power-saving mode. The intent is to be able to park the DRAM at a very low-power state; the device can be switched to an active state via the per-DRAM addressability (PDA) mode.

Maximum Power-Saving Mode Entry

Maximum power-saving mode is entered through an MRS command. For devices with shared control/address signals, a single DRAM device can be entered into the maximum power-saving mode using the per-DRAM addressability MRS command. Large CS_n hold time to CKE upon the mode exit could cause DRAM malfunction; as a result, CA parity, CAL, and gear-down modes must be disabled prior to the maximum power-saving mode entry MRS command.

The MRS command may use both address and DQ information, as defined in the Per-DRAM Addressability section. As illustrated in the figure below, after tMPED from the mode entry MRS command, the DRAM is not responsive to any input signals except CKE, CS_n, and RESET_n. All other inputs are disabled (external input signals may become High-Z). The system will provide a valid clock until tCKMPE expires, at which time clock inputs (CK) should be disabled (external clock signals may become High-Z).

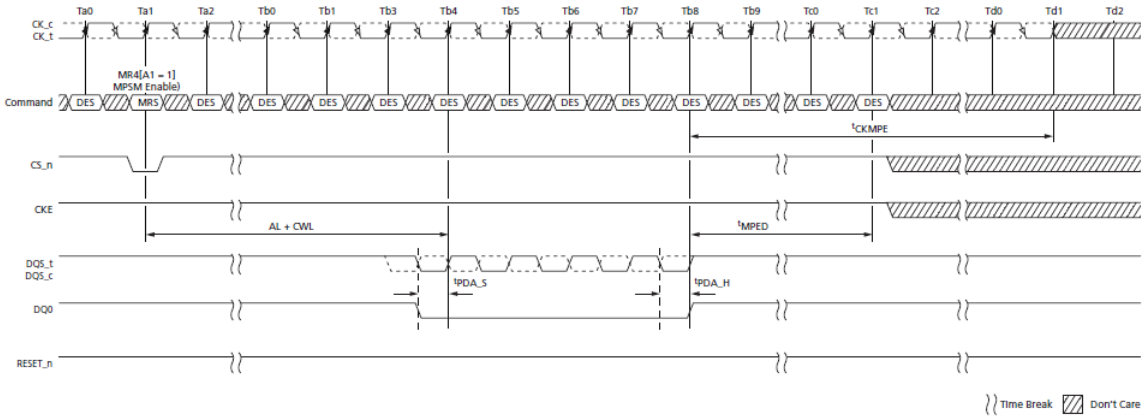
Figure 36. Maximum Power-Saving Mode Entry



Maximum Power-Saving Mode Entry in PDA

The sequence and timing required for the maximum power-saving mode with the per-DRAM addressability enabled is illustrated in the figure below.

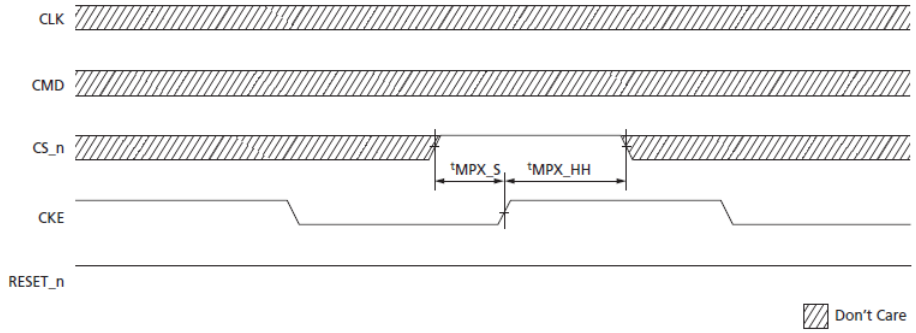
Figure 37. Maximum Power-Saving Mode Entry with PDA



CKE Transition During Maximum Power-Saving Mode

The following figure shows how to maintain maximum power-saving mode even though the CKE input may toggle. To prevent the device from exiting the mode, CS_n should be HIGH at the CKE LOW-to-HIGH edge, with appropriate setup (^{t}MPX_S) and hold (^{t}MPX_H) timings.

Figure 38. **Maintaining Maximum Power-Saving Mode with CKE Transition**

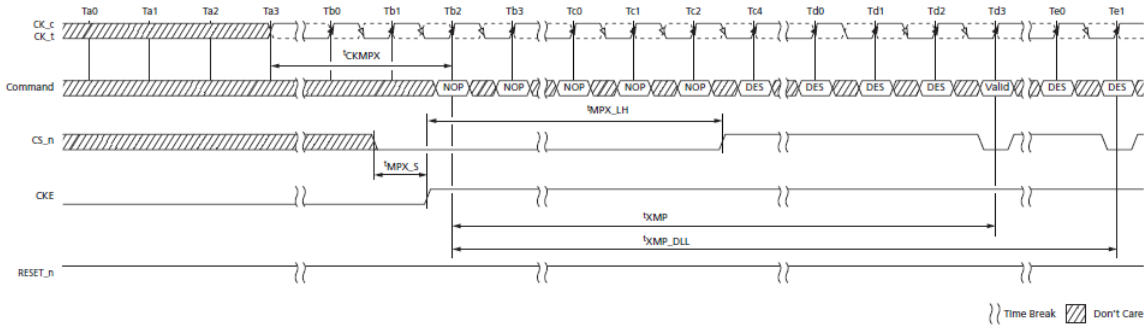


Maximum Power-Saving Mode Exit

To exit the maximum power-saving mode, CS_n should be LOW at the CKE LOW-to-HIGH transition, with appropriate setup (^{t}MPX_S) and hold (^{t}MPX_LH) timings, as shown in the figure below. Because the clock receivers (CK_t, CK_c) are disabled during this mode, CS_n = LOW is captured by the rising edge of the CKE signal. If the CS_n signal level is detected LOW, the DRAM clears the maximum power-saving mode MRS bit and begins the exit procedure from this mode. The external clock must be restarted and be stable by ^{t}CKMPX before the device can exit the maximum power-saving mode.

During the exit time (^{t}XMP), only NOP and DES commands are allowed: NOP during ^{t}MPX_LH and DES the remainder of ^{t}XMP. After ^{t}XMP expires, valid commands not requiring a locked DLL are allowed; after ^{t}XMP_DLL expires, valid commands requiring a locked DLL are allowed.

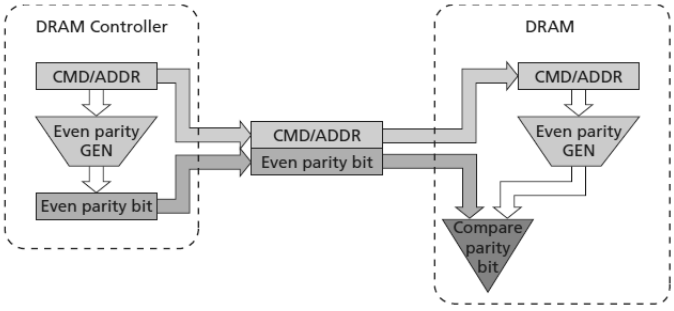
Figure 39. Maximum Power-Saving Mode Exit



Command / Address Parity

Command/address (CA) parity takes the CA parity signal (PAR) input carrying the parity bit for the generated address and commands signals and matches it to the internally generated parity from the captured address and commands signals. CA parity is supported in the DLL enabled state only; if the DLL is disabled, CA parity is not supported.

Figure 40. Command / Address Parity Operation



CA parity is disabled or enabled via an MRS command. If CA parity is enabled by programming a non-zero value to CA parity latency in the MR, the DRAM will ensure that there is no parity error before executing commands. There is an additional delay required for executing the commands versus when parity is disabled. The delay is programmed in the MR when CA parity is enabled (parity latency) and applied to all commands which are registered by CS_n (rising edge of CK_t and falling CS_n). The command is held for the time of the parity latency (PL) before it is executed inside the device. The command captured by the input clock has an internal delay before executing and is determined with PL. ALERT_n will go active when the DRAM detects a CA parity error.

CA parity covers ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, the address bus including bank address and bank group bits, and C[2:0] on 3DS devices; the control signals CKE, ODT, and CS_n are not covered. For example, for a 4Gb x4 monolithic device, parity is computed across BG[1:0], BA[1:0], A16/RAS_n, A15/CAS_n, A14/ WE_n, A[13:0], and ACT_n. The DRAM treats any unused address pins internally as zeros; for example, if a common die has stacked pins but the device is used in a monolithic application, then the address pins used for stacking and not connected are treated internally as zeros.

The convention for parity is even parity; for example, valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words, the parity bit is chosen so that the total number of ones in the transmitted signal, including the parity bit, is even.

If a DRAM device detects a CA parity error in any command qualified by CS_n, it will perform the following steps:

1. Ignore the erroneous command. Commands in the MAX N*n*CK window (^{t}PAR_UNKNOWN) prior to the erroneous command are not guaranteed to be executed. When a READ command in this N*n*CK window is not executed, the device does not activate DQS outputs. If WRITE CRC is enabled and a WRITE CRC occurs during the ^{t}PAR_UNKNOWN window, the WRITE CRC Error Status Bit located at MR5[3] may or may not get set. When CA Parity and WRITE CRC are both enabled and a CA Parity occurs, the WRITE CRC Error Status Bit should be reset.
2. Log the error by storing the erroneous command and address bits in the MPR error log.
3. Set the parity error status bit in the mode register to 1. The parity error status bit must be set before the ALERT_n signal is released by the DRAM (that is, ^{t}PAR_ALERT_ON + ^{t}PAR_ALERT_PW (MIN)).
4. Assert the ALERT_n signal to the host (ALERT_n is active LOW) within ^{t}PAR_ALERT_ON time.
5. Wait for all in-progress commands to complete. These commands were received ^{t}PAR_UNKOWN before the erroneous command.
6. Wait for tRAS (MIN) before closing all the open pages. The DRAM is not executing any commands uring the window defined by (^{t}PAR_ALERT_ON + ^{t}PAR_ALERT_PW).
7. After ^{t}PAR_ALERT_PW (MIN) has been satisfied, the device may de-assert ALERT_n.
   a) When the device is returned to a known precharged state, ALERT_n is allowed to be de-asserted.
8. After (^{t}PAR_ALERT_PW (MAX)) the DRAM is ready to accept commands for normal operation. Parity latency will be in effect; however, parity checking will not resume until the memory controller has cleared the parity error status bit by writing a zero. The DRAM will execute any erroneous commands until the bit is cleared; unless persistent mode is enabled.

- It is possible that the device might have ignored a REFRESH command during tPAR_ALERT_PW or the REFRESH command is the first erroneous frame, so it is recommended that extra REFRESH cycles be issued, as needed.
- The parity error status bit may be read anytime after tPAR_ALERT_ON + tPAR_ALERT_PW to determine which DRAM had the error. The device maintains the error log for the first erroneous command until the parity error status bit is reset to a zero or a second CA parity occurs prior to resetting.

The mode register for the CA parity error is defined as follows: CA parity latency bits are write only, the parity error status bit is read/write, and error logs are read-only bits. The DRAM controller can only program the parity error status bit to zero. If the DRAM controller illegally attempts to write a 1 to the parity error status bit, the DRAM can not be certain that parity will be checked; the DRAM may opt to block the DRAM controller from writing a 1 to the parity error status bit.

The device supports persistent parity error mode. This mode is enabled by setting MR5[9] = 1; when enabled, CA parity resumes checking after the ALERT_n is de-asserted, even if the parity error status bit remains a 1. If multiple errors occur before the error status bit is cleared the error log in MPR Page 1 should be treated as ”Don’t Care.” In persistent parity error mode the ALERT_n pulse will be asserted and de-asserted by the DRAM as defined with the MIN and MAX value ^{t}PAR_ALERT_PW. The DRAM controller must issue DESELECT commands once it detects the ALERT_n signal, this response time is defined as ^{t}PAR_ALERT_RSP. The following figures capture the flow of events on the CA bus and the ALERT_n signal.

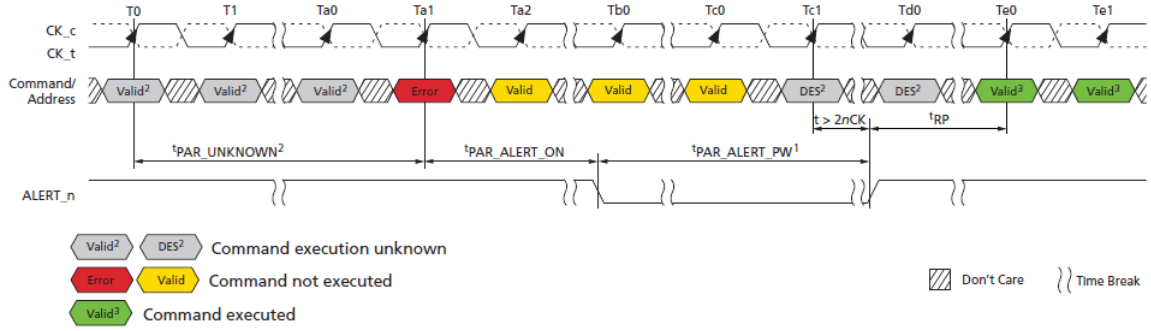
Table 33. Mode Register Setting for CA Parity

CA Parity Latency MR5[2:0] *1	Applicable Speed Bin	Parity Error Status	Parity Persistent Mode	Erroneous CA Frame
000 = Disabled	N/A	MR5 [4] 0 = Clear MR5 [4] 1 = Error	MR5 [9] 0 = Disabled- MR5 [9] 1 = Enabled	C[2:0], ACT_n, BG1, BG0, BA[1:0], PAR, A17, A16/RAS_n, A15/CAS_n, A14/WE_n, A[13:0]
001 = 4 clocks	1600, 1866, 2133			
010 = 5 clocks	2400, 2666			
011 = 6 clocks	2933, 3200			
100 = 8 clocks	RFU			
101 = Reserved	RFU			
110 = Reserved	RFU			
111 = Reserved	RFU			
000 = Disabled	N/A			

Notes:

1. Parity latency is applied to all commands.
2. Parity latency can be changed only from a CA parity disabled state; for example, a direct change from PL = 3 to PL = 4 is not allowed. The correct sequence is PL = 3 to disabled to PL = 4.
3. Parity latency is applied to WRITE and READ latency. WRITE latency = AL + CWL + PL. READ latency = AL + CL + PL.

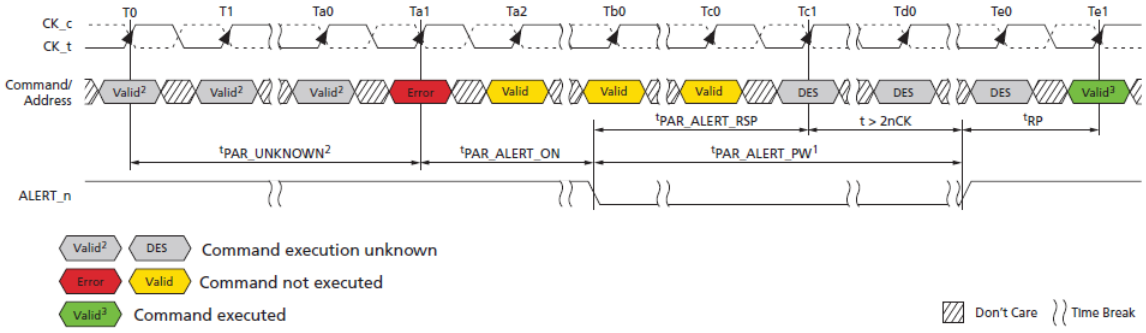
Figure 41. Command / Address Parity During Normal Operation



Notes:

1. DRAM is emptying queues. Precharge all and parity checking are off until parity error status bit is cleared.
2. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
   If WRITE CRC is enabled and a WRITE CRC occurs during the ^{t}PAR_UNKNOWN window, the WRITE CRC Error Status Bit located at MR5[3] may or may not get set.
3. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking is off until parity error status bit is cleared.

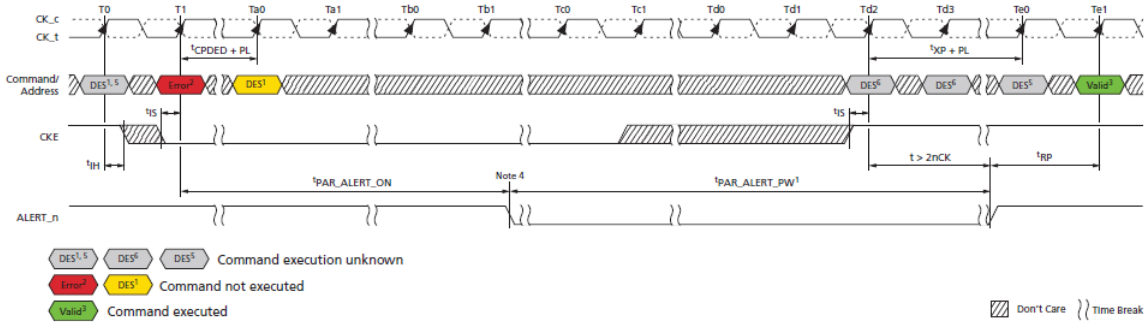
Figure 42. Persistent CA Parity Error Checking Operation



Notes:

1. DRAM is emptying queues. Precharge all and parity check re-enable finished by ^{t}PAR_ALERT_PW.
2. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
   If WRITE CRC is enabled and a WRITE CRC occurs during the ^{t}PAR_UNKNOWN window, the WRITE CRC Error Status Bit located at MR5[3] may or may not get set
3. Normal operation with parity latency and parity checking (CA parity persistent error mode enabled).

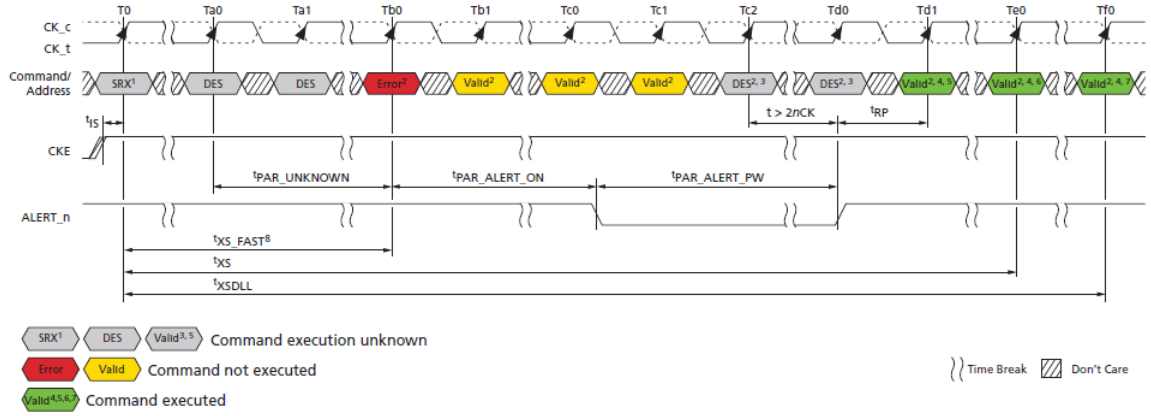
Figure 43. CA Parity Error Checking – SRE Attempt



Notes:

1. Only DESELECT command is allowed.
2. SELF REFRESH command error. The DRAM masks the intended SRE command and enters precharge power-down.
3. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking is off until the parity error status bit cleared.
4. The controller cannot disable the clock until it has been capable of detecting a possible CA parity error.
5. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
6. Only a DESELECT command is allowed; CKE may go HIGH prior to Tc2 as long as DES commands are issued.

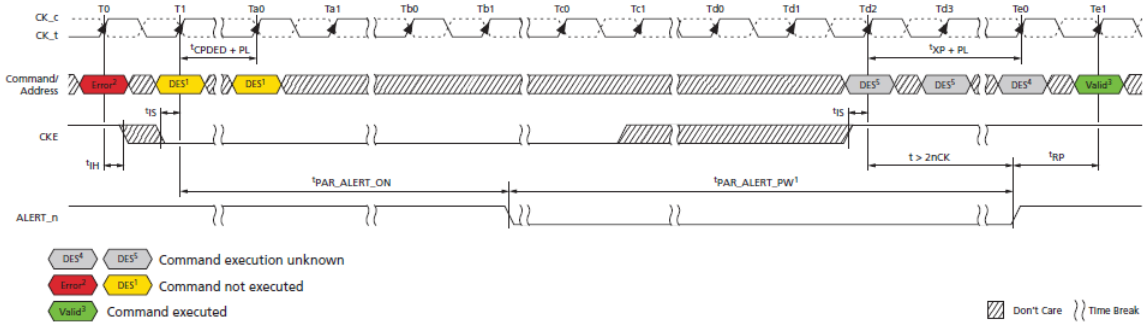
Figure 44. CA Parity Error Checking – SRX Attempt



Notes:

1. Self refresh abort = disable: MR4 [9] = 0.
2. Input commands are bounded by tXSDLL, tXS, tXS_ABORT, and tXS_FAST timing.
3. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
4. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking off until parity error status bit cleared.
5. Only an MRS (limited to those described in the SELF REFRESH Operation section), ZQCS, or ZQCL command is allowed.
6. Valid commands not requiring a locked DLL.
7. Valid commands requiring a locked DLL.
8. This figure shows the case from which the error occurred after tXS_FAST. An error may also occur after tXS_ABORT and tXS.

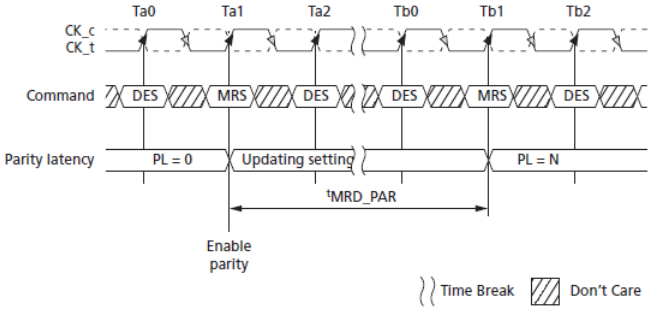
Figure 45. CA Parity Error Checking – PDE / PDX



Notes:

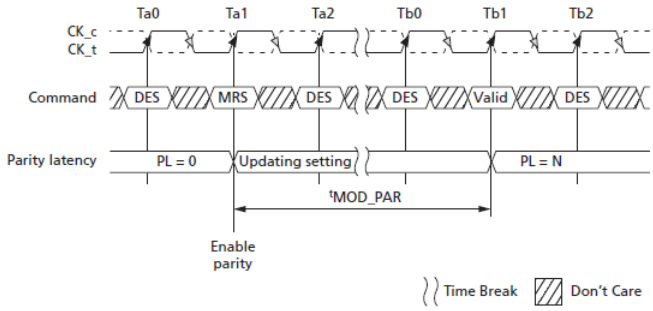
1. Only DESELECT command is allowed.
2. Error could be precharge or activate.
3. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking is off until parity error status bit cleared.
4. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
5. Only a DESELECT command is allowed; CKE may go HIGH prior to Td2 as long as DES commands are issued.

Figure 46. Parity Entry Timing Example - ^{t}MRD_PAR



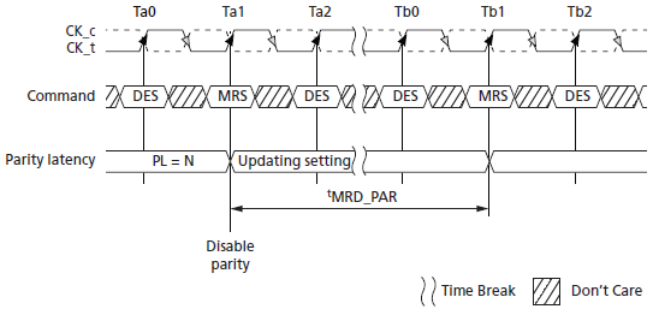
Note: 1. ^{t}MRD_PAR = ^{t}MOD + N; where N is the programmed parity latency.

Figure 47. Parity Entry Timing Example - ^{t}MOD_PAR



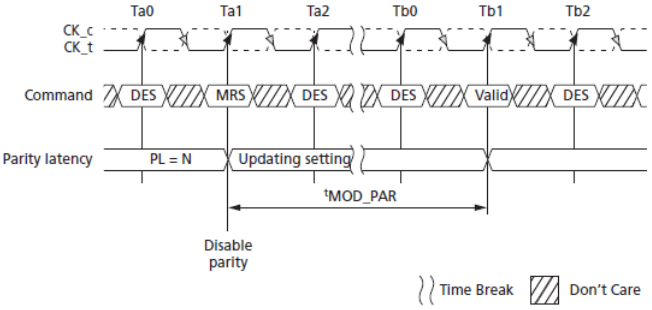
Note: 1. ^{t}MOD_PAR = ^{t}MOD + N; where N is the programmed parity latency.

Figure 48. Parity Exit Timing Example - ^{t}MRD_PAR



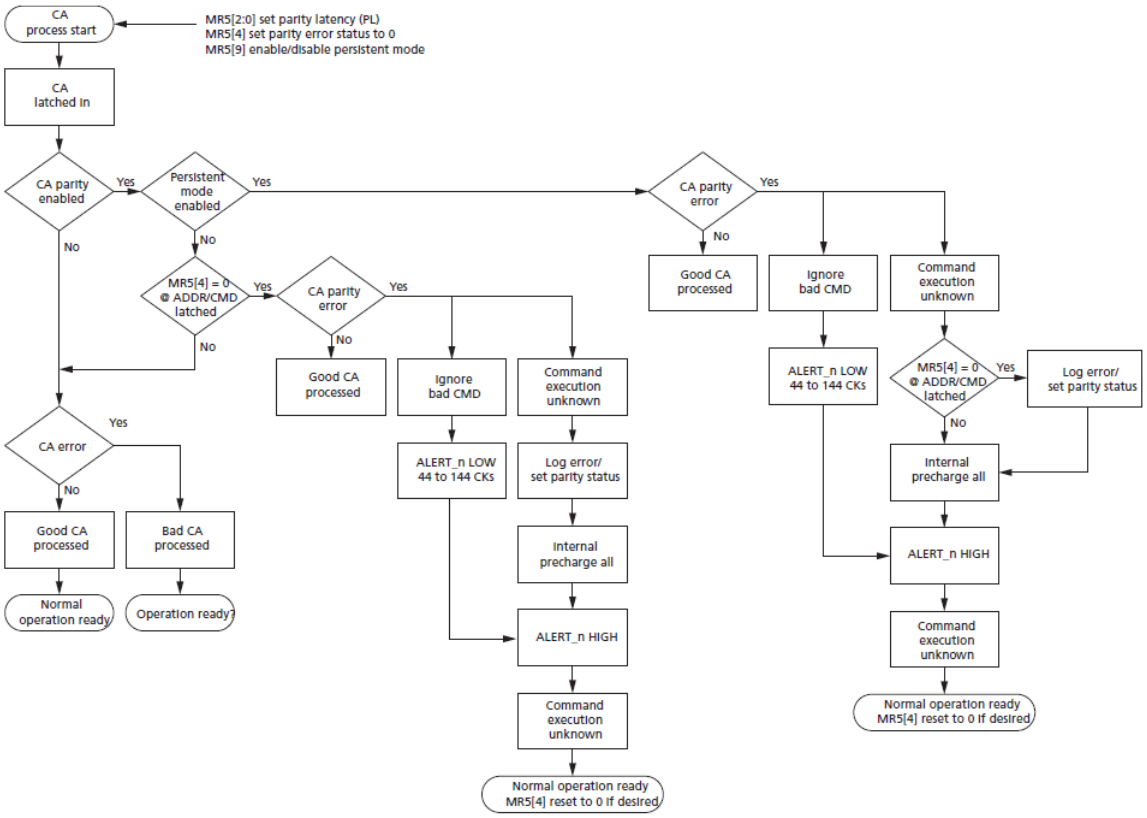
Note: 1. ^{t}MRD_PAR = ^{t}MOD + N; where N is the programmed parity latency.

Figure 49. Parity Exit Timing Example - ^{t}MOD_PAR



Note: 1. ^{t}MOD_PAR = ^{t}MOD + N; where N is the programmed parity latency.

Figure 50. CA Parity Flow Diagram



Per-DRAM Addressability

DDR4 allows programmability of a single, specific DRAM on a rank. As an example, this feature can be used to program different ODT or VREF values on each DRAM on a given rank. Because per-DRAM addressability (PDA) mode may be used to program optimal VREF for the DRAM, the data set up for first DQ0 transfer or the hold time for the last DQ0 transfer cannot be guaranteed. The DRAM may sample DQ0 on either the first falling or second rising DQS transfer edge. This supports a common implementation between BC4 and BL8 modes on the DRAM. The DRAM controller is required to drive DQ0 to a stable LOW or HIGH state during the length of the data transfer for BC4 and BL8 cases. Note, both fixed and on-the-fly (OTF) modes are supported for BC4 and BL8 during PDA mode.

1. Before entering PDA mode, write leveling is required.
   - BL8 or BC4 may be used.
2. Before entering PDA mode, the following MR settings are possible:
   - $R_{TT(Park)}$ MR5 A[8:6] = Enable
   - $R_{TT(NOM)}$ MR1 A[10:8] = Enable
3. Enable PDA mode using MR3 [4] = 1. (The default programed value of MR3[4] = 0.)
4. In PDA mode, all MRS commands are qualified with DQ0. The device captures DQ0 by using DQS signals. If the value on DQ0 is LOW, the DRAM executes the MRS command. If the value on DQ0 is HIGH, the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits.
5. Program the desired DRAM and mode registers using the MRS command and DQ0.
6. In PDA mode, only MRS commands are allowed.
7. The MODE REGISTER SET command cycle time in PDA mode, AL + CWL + BL/2 - 0.5^{t}CK + ^{t}MRD_PDA + PL, is required to complete the WRITE operation to the mode register and is the minimum time required between two MRS commands.
8. Remove the device from PDA mode by setting MR3[4] = 0. (This command requires DQ0 = 0.)

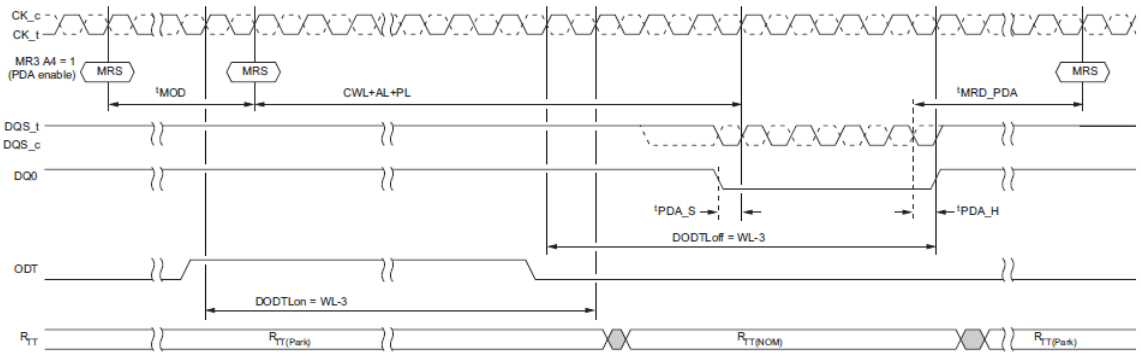
Note: Removing the device from PDA mode will require programming the entire MR3 when the MRS command is issued. This may impact some PDA values programmed within a rank as the EXIT command is sent to the rank. To avoid such a case, the PDA enable/disable control bit is located in a mode register that does not have any PDA mode controls.

In PDA mode, the device captures DQ0 using DQS signals the same as in a normal WRITE operation; however, dynamic ODT is not supported. Extra care is required for the ODT setting. If $R_{TT(NOM)}$ MR1 [10:8] = enable, device data termination needs to be controlled by the ODT pin, and applies the same timing parameters (defined below).

Table 34. Per-DRAM Addressability

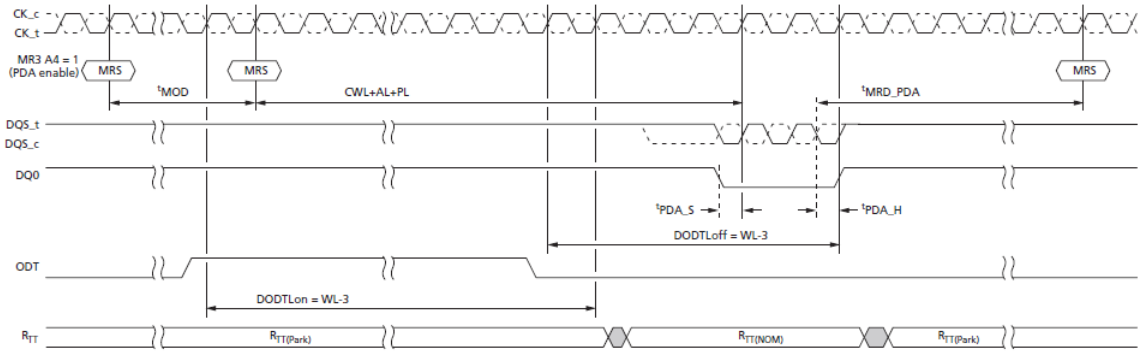
Symbol	Parameter
DODTLon	Direct ODT turnon latency
DODTLoff	Direct ODT turn off latency
^{t}ADC	R_{TT} change timing skew
^{t}AONAS	Asynchronous $R_{TT(NOM)}$ turn-on delay
^{t}AOFAS	Asynchronous $R_{TT(NOM)}$ turn-off delay

Figure 51. PDA Operation Enabled, BL8



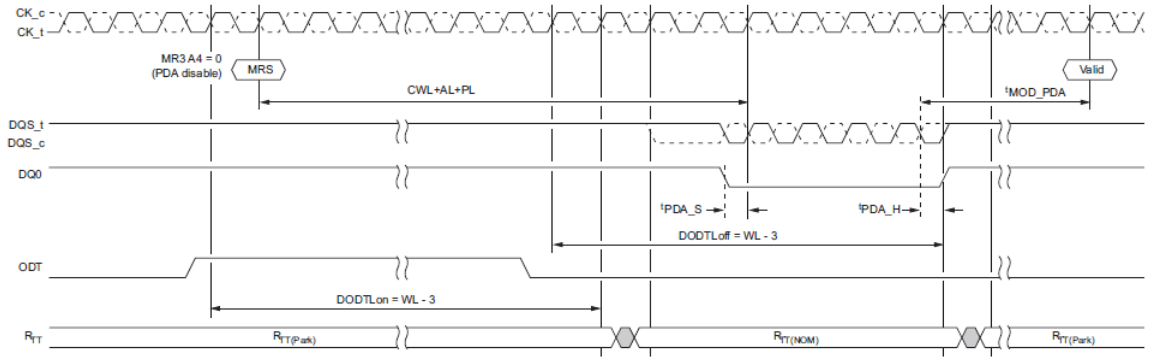
Note: 1. $R_{TT(Park)}$ = Enable; $R_{TT(NOM)}$ = Enable; WRITE preamble set = 2^{t}CK; and DLL = On.

Figure 52. PDA Operation Enabled, BC4



Note: 1. $R_{TT(Park)}$ = Enable; $R_{TT(NOM)}$ = Enable; WRITE preamble set = 2^{t}CK; and DLL = On.

Figure 53. MRS PDA Exit



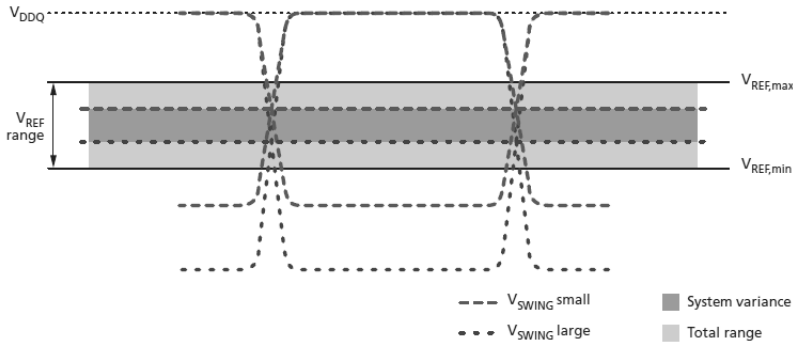
Note: 1. $R_{TT(Park)}$ = Enable; $R_{TT(NOM)}$ = Enable; WRITE preamble set = 2^{t}CK; and DLL = On.

V_{REFDQ} Calibration

The V_{REFDQ} level, which is used by the DRAM DQ input receivers, is internally generated. The DRAM VREFDQ does not have a default value upon power-up and must be set to the desired value, usually via V_{REFDQ} calibration mode. If PDA or PPR modes (hPPR or sPPR) are used prior to V_{REFDQ} calibration, V_{REFDQ} should initially be set at the midpoint between the $V_{DD,max}$, and the LOW as determined by the driver and ODT termination selected with wide voltage swing on the input levels and setup and hold times of approximately 0.75UI. The memory controller is responsible for V_{REFDQ} calibration to determine the best internal V_{REFDQ} level. The V_{REFDQ} calibration is enabled/disabled via MR6[7], MR6[6] selects Range 1 (60% to 92.5% of VDDQ) or Range 2 (45% to 77.5% of V_{DDQ}), and an MRS protocol using MR6[5:0] to adjust the V_{REFDQ} level up and down. MR6[6:0] bits can be altered using the MRS command if MR6[7] is enabled. The DRAM controller will likely use a series of writes and reads in conjunction with V_{REFDQ} adjustments to obtain the best V_{REFDQ}, which in turn optimizes the data eye.

The internal V_{REFDQ} specification parameters are voltage range, step size, V_{REF} step time, V_{REF} full step time, and V_{REF} valid level. The voltage operating range specifies the minimum required V_{REF} setting range for DDR4 SDRAM devices. The minimum range is defined by $V_{REFDQ,min}$ and $V_{REFDQ,max}$. As noted, a calibration sequence, determined by the DRAM controller, should be performed to adjust V_{REFDQ} and optimize the timing and voltage margin of the DRAM data input receivers. The internal V_{REFDQ} voltage value may not be exactly within the voltage range setting coupled with the V_{REF} set tolerance; the device must be calibrated to the correct internal V_{REFDQ} voltage.

Figure 54. V_{REFDQ} Voltage Range



V_{REFDQ} Range and Levels

Table 35. V_{REFDQ} Range and Levels

MR6[5:0]	Range 1 MR6[6] 0	Range 2 MR6[6] 1	MR6[5:0]	Range 1 MR6[6] 0	Range 2 MR6[6] 1
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111 = Reserved		

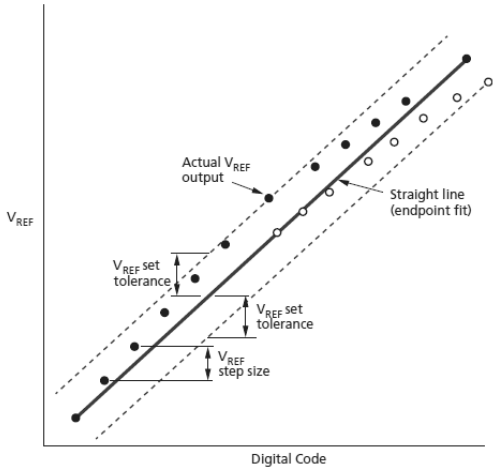
V_{REFDQ} Step Size

The V_{REF} step size is defined as the step size between adjacent steps. V_{REF} step size ranges from 0.5% V_{DDQ} to 0.8% V_{DDQ}. However, for a given design, the device has one value for V_{REF} step size that falls within the range.

The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REF} set tolerance uncertainty. The range of V_{REF} set tolerance uncertainty is a function of number of steps *n*.

The V_{REF} set tolerance is measured with respect to the ideal line, which is based on the MIN and MAX V_{REF} value endpoints for a specified range. The internal V_{REFDQ} voltage value may not be exactly within the voltage range setting coupled with the V_{REF} set tolerance; the device must be calibrated to the correct internal V_{REFDQ} voltage.

Figure 55. Example of V_{REF} Set Tolerance and Step Size

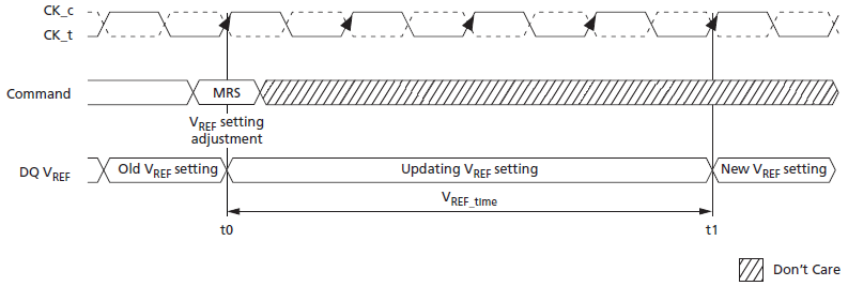


Note: 1. Maximum case shown.

V_{REFDQ} Increment and Decrement Timing

The V_{REF} increment/decrement step times are defined by $V_{REF,time}$. $V_{REF,time}$ is defined from t0 to t1, where t1 is referenced to the V_{REF} voltage at the final DC level within the V_{REF} valid tolerance (V_{REF,val_tol}). The V_{REF} valid level is defined by $V_{REF,val\ tolerance}$ to qualify the step time t1. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment.

Figure 56. V_{REFDO} Timing Diagram for $V_{REF.time}$ Parameter



Note:

1. t0 is referenced to the MRS command clock
   t1 is referenced to $V_{REF,tol}$

V_{REFDQ} calibration mode is entered via an MRS command, setting MR6[7] to 1 (0 disables V_{REFDQ} calibration mode) and setting MR6[6] to either 0 or 1 to select the desired range (MR6[5:0] are "Don't Care"). After V_{REFDQ} calibration mode has been entered, V_{REFDQ} calibration mode legal commands may be issued once $^{t}V_{REFDQE}$ has been satisfied. Legal commands for V_{REFDQ} calibration mode are ACT, WR, WRA, RD, RDA, PRE, DES, and MRS to set V_{REFDQ} values, and MRS to exit V_{REFDQ} calibration mode. Also, after V_{REFDQ} calibration mode has been entered, "dummy" WRITE commands are allowed prior to adjusting the V_{REFDQ} value the first time V_{REFDQ} calibration is performed after initialization.

Setting V_{REFDQ} values requires MR6[7] be set to 1 and MR6[6] be unchanged from the initial range selection; MR6[5:0] may be set to the desired V_{REFDQ} values. If MR6[7] is set to 0, MR6[6:0] are not written. $V_{REF,time\text{-}short}$ or $V_{REF,time\text{-}long}$ must be satisfied after each MR6 command to set V_{REFDQ} value before the internal V_{REFDQ} value is valid.

If PDA mode is used in conjunction with V_{REFDQ} calibration, the PDA mode requirement that only MRS commands are allowed while PDA mode is enabled is not waived. That is, the only V_{REFDQ} calibration mode legal commands noted above that may be used are the MRS commands: MRS to set V_{REFDQ} values and MRS to exit V_{REFDQ} calibration mode.

The last MR6[6:0] setting written to MR6 prior to exiting V_{REFDQ} calibration mode is the range and value used for the internal V_{REFDQ} setting. V_{REFDQ} calibration mode may be exited when the DRAM is in idle state. After the MRS command to exit V_{REFDQ} calibration mode has been issued, DES must be issued until $^{t}V_{REFDQX}$ has been satisfied where any legal command may then be issued. V_{REFDQ} setting should be updated if the die temperature changes too much from the calibration temperature.

The following are typical script when applying the above rules for V_{REFDQ} calibration routine when performing V_{REFDQ} calibration in Range 1:

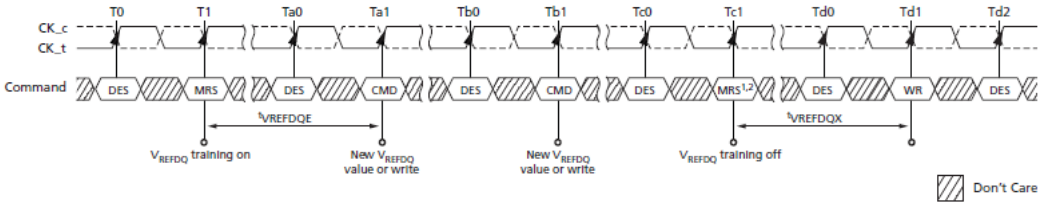
- MR6[7:6]10 [5:0]XXXXXXX.
  - Subsequent legal commands while in VREFDQ calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set V_{REFDQ} values and exit V_{REFDQ} calibration mode).
- All subsequent V_{REFDQ} calibration MR setting commands are MR6[7:6]10 [5:0]VVVVVV.
  - "VVVVVV" are desired settings for V_{REFDQ}.
- Issue ACT/WR/RD looking for pass/fail to determine V_{CENT} (midpoint) as needed.
- To exit V_{REFDQ} calibration, the last two V_{REFDQ} calibration MR commands are:
  - MR6[7:6]10 [5:0]VVVVVV* where VVVVVV* = desired value for V_{REFDQ}.
  - MR6[7]0 [6:0]XXXXXXX to exit V_{REFDQ} calibration mode.

The following are typical script when applying the above rules for V_{REFDQ} calibration routine when performing V_{REFDQ} calibration in Range 2:

- MR6[7:6]11 [5:0]XXXXXXX.
  - Subsequent legal commands while in V_{REFDQ} calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set V_{REFDQ} values and exit V_{REFDQ} calibration mode).
- All subsequent V_{REFDQ} calibration MR setting commands are MR6[7:6]11 [5:0]VVVVVV.
  - "VVVVVV" are desired settings for V_{REFDQ}.
- Issue ACT/WR/RD looking for pass/fail to determine V_{CENT} (midpoint) as needed.
- To exit V_{REFDQ} calibration, the last two V_{REFDQ} calibration MR commands are:
  - MR6[7:6]11 [5:0]VVVVVV* where VVVVVV* = desired value for V_{REFDQ}.
  - MR6[7]0 [6:0]XXXXXXX to exit V_{REFDQ} calibration mode.

Note: Range may only be set or changed when entering V_{REFDQ} calibration mode; changing range while in or exiting V_{REFDQ} calibration mode is illegal.

Figure 57. V_{REFDQ} Training Mode Entry and Exit Timing Diagram



Note:

1. New V_{REFDQ} values are not allowed with an MRS command during calibration mode entry.
2. Depending on the step size of the latest programmed V_{REF} value, V_{REF} must be satisfied before disabling V_{REFDQ} training mode.

Figure 58. V_{REF} Step: Single Step Size Increment Case

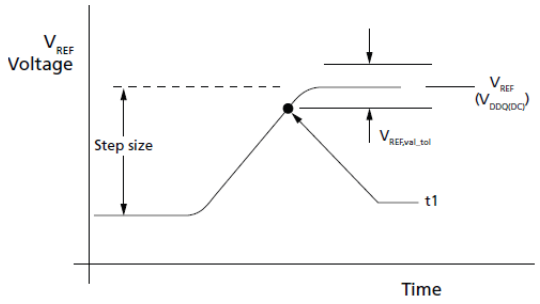


Figure 59. V_{REF} Step: Single Step Size Decrement Case

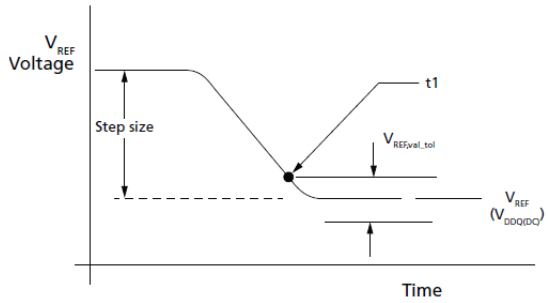


Figure 60. V_{REF} Full Step: From $V_{REF,min}$ to $V_{REF,max}$ Case

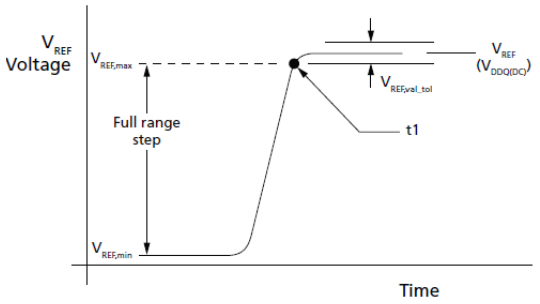
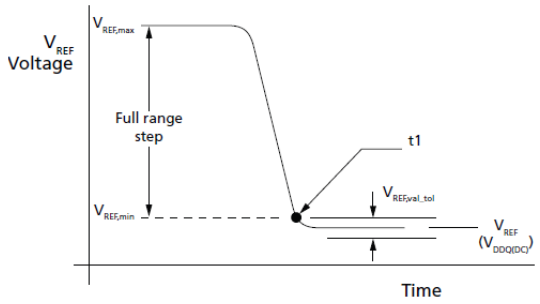


Figure 61. V_{REF} Full Step: From $V_{REF,max}$ to $V_{REF,min}$ Case



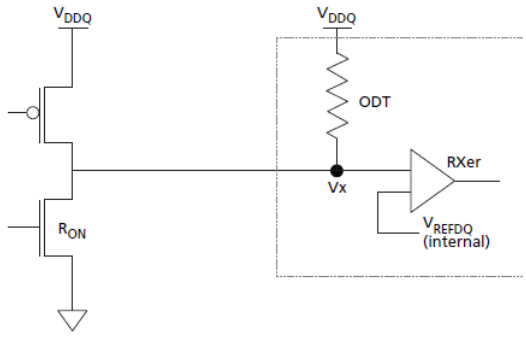
V_{REFDQ} Target Settings

The V_{REFDQ} initial settings are largely dependant on the ODT termination settings. The table below shows all of the possible initial settings available for V_{REFDQ} training; it is unlikely the lower ODT settings would be used in most cases.

Table 36. V_{REFDQ} Settings (V_{DDQ} = 1.2V)

R_{ON}	ODT	V_x - V_{IN} LOW (mV)	V_{REFDQ} (mv)	V_{REFDQ} (%V_{DDQ})
34 ohm	34 ohm	600	900	75%
	40 ohm	550	875	73%
	48 ohm	500	850	71%
	60 ohm	435	815	68%
	80 ohm	360	780	65%
	120 ohm	265	732	61%
	240 ohm	150	675	56%
48 ohm	34 ohm	700	950	79%
	40 ohm	655	925	77%
	48 ohm	600	900	75%
	60 ohm	535	865	72%
	80 ohm	450	825	69%
	120 ohm	345	770	64%
	240 ohm	200	700	58%

Figure 62. V_{REFDQ} Equivalent Circuit



Connectivity Test Mode

Connectivity test (CT) mode is similar to boundary scan testing but is designed to significantly speed up the testing of electrical continuity of pin interconnections between the device and the memory controller on the PC boards. Designed to work seamlessly with any boundary scan device, CT mode is supported in all x4, x8, and x16 non-3DS devices (JEDEC states CT mode for x4 and x8 is not required on 4Gb and is an optional feature on 8Gb and above). 3DS devices do not support CT mode and the TEN pin should be considered RFU maintained LOW at all times.

Contrary to other conventional shift-register-based test modes, where test patterns are shifted in and out of the memory devices serially during each clock, the CT mode allows test patterns to be entered on the test input pins in parallel and the test results to be extracted from the test output pins of the device in parallel. These two functions are also performed at the same time, significantly increasing the speed of the connectivity check. When placed in CT mode, the device appears as an asynchronous device to the external controlling agent. After the input test pattern is applied, the connectivity test results are available for extraction in parallel at the test output pins after a fixed propagation delay time.

Note: A reset of the device is required after exiting CT mode (see RESET and Initialization Procedure).

Pin Mapping

Only digital pins can be tested using the CT mode. For the purposes of a connectivity check, all the pins used for digital logic in the device are classified as one of the following types:

- **Test enable (TEN):** When asserted HIGH, this pin causes the device to enter CT mode. In CT mode, the normal memory function inside the device is bypassed and the I/O pins appear as a set of test input and output pins to the external controlling agent. Additionally, the device will set the internal V_{REFDQ} to V_{DDQ} x 0.5 during CT mode (this is the only time the DRAM takes direct control over setting the internal V_{REFDQ}). The TEN pin is dedicated to the connectivity check function and will not be used during normal device operation.
- **Chip select (CS_n):** When asserted LOW, this pin enables the test output pins in the device. When de-asserted, these output pins will be High-Z. The CS_n pin in the device serves as the CS_n pin in CT mode.
- **Test input:** A group of pins used during normal device operation designated as test input pins. These pins are used to enter the test pattern in CT mode.
- **Test output:** A group of pins used during normal device operation designated as test output pins.
- These pins are used for extraction of the connectivity test results in CT mode.
- **RESET_n:** This pin must be fixed high level during CT mode, as in normal function.

Table 37. Connectivity Mode Pin Description and Switching Levels

CT Mode Pins		Pin Names during Normal Memory Operation	Switching Level	Notes
Test Enable		TEN	CMOS (20%/80% V_{DD})	1,2
Chip Select		CS_n	V_{REFCA} ± 200mV	3
Test Input	A	BA[1:0], BG[1:0], A[9:0], A10/AP, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, A17, CKE, ACT_n, ODT, CK_t, CK_c, PAR	V_{REFCA} ± 200mV	3
	B	DML_n/DBIL_n, DMU_n/DBIU_n, DM_n/DBI_n	V_{REFDQ} ± 200mV	4
	C	ALERT_n	CMOS (20%/80% V_{DD})	2,5
	D	RESET_n	CMOS (20%/80% V_{DD})	2
Test Output		DQ[15:0], DQSU_t, DQSU_c, DQSL_t, DQSL_c, DQS_t, DQS_c	V_{TT} ± 100mV	6

Note:

1. TEN: Connectivity test mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation.
2. CMOS is a rail-to-rail signal with DC HIGH at 80% and DC LOW at 20% of V_{DD} (960mV for DC HIGH and 240mV for DC LOW.)
3. V_{REFCA} should be $V_{DD}/2$.
4. V_{REFDQ} should be $V_{DDQ}/2$.
5. ALERT_n switching level is not a final setting.
6. V_{TT} should be set to $V_{DD}/2$.

Minimum Terms Definition for Logic Equations

The test input and output pins are related by the following equations, where INV denotes a logical inversion operation and XOR a logical exclusive OR operation:

MT0 = XOR (A1, A6, PAR)
MT1 = XOR (A8, ALERT_n, A9)
MT2 = XOR (A2, A5, A13) or XOR (A2, A5, A13, A17)
MT3 = XOR (A0, A7, A11)
MT4 = XOR (CK_c, ODT, CAS_n/A15)
MT5 = XOR (CKE, RAS_n/A16, A10/AP)
MT6 = XOR (ACT_n, A4, BA1)
MT7 = x16: XOR (DMU_n/DBIU_n, DML_n/DBIL_n, CK_t)
MT8 = XOR (WE_n/A14, A12 / BC, BA0)
MT9 = XOR (BG0, A3, RESET_n and TEN)

Logic Equations for a x16 Device

DQ0 = MT0	DQ10 = INV DQ2
DQ1 = MT1	DQ11 = INV DQ3
DQ2 = MT2	DQ12 = INV DQ4
DQ3 = MT3	DQ13 = INV DQ5
DQ4 = MT4	DQ14 = INV DQ6
DQ5 = MT5	DQ15 = INV DQ7
DQ6 = MT6	LDQS_t = MT8
DQ7 = MT7	LDQS_c = MT9
DQ8 = INV DQ0	UDQS_t = INV LDQS_t
DQ9 = INV DQ1	UDQS_c = INV LDQS_c

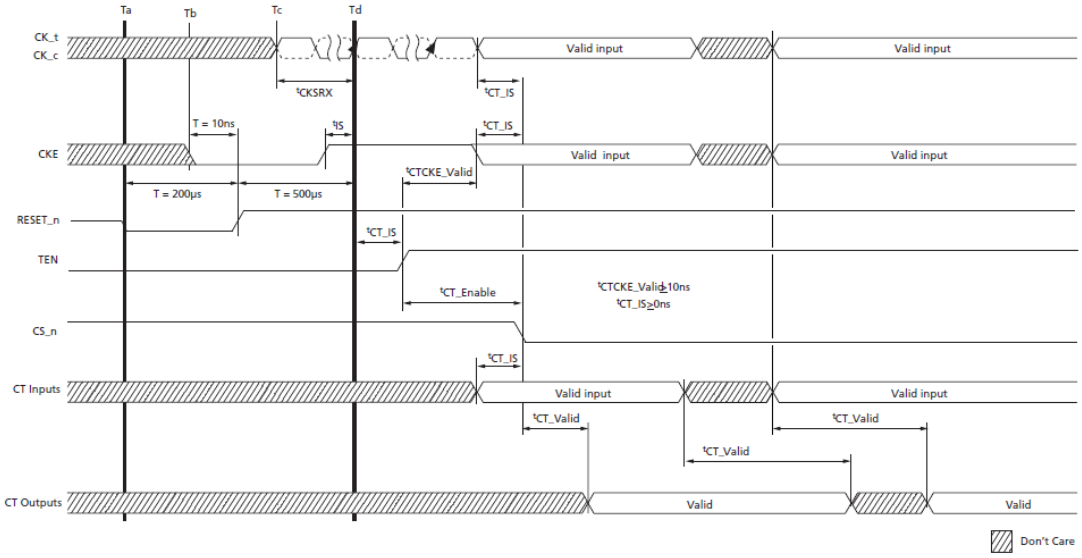
CT Input Timing Requirements

Prior to the assertion of the TEN pin, all voltage supplies, including VREFCA, must be valid and stable and RESET_n registered high prior to entering CT mode. Upon the assertion of the TEN pin HIGH with RESET_n, CKE, and CS_n held HIGH; CK_t, CK_c, and CKE signals become test inputs within ^{t}CTECT_Valid. The remaining CT inputs become valid tCT_Enable after TEN goes HIGH when CS_n allows input to begin sampling, provided inputs were valid for at least ^{t}CT_Valid. While in CT mode, refresh activities in the memory arrays are not allowed; they are initiated either externally (auto refresh) or internally (self refresh).

The TEN pin may be asserted after the DRAM has completed power-on. After the DRAM is initialized and V_{REFDQ} is calibrated, CT mode may no longer be used. The TEN pin may be de-asserted at any time in CT mode. Upon exiting CT mode, the states and the integrity of the original content of the memory array are unknown. A full reset of the memory device is required.

After CT mode has been entered, the output signals will be stable within ^{t}CT_Valid after the test inputs have been applied as long as TEN is maintained HIGH and CS_n is maintained LOW.

Figure 63. Connectivity Test Mode Entry



Excessive Row Activation

Rows can be accessed a limited number of times within a certain time period before adjacent rows require refresh. The maximum activate count (MAC) is the maximum number of activates that a single row can sustain within a time interval of equal to or less than the maximum activate window (^{t}MAW) before the adjacent rows need to be refreshed, regardless of how the activates are distributed over ^{t}MAW.

DDR4 devices automatically perform a type of TRR mode in the background and provide an MPR Page 3 MPR3[3:0] of 1000, indicating there is no restriction to the number of ACTIVATE commands to a given row in a refresh period provided DRAM timing specifications are not violated.

However, specific attempts to by-pass TRR may result in data disturb.

Table 38. MAC Encoding of MPR Page 3 MPR3

[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	MAC	Comments
x	x	x	x	0	0	0	0	Untested	The device has not been tested for MAC.
x	x	x	x	0	0	0	1	^{t}MAC = 700K	
x	x	x	x	0	0	1	0	^{t}MAC = 600K	
x	x	x	x	0	0	1	1	^{t}MAC = 500K	
x	x	x	x	0	1	0	0	^{t}MAC = 400K	
x	x	x	x	0	1	0	1	^{t}MAC = 300K	
x	x	x	x	0	1	1	0	Reserved	
x	x	x	x	0	1	1	1	^{t}MAC = 200K	
x	x	x	x	1	0	0	0	Unlimited	There is no restriction to the number of ACTIVATE commands to a given row in a refresh period provided DRAM timing specifications are not violated.
x	x	x	x	1	0	0	1	Reserved	
x	x	x	x	..	..	..	..	Reserved	
x	x	x	x	1	1	1	1	Reserved	

Notes: 1. MAC encoding in MPR Page 3 MPR3.

Post Package Repair

Post Package Repair

JEDEC defines two modes of Post Package Repair (PPR): soft Post Package Repair (sPPR) and hard Post Package Repair (hPPR). sPPR is non-persistent so the repair row maybe altered; that is, sPPR is NOT a permanent repair and even though it will repair a row, the repair can be reversed, reassigned via another sPPR, or made permanent via hPPR. Hard Post Package Repair is persistent so once the repair row is assigned for a hPPR address, further PPR commands to a previous hPPR section should not be performed, that is, hPPR is a permanent repair; once repaired, it cannot be reversed. The controller provides the failing row address in the hPPR/sPPR sequence to the device to perform the row repair.

hPPR Mode and sPPR Mode may not be enabled at the same time.

JEDEC states hPPR is optional for 4Gb and sPPR is optional for 4Gb and 8Gb parts however 4Gb and 8Gb DDR4 DRAMs should have both sPPR and hPPR support. The hPPR support is identified via an MPR read from MPR Page 2, MPR0[7] and sPPR support is identified via an MPR read from MPR Page 2, MPR0[6].

The JEDEC minimum support requirement for DDR4 PPR (hPPR or sPPR) is to provide one row of repair per bank group (BG), x4/x8 have 4 BG and x16 has 2 BG; this is a total of 4 repair rows available on x4/x8 and 2 repair rows available on x16. PPR support exceeds the JEDEC minimum requirements; DDR4 DRAMs have at least one row of repair for each bank which is essentially 4 row repairs per BG for a total of 16 repair rows for x4 and x8 and 8 repair rows for x16; a 4x increase in repair rows.

JEDEC requires the user to have all sPPR row repair addresses reset and cleared prior to enabling hPPR Mode. DDR4 PPR does not have this restriction, the existing sPPR row repair addresses are not required to be cleared prior to entering hPPR mode. Each bank in a BG is PPR independent: sPPR or hPPR issued to a bank will not alter a sPPR row repair existing in a different bank.

sPPR followed by sPPR to same bank

When PPR is issued to a bank for the first time and is a sPPR command, the repair row will be a sPPR.
When a subsequent sPPR is issued to the same bank, the previous sPPR repair row will be cleared and used for the subsequent sPPR address as the sPPR operation is non-persistent.

sPPR followed by hPPR to same bank

When a PPR is issued to a bank for the first time and is a sPPR command, the repair row will be a sPPR.
When a subsequent hPPR is issued to the same bank, the initial sPPR repair row will be cleared and used for the hPPR address1. If a further subsequent PPR (hPPR or sPPR) is issued to the same bank, the further subsequent PPR (hPPR or sPPR) repair row will not clear or overwrite the previous hPPR address as the hPPR operation is persistent.

hPPR followed by hPPR or sPPR to same bank

When a PPR is issued to a bank for the first time and is a hPPR command, the repair row will be a hPPR.
When a subsequent PPR (hPPR or sPPR) is issued to the same bank, the subsequent PPR (hPPR or sPPR) repair row will not clear or overwrite the initial hPPR address as the initial hPPR is persistent.

Note: Newer DDR4 designs may not guarantee that a sPPR followed by a hPPR to the same bank will result the same repair row being used. Contact factory for more information.

Hard Post Package Repair

All banks must be precharged and idle. DBI and CRC modes must be disabled. Both sPPR and hPPR must be disabled. sPPR is disabled with MR4[5] = 0. hPPR is disabled with MR4[13] = 0, which is the normal state, and hPPR is enabled with MR4 [13]= 1, which is the hPPR enabled state. There are two forms of hPPR mode. Both forms of hPPR have the same entry requirement as defined in the sections below. The first command sequence uses a WRA command and supports data retention with a REFRESH operation except for the bank containing the row that is being repaired; JEDEC has relaxed this requirement and allows BA[0] to be a Don't Care regarding the banks which are not required to maintain data a REFRESH operation during hPPR. The second command sequence uses a WR command (a REFRESH operation can't be performed in this command sequence). The second command sequence doesn't support data retention for the target DRAM.

hPPR Row Repair - Entry

As stated above, all banks must be precharged and idle. DBI and CRC modes must be disabled, and all timings must be followed as shown in the timing diagram that follows.
All other commands except those listed in the following sequences are illegal.

1. Issue MR4[13] 1 to enter hPPR mode enable.
   a) All DQ are driven HIGH.
2. Issue four consecutive guard key commands (shown in the table below) to MR0 with each command separated by tMOD. The PPR guard key settings are the same whether performing sPPR or hPPR mode.
   a) Any interruption of the key sequence by other commands, such as ACT, WR, RD, PRE, REF, ZQ and NOP, are not allowed.
   b) If the guard key bits are not entered in the required order or interrupted with other MR commands, hPPR will not be enabled, and the programming cycle will result in a NOP.
   c) When the hPPR entry sequence is interrupted and followed by ACT and WR commands, these commands will be conducted as normal DRAM commands.
   d) JEDEC allows A6:0 to be Don't Care on 4Gb and 8Gb devices from a supplier perspective and the user should rely on vendor datasheet.

Table 39. PPR MR0 Guard Key Settings

MR0	BG[1:0]	BA[1:0]	A17:12	A11	A10	A9	A8	A7	A6:0
First guard key	0	0	xxxxxx	1	1	0	0	1	1111111
Second guard key	0	0	xxxxxx	0	1	1	1	1	1111111
Third Guard key	0	0	xxxxxx	1	0	1	1	1	1111111
Fourth guard key	0	0	xxxxxx	0	0	1	1	1	1111111

hPPR Row Repair – WRA Initiated (REF Commands Allowed)

1. Issue an ACT command with failing BG and BA with the row address to be repaired.
2. Issue a WRA command with BG and BA of failing row address.
   a) The address must be at valid levels, but the address is Don't Care.
3. All DQ of the target DRAM should be driven LOW for 4*n*CK (bit 0 through bit 7) after WL (WL = CWL + AL + PL) in order for hPPR to initiate repair.
   a) Repair **will be** initiated to the target DRAM only if all DQ during bit 0 through bit 7 are LOW. The bank under repair does not get the REFRESH command applied to it.
   b) Repair **will not be** initiated to the target DRAM if any DQ during bit 0 through bit 7 is HIGH.
      i) JEDEC states: All DQs of target DRAM should be LOW for 4^{t}CK. If HIGH is driven to all DQs of a DRAM consecutively for equal to or longer than 2^{t}CK, then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4^{t}CK nor HIGH for equal to or longer than 2^{t}CK, then hPPR mode execution is unknown.
   c) DQS should function normally.
4. REF command may be issued anytime after the WRA command followed by WL + 4*n*CK + ^{t}WR + ^{t}RP.
   a) Multiple REF commands are issued at a rate of tREFI or ^{t}REFI/2, however back-to-back REF commands must be separated by at least ^{t}REFI/4 when the DRAM is in hPPR mode.
   b) All banks except the bank under repair will perform refresh.
5. Issue PRE after tPGM time so that the device can repair the target row during ^{t}PGM time.
   a) Wait ^{t}PGM_Exit after PRE to allow the device to recognize the repaired target row address.
6. Issue MR4[13] 0 command to hPPR mode disable.
   a) Wait ^{t}PGMPST for hPPR mode exit to complete.
   b) After ^{t}PGMPST has expired, any valid command may be issued.

The entire sequence from hPPR mode enable through hPPR mode disable may be repeated if more than one repair is to be done.

After completing hPPR mode, MR0 must be re-programmed to a prehPPR mode state if the device is to be accessed.

After hPPR mode has been exited, the DRAM controller can confirm if the target row was repaired correctly by writing data into the target row and reading it back.

Figure 64. hPPR WRA – Entry

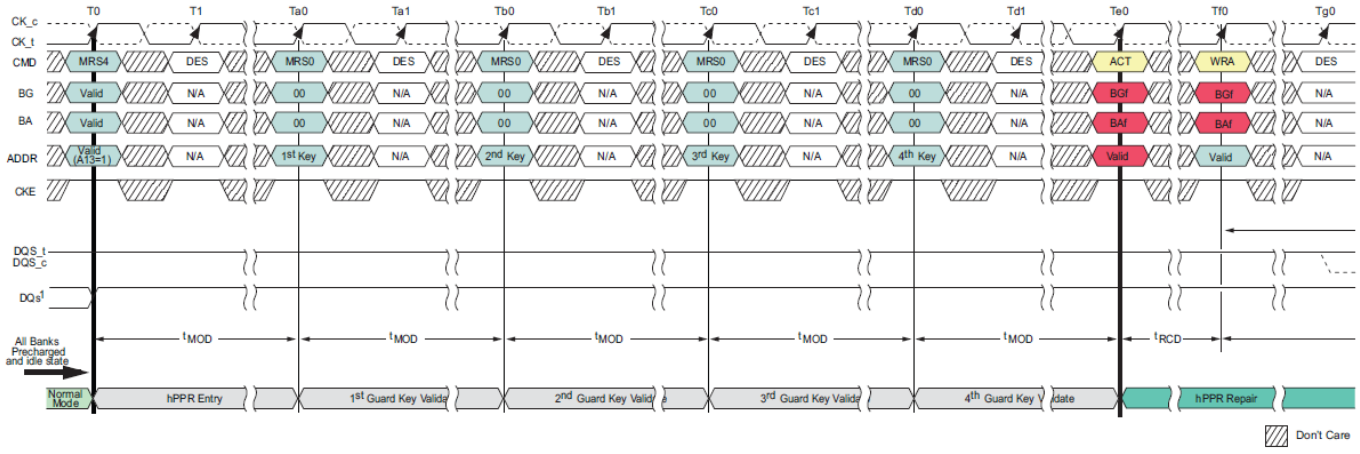
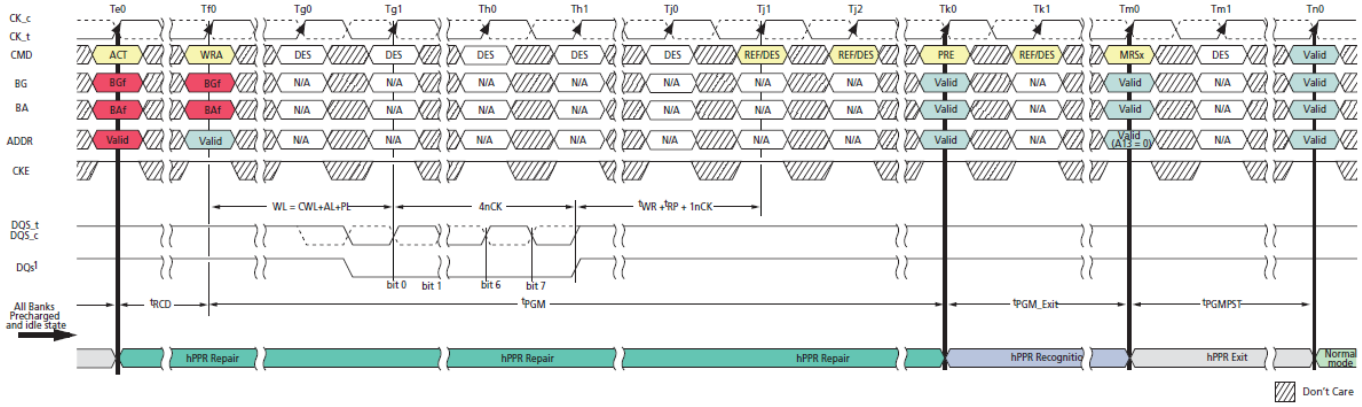


Figure 65. hPPR WRA – Repair and Exit



hPPR Row Repair – WR Initiated (REF Commands NOT Allowed)

1. Issue an ACT command with failing BG and BA with the row address to be repaired.
2. Issue a WR command with BG and BA of failing row address.
   a) The address must be at valid levels, but the address is Don't Care.
3. All DQ of the target DRAM should be driven LOW for 4*n*CK (bit 0 through bit 7) after WL (WL = CWL + AL + PL) in order for hPPR to initiate repair.
   a) Repair **will be** initiated to the target DRAM only if all DQ during bit 0 through bit 7 are LOW.
   b) Repair **will not be** initiated to the target DRAM if any DQ during bit 0 through bit 7 is HIGH.
      i) JEDEC states: All DQs of target DRAM should be LOW for 4^{t}CK. If HIGH is driven to all DQs of a DRAM consecutively for equal to or longer than 2^{t}CK, then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4^{t}CK nor HIGH for equal to or longer than 2^{t}CK, then hPPR mode execution is unknown.
   c) DQS should function normally.
4. REF commands may NOT be issued at anytime while in PPT mode.
5. Issue PRE after tPGM time so that the device can repair the target row during tPGM time.
   a) Wait ^{t}PGM_Exit after PRE to allow the device to recognize the repaired target row address.
6. Issue MR4[13] 0 command to hPPR mode disable.
   a) Wait ^{t}PGMPST for hPPR mode exit to complete.
   b) After ^{t}PGMPST has expired, any valid command may be issued.

The entire sequence from hPPR mode enable through hPPR mode disable may be repeated if more than one repair is to be done.

After completing hPPR mode, MR0 must be re-programmed to a prehPPR mode state if the device is to be accessed.

After hPPR mode has been exited, the DRAM controller can confirm if the target row was repaired correctly by writing data into the target row and reading it back.

Figure 66. hPPR WR – Entry

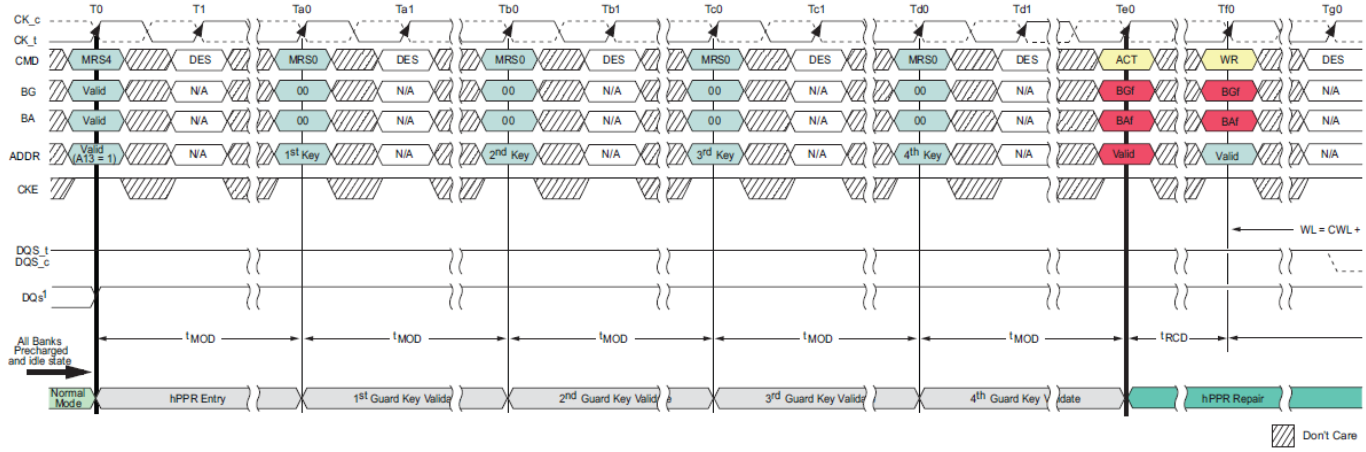


Figure 67. hPPR WR – Repair and Exit

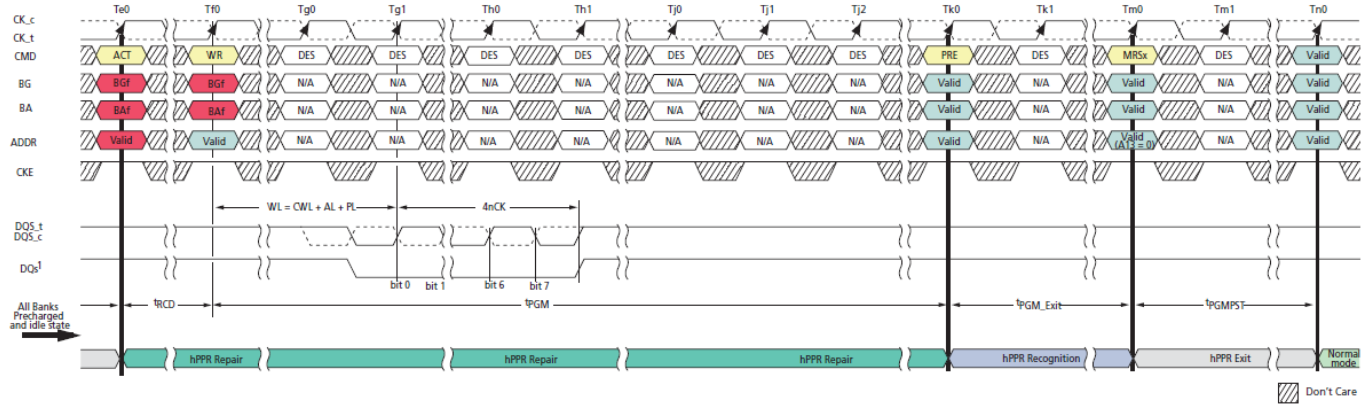


Table 40. DDR4 hPPR Timing Parameters DDR4-1600 through DDR4-3200

Parameter	Symbol	Min	Max	Unit
hPPR programming time	^{t}PGM (x16)	2000	-	ms
hPPR precharge exit time	^{t}PGM_Exit	15	-	ns
hPPR exit time	^{t}PGMPST	50	-	µs

sPPR Row Repair

Soft post package repair (sPPR) is a way to quickly, but temporarily, repair a row element in a bank on a DRAM device, where hPPR takes longer but permanently repairs a row element. sPPR mode is entered in a similar fashion as hPPR, sPPR uses MR4[5] while hPPR uses MR4[13]. sPPR is disabled with MR4[5] = 0, which is the normal state, and sPPR is enabled with MR4[5] = 1, which is the sPPR enabled state.

sPPR requires the same guard key sequence as hPPR to qualify the MR4 PPR entry. After sPPR entry, an ACT command will capture the target bank and target row, herein seed row, where the row repair will be made. After tRCD time, a WR command is used to select the individual DRAM, through the DQ bits, to transfer the repair address into an internal register in the DRAM. After a write recovery time and PRE command, the sPPR mode can be exited and normal operation can resume.

The DRAM will retain the soft repair information as long as VDD remains within the operating region unless rewritten by a subsequent sPPR entry to the same bank. If DRAM power is removed or the DRAM is reset, the soft repair will revert to the unrepaired state. hPPR and sPPR should not be enabled at the same time; sPPR does not have to be disabled and cleared prior to entering hPPR mode, but sPPR must be disabled and cleared prior to entering MBIST-PPR mode.

With sPPR, DDR4 can repair one row per bank. When a subsequent sPPR request is made to the same bank, the subsequently issued sPPR address will replace the previous sPPR address. When the hPPR resource for a bank is used up, the bank should be assumed to not have available resources for sPPR. If a repair sequence is issued to a bank with no repair resource available, the DRAM will ignore the programming sequence.

The bank receiving sPPR change is expected to retain memory array data in all rows except for the seed row and its associated row addresses. If the data in the memory array in the bank under sPPR repair is not required to be retained, then the handling of the seed row's addresses is not of interest and can be ignored. If the data in the memory array is required to be retained in the bank under sPPR mode, then prior to executing the sPPR mode, the seed row and its associated row addresses should be backed up and subsequently restored after sPPR has been completed. sPPR associated seed row addresses are specified in the Table below; BA0 is not required by DRAMs however it is JEDEC reserved.

Table 41. sPPR Associated Rows

sPPR Associated Row Address							
BA0*	A17	A16	A15	A14	A13	A1	A0

All banks must be precharged and idle. DBI and CRC modes must be disabled, and all sPPR timings must be followed as shown in the timing diagram that follows.

All other commands except those listed in the following sequences are illegal.

1. Issue MR4[5] 1 to enter sPPR mode enable.
   a) All DQ are driven HIGH.
2. Issue four consecutive guard key commands (shown in the table below) to MR0 with each command separated by tMOD. Please note that JEDEC recently added the four guard key entry used for hPPR to sPPR entry; early DRAMs may not require four guard key entry code. A prudent controller design should accommodate either option in case an earlier DRAM is used.
   a) Any interruption of the key sequence by other commands, such as ACT, WR, RD, PRE, REF, ZQ and NOP, are not allowed.
   b) If the guard key bits are not entered in the required order or interrupted with other MR commands, sPPR will not be enabled, and the programming cycle will result in a NOP.
   c) When the sPPR entry sequence is interrupted and followed by ACT and WR commands, these commands will be conducted as normal DRAM commands.
   d) JEDEC allows A6:0 to be "Don't Care" on 4Gb and 8Gb devices from a supplier perspective and the user should rely on vendor datasheet.

Table 42. PPR MR0 Guard Key Settings

MR0	BG[1:0]	BA[1:0]	A17:12	A11	A10	A9	A8	A7	A6:0
First guard key	0	0	xxxxxx	1	1	0	0	1	1111111
Second guard key	0	0	xxxxxx	0	1	1	1	1	1111111
Third guard key	0	0	xxxxxx	1	0	1	1	1	1111111
Fourth guard key	0	0	xxxxxx	0	0	1	1	1	1111111

3. After ^{t}MOD, issue an ACT command with failing BG and BA with the row address to be repaired.
4. After ^{t}RCD, issue a WR command with BG and BA of failing row address.
   a) The address must be at valid levels, but the address is a "Don't Care."
5. All DQ of the target DRAM should be driven LOW for 4*n*CK (bit 0 through bit 7) after WL (WL = CWL + AL + PL) in order for sPPR to initiate repair.
   a) Repair **will be** initiated to the target DRAM only if all DQ during bit 0 through bit 7 are LOW.
   b) Repair **will not be** initiated to the target DRAM if any DQ during bit 0 through bit 7 is HIGH.
      i) JEDEC states: All DQs of target DRAM should be LOW for 4^{t}CK. If HIGH is driven to all DQs of a DRAM consecutively for equal to or longer than the first 2^{t}CK, then DRAM does not conduct hPPR and retains data if REF command is properly issued; if all DQs are neither LOW for 4^{t}CK nor HIGH for equal to or longer than the first 2^{t}CK, then hPPR mode execution is unknown.
   c) DQS should function normally.
6. REF command may NOT be issued at anytime while in sPPR mode.
7. Issue PRE after tWR time so that the device can repair the target row during ^{t}WR time.
   a) Wait ^{t}PGM_Exit_s after PRE to allow the device to recognize the repaired target row address.
8. Issue MR4[5] 0 command to sPPR mode disable.
   a) Wait ^{t}PGMPST_s for sPPR mode exit to complete.
   b) After ^{t}PGMPST_s has expired, any valid command may be issued.

The entire sequence from sPPR mode enable through sPPR mode disable may be repeated if more than one repair is to be done.

After sPPR mode has been exited, the DRAM controller can confirm if the target row was repaired correctly by writing data into the target row and reading it back.

Figure 68. sPPR – Entry

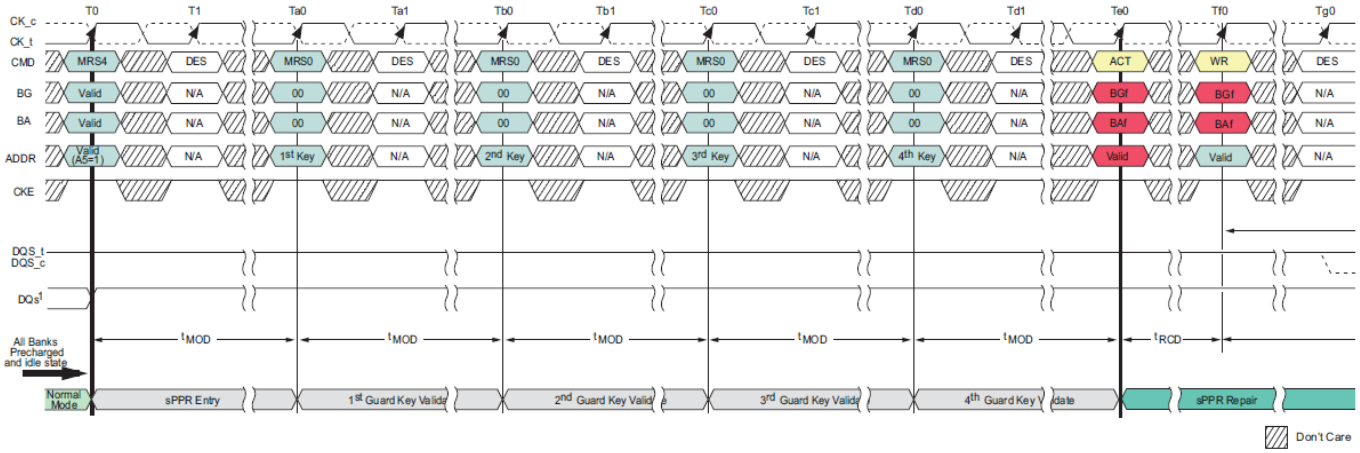


Figure 69. sPPR – Repair and Exit

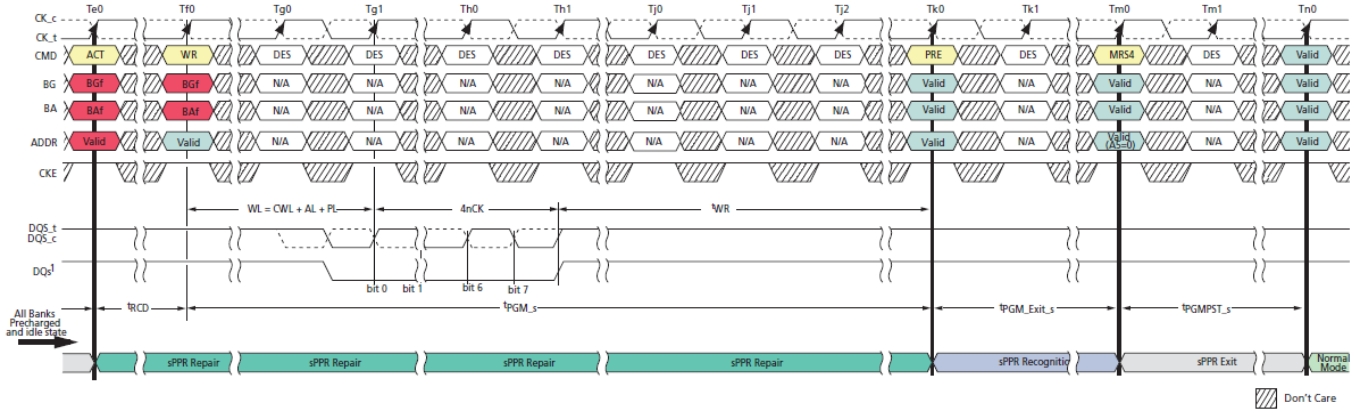


Table 43. DDR4 sPPR Timing Parameters DDR4-1600 through DDR4-3200

Parameter	Symbol	Min	Max	Unit
sPPR programming time	^{t}PGM (x16)_s	^{t}RCD(MIN)+ WL + 4nCK + ^{t}WR(MIN)	-	ns
sPPR precharge exit time	^{t}PGM_Exit_s	20	-	ns
sPPR exit time	^{t}PGMPST_s	^{t}MOD	-	ns

MBIST-PPR

DDR4 devices can support optional memory built-in self-test post-package repair (MBIST-PPR) to help with hard failures such as single-bit or multi-bit failures in a single device so that weak cells can be scanned and repaired during the initialization phase. The DRAM will use vendor-specific patterns to investigate the status of all cell arrays and automatically perform PPR for weak bits during this operation.

This operation introduces proactive, automated PPR by the DRAM, and it is recommended to be done for a very first boot-up at least. After that, it is at the controller's discretion whether to activate MBIST. MBIST mode can only be entered from the all banks idle state. The DLL is required to be enabled and locked prior to MBIST-PPR execution.

MBIST-PPR resources are separated from normal hPPR/sPPR resources. MBIST-PPR resources are typically used for initial scan and repair, and hPPR/sPPR resources must still satisfy the number of repair elements, one per BG, specified in the DDR4 Bank Group Timing Examples. Once the MBIST-PPR is completed, the DRAM will update the status flag in MPR3[7] of MPR page 3. Detailed status is described in the MPR Page and MPRx Definitions.

The test time of MBIST-PPR will not exceed 10 seconds for all mono-die DRAM densities. For DDP devices, test time will be 20 seconds.

The controller is required to inject an MRS command to enter this operation. The controller sets MR4:A0 to 1, followed by MR0 commands for the guard key. Then the DRAM enters MBIST-PPR operation.

The ALERT_n signal notifies the host of the status of this operation. When the controller sets MR4:A0 to 1, followed by the MR0 guard key sequence, the DRAM drives ALERT_n to 0. Once the MBIST-PPR is completed, the DRAM drives ALERT_n to 1 to notify the controller that this operation is completed. DRAM data will not be guaranteed after the MBIST-PPR operation.

Table 44. MBIST-PPR Timing Parameter

Parameter		Value		Unit
		Min	Max	
^{t}SELFHEAL	Monolithic	-	10	s
	DDP	-	20	s

MBIST-PPR Procedure

The following sequences are required for MBIST-PPR and are shown in the figure below.

1. The DRAM needs to finalize initialization, MR training, and ZQ calibration prior to entering MBIST-PPR.
2. Four consecutive guard key commands must be issued to MR0, with each command separated by ^{t}MOD. The PPR guard key settings are the same whether performing sPPR, hPPR, or MBIST-PPR mode.
3. Anytime after Tk in the Read Termination Disable Window 15, the host must set MR4:A0 to 1, followed by subsequent MR0 guard key sequences (which is identical to typical hPPR/sPPR guard key sequences and specified in Read Termination Disable Window table) to start MBIST-PPR operation, and the DRAM drives the ALERT_n signal to 0.
4. During MBIST-PPR mode, only DESELECT commands are allowed.
5. The ODT pin must be driven LOW during MBIST-PPR to satisfy DODTLoff from time Tb0 until Tc2.
   The DRAM may or may not provide R_{TT_PARK} termination during MBIST-PPR regardless of whether R_{TT_PARK} is enabled in MR5.

Figure 70. MBIST-PPR Sequence

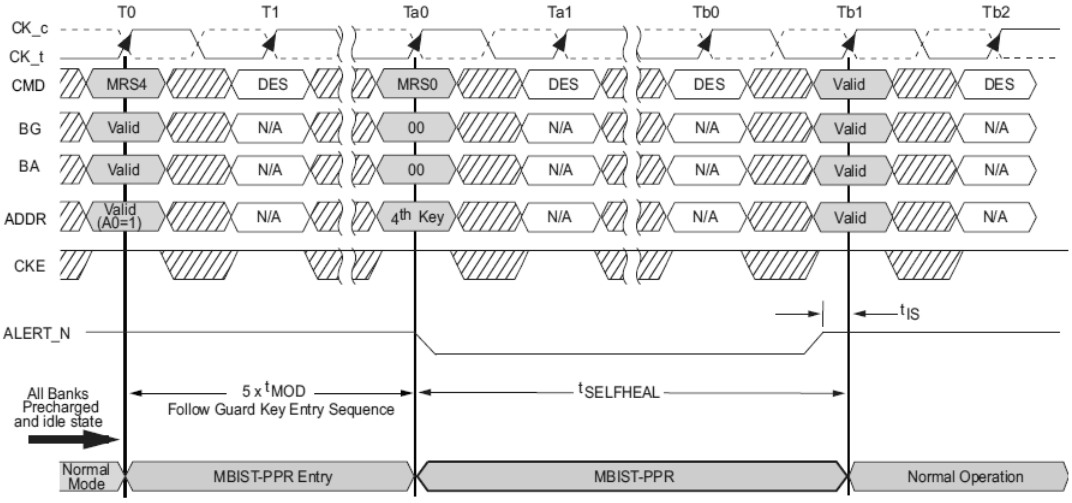


Table 45. MPR Page3 Configuration for MBIST-PPR

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA[1:0]	00 = MPR0	DC	DC	DC	DC	DC	DC	DC	DC	Read-only
	01 = MPR1	DC	DC	DC	DC	DC	DC	DC	DC	
	10 = MPR2	DC	DC	DC	DC	DC	DC	DC	DC	
	11 = MPR3	MBIST-PPR Support	DC	MBIST-PPR Transparency		MAC				

MPR Location	Address Bit	Funtion	Data	Notes
11 = MPR3	7	MBIST-PPR Support	0: Don't Support 1: Support	1
11 = MPR3	5:4	MBIST-PPR Transparency	00_B: MBIST-PPR hasn't run since init OR no fails found during most recent MBIST-PPR	1,2
			01_B: Repaired all found fails during most recent run	1
			10_B: Unrepairable fails found during most recent run	1
			11_B: MBIST-PPR should be run again	1,3

Notes:

1. MPR bits are cleared either by a power-up sequence or re-initialization by RESET_n signal
2. The host should track whether MBIST-PPR has run since INIT. If MBIST-PPR is performed and it finds no fails, this transparency state will remain set to 00B
3. This state does not imply that MBIST-PPR is required to run again. This implies that additional repairable fails were found during the most recent MBIST-PPR beyond what could be repaired in the ^{t}SELFHEAL window.

hPPR/sPPR/MBIST-PPR Support Identifier

Table 46. DDR4 Repair Mode Support Identifier

MPR Page 2	A7	A6	A5	A4	A3	A2	A1	A0
	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
MPR0	hPPR [*1]	sPPR [*2]	R_{TT_WR}	Temp sensor		CRC	R_{TT_WR}	

MPR Page 3	A7	A6	A5	A4	A3	A2	A1	A0
	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
MPR3	MBIST-PPR Support 3 [*3]	Don't Care	MBIST-PPR Transparency		MAC	MAC	MAC	MAC

Notes:

1. 0 = hPPR mode is not available, 1 = hPPR mode is available.
2. 0 = sPPR mode is not available, 1 = sPPR mode is available.
3. 0 = MBIST-PPR mode is not available, 1 = MBIST-PPR mode is available.
4. Gray shaded areas are for reference only.

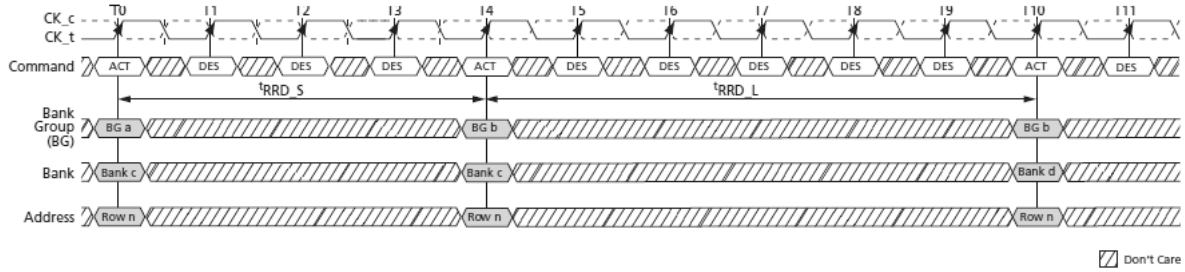
ACTIVATE Command

The ACTIVATE command is used to open (activate) a row in a particular bank for subsequent access.

The values on the BG[1:0] inputs select the bank group, the BA[1:0] inputs select the bank within the bank group, and the address provided on inputs A[17:0] selects the row within the bank. This row remains active (open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

Bank-to-bank command timing for ACTIVATE commands uses two different timing parameters, depending on whether the banks are in the same or different bank group. ^{t}RRD_S (short) is used for timing between banks located in different bank groups. ^{t}RRD_L (long) is used for timing between banks located in the same bank group. Another timing restriction for consecutive ACTIVATE commands [issued at ^{t}RRD (MIN)] is ^{t}FAW (four activate window). Because there is a maximum of four banks in a bank group, the ^{t}FAW parameter applies across different bank groups (five ACTIVATE commands issued at ^{t}RRD_L (MIN) to the same bank group would be limited by ^{t}RC).

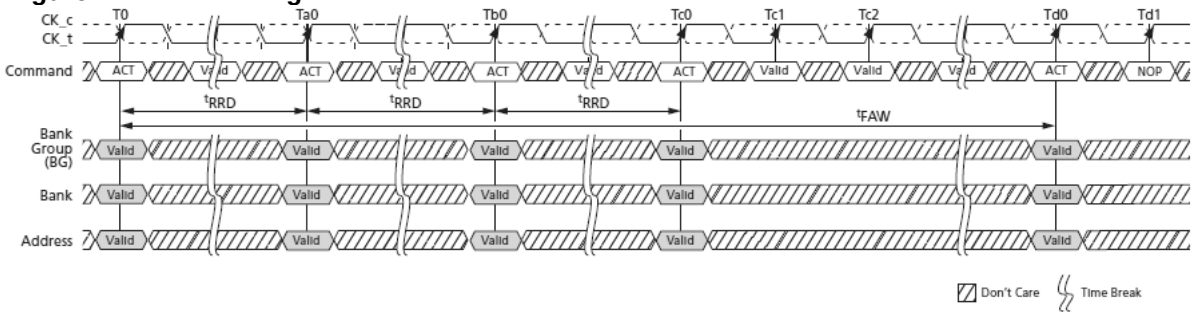
Figure 71. ^{t}RRD Timing



Notes:

1. ^{t}RRD_S; ACTIVATE-to-ACTIVATE command period (short); applies to consecutive ACTIVATE commands to different bank groups (that is, T0 and T4).
2. ^{t}RRD_L; ACTIVATE-to-ACTIVATE command period (long); applies to consecutive ACTIVATE commands to the different banks in the same bank group (that is, T4 and T10).

Figure 72. ^{t}FAW Timing



Notes: 1. ^{t}FAW; four activate windows.

PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation for a specified time (^{t}RP) after the PRECHARGE command is issued. An exception to this is the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters.

After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

The auto precharge feature is engaged when a READ or WRITE command is issued with A10 HIGH. The auto precharge feature uses the RAS lockout circuit to internally delay the PRECHARGE operation until the ARRAY RESTORE operation has completed. The RAS lockout circuit feature allows the PRECHARGE operation to be partially or completely hidden during burst READ cycles when the auto precharge feature is engaged. The PRECHARGE operation will not begin until after the last data of the burst write sequence is properly stored in the memory array.

REFRESH Command

The REFRESH command (REF) is used during normal operation of the device. This command is nonpersistent, so it must be issued each time a refresh is required. The device requires REFRESH cycles at an average periodic interval of ^{t}REFI. When CS_n, RAS_n/A16, and CAS_n/A15 are held LOW and WE_n/A14 HIGH at the rising edge of the clock, the device enters a REFRESH cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time, ^{t}RP (MIN), before the REFRESH command can be applied. The refresh addressing is generated by the internal DRAM refresh controller. This makes the address bits “Don’t Care” during a refresh command. An internal address counter supplies the addresses during the REFRESH cycle. No control of the external address bus is required once this cycle has started. When the REFRESH cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the REFRESH command and the next valid command, except DES, must be greater than or equal to the minimum REFRESH cycle time ^{t}RFC (MIN), as shown in.

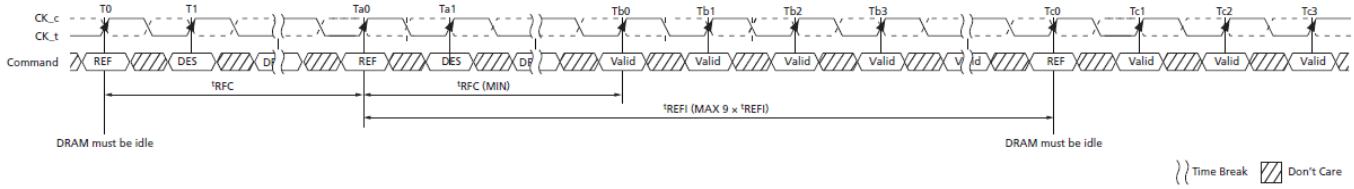
Note: The ^{t}RFC timing parameter depends on memory density.

In general, a REFRESH command needs to be issued to the device regularly every ^{t}REFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling-in the REFRESH command. A limited number REFRESH commands can be postponed depending on refresh mode: a maximum of 8 REFRESH commands can be postponed when the device is in 1X refresh mode; a maximum of 16 REFRESH commands can be postponed when the device is in 2X refresh mode; and a maximum of 32 REFRESH commands can be postponed when the device is in 4X refresh mode.

When 8 consecutive REFRESH commands are postponed, the resulting maximum interval between the surrounding REFRESH commands is limited to 9 x ^{t}REFI. For both the 2X and 4X refresh modes, the maximum interval between surrounding REFRESH commands allowed is limited to 17 x ^{t}REFI2 and 33 x ^{t}REFI4, respectively.

A limited number REFRESH commands can be pulled-in as well. A maximum of 8 additional REFRESH commans can be issued in advance or “pulled-in” in 1X refresh mode, a maximum of 16 additional REFRESH commands can be issued when in advance in 2X refresh mode, and a maximum of 32 additional REFRESH commands can be issued in advance when in 4X refresh mode. Each of these REFRESH commands reduces the number of regular REFRESH commands required later by one. The resulting maximum interval between two surrounding REFRESH commands is limited to 9 x ^{t}REFI, 17 x ^{t}RFEI2, or 33 x ^{t}REFI4. At any given time, a maximum of 16 REF commands can be issued within 2 x ^{t}REFI, 32 REF2 commands can be issued within 4 x ^{t}REFI2, and 64 REF4 commands can be issued within 8 x ^{t}REFI4 (larger densities are limited by ^{t}RFC1, ^{t}RFC2, and ^{t}RFC4, respectively, which must still be met).

Figure 73. REFRESH Command Timing



Notes:

1. Only DES commands are allowed after a REFRESH command is registered until ^{t}RFC (MIN) expires.
2. Time interval between two REFRESH commands may be extended to a maximum of 9 x ^{t}REFI.

Figure 74. Postponing REFRESH Commands (Example)

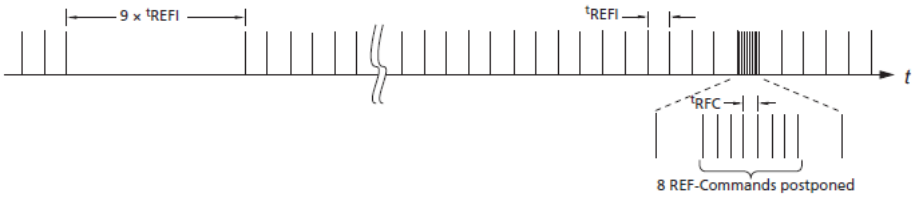
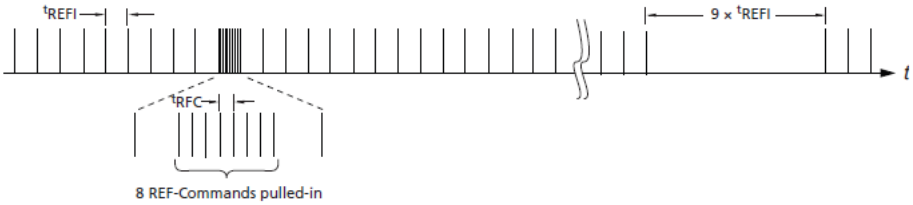


Figure 75. Pulling In REFRESH Commands (Example)



Temperature-Controlled Refresh Mode

During normal operation, temperature-controlled refresh (TCR) mode disabled, the device must have a REFRESH command issued once every ^{t}REFI, except for what is allowed by posting (see REFRESH Command section). This means a REFRESH command must be issued once every 7.8µs if T_C is less than or equal to 85°C, once every 3.9µs if T_C is greater than 85°C. TCR mode is disabled by setting MR4[3] = 0 while TCR mode is enabled by setting MR4[3] = 1. When TCR mode is enabled (MR4[3] = 1), the Temperature Mode must be selected where MR4[2] = 0 enables the Normal Temperature Mode.

When TCR mode is enabled, the device will register the externally supplied REFRESH command and adjust the internal refresh period to be longer than ^{t}REFI of the normal temperature range, when allowed, by skipping REFRESH commands with the proper gear ratio. The DRAM must have the correct refresh rate applied externally; the internal refresh rate is determined by the DRAM based upon the temperature.

Normal Temperature Mode

REFRESH commands should be issued to the device with the refresh period equal to ^{t}REFI of normal temperature range (0°C to 85°C). The system must guarantee that the T_C does not exceed 85°C when ^{t}REFI of the normal temperature range is used. The device may adjust the internal refresh period to be longer than ^{t}REFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio when T_C is below 85°C. The internal refresh period is automatically adjusted inside the DRAM, and the DRAM controller does not need to provide any additional control.

Table 47. Normal ^{t}REFI Refresh (TCR Enabled)

Temperature	Normal Temperature Mode	
	External Refresh Period	Internal Refresh Period
$T_C \leqq 85°C$	7.8µs	$\geqq$7.8µs
85°C < $T_C \leqq 95°C$	3.9µs	

Fine Granularity Refresh Mode

Mode Register and Command Truth Table

The REFRESH cycle time (^{t}RFC) and the average refresh interval (^{t}REFI) can be programmed by the MRS command. The appropriate setting in the mode register will set a single set of REFRESH cycle times and average refresh interval for the device (fixed mode), or allow the dynamic selection of one of two sets of REFRESH cycle times and average refresh interval for the device (on-the-fly mode [OTF]).

OTF mode must be enabled by MRS before any OTF REFRESH command can be issued.

Table 48. MRS Definition

MR3[8]	MR3[7]	MR3[6]	Refresh Rate Mode
0	0	0	Normal mode (fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	On-the-fly 1x/2x
1	1	0	On-the-fly 1x/4x
1	1	1	Reserved

There are two types of OTF modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register MR3 [8:6]. When either of the two OTF modes is selected, the device evaluates the BG0 bit when a REFRESH command is issued, and depending on the status of BG0, it dynamically switches its internal refresh configuration between 1x and 2x (or 1x and 4x) modes, and then executes the corresponding REFRESH operation.

Table 49. REFRESH Command Truth Table

Function	CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n /A14	BG1	BG0	BA0-1	A10/AP	A[9:0], A[12:11], A[20:16]	MR3[8:6]
Refresh (Fixed rate)	L	H	L	L	H	V	V	V	V	V	0vv
Refresh (on-the-fly 1x)	L	H	L	L	H	V	L	V	V	V	1vv
Refresh (on-the-fly 2x)	L	H	L	L	H	V	H	V	V	V	101
Refresh (on-the-fly 4x)											110

^{t}REFI and ^{t}RFC parameters

The default refresh rate mode is fixed 1x mode where REFRESH commands should be issued with the normal rate; that is, ^{t}REFI1 =^{t}REFI(base) (for $T_C \leq 85°C$), and the duration of each REFRESH command is the normal REFRESH cycle time (^{t}RFC1). In 2x mode (either fixed 2x or OTF 2x mode), REFRESH commands should be issued to the device at the double frequency (^{t}REFI2 = ^{t}REFI(base)/2) of the normal refresh rate. In 4x mode, the REFRESH command rate should be quadrupled (^{t}REFI4 = ^{t}REFI(base)/4). Per each mode and command type, the tRFC parameter has different values as defined in the following table.

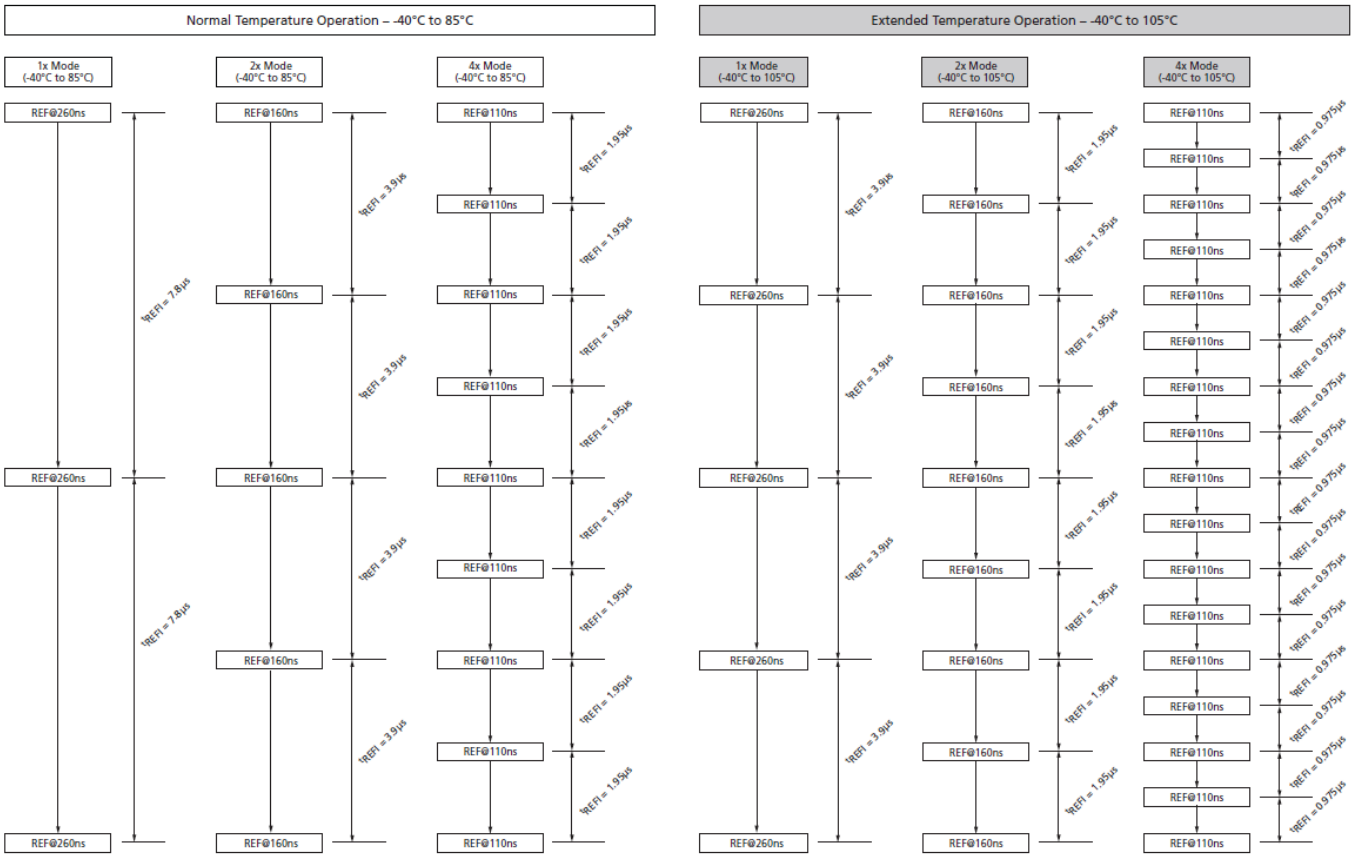
For discussion purposes, the REFRESH command that should be issued at the normal refresh rate and has the normal REFRESH cycle duration may be referred to as a REF1x command. The REFRESH command that should be issued at the double frequency (^{t}REFI2 = ^{t}REFI(base)/2) may be referred to as a REF2x command. Finally, the REFRESH command that should be issued at the quadruple rate (^{t}REFI4 = ^{t}REFI(base)/4) may be referred to as a REF4x command.

In the fixed 1x refresh rate mode, only REF1x commands are permitted. In the fixed 2x refresh rate mode, only REF2x commands are permitted. In the fixed 4x refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the OTF 1x/4x refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

Table 50. ^{t}REFI and ^{t}RFC parameters

Refresh Mode	Parameter		8 Gb	Unit
	^{t}REFI(base)		7.8	us
1X mode	^{t}REFI1	$0°C \leq T_C \leq 85°C$	^{t}REFI(base)	us
		$85°C < T_C \leq 95°C$	^{t}REFI(base)/2	us
	^{t}RFC1(min)		350	ns
2X mode	^{t}REFI2	$0°C \leq T_C \leq 85°C$	^{t}REFI(base)/2	us
		$85°C < T_C \leq 95°C$	^{t}REFI(base)/4	us
	^{t}RFC2(min)		260	ns
4X mode	^{t}REFI4	$0°C \leq T_C \leq 85°C$	^{t}REFI(base)/4	us
		$85°C < T_C \leq 95°C$	^{t}REFI(base)/8	us
	^{t}RFC4(min)		160	ns

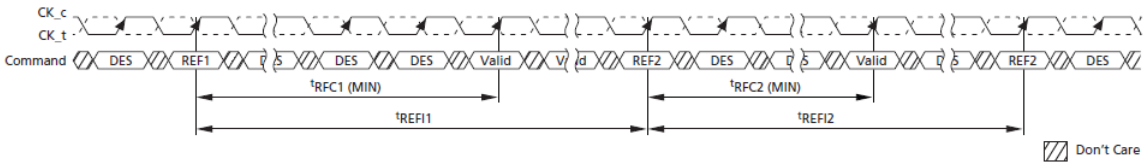
Figure 76. 4Gb with Fine Granularity Refresh Mode Example



Changing Refresh Rate

If the refresh rate is changed by either MRS or OTF. New ^{t}REFI and ^{t}RFC parameters will be applied from the moment of the rate change. When the REF1x command is issued to the DRAM, ^{t}REF1 and ^{t}RFC1 are applied from the time that the command was issued; when the REF2x command is issued, ^{t}REF2 and ^{t}RFC2 should be satisfied.

Figure 77. OTF REFRESH Command Timing



The following conditions must be satisfied before the refresh rate can be changed. Otherwise, data retention cannot be guaranteed.

- In the fixed 2x refresh rate mode or the OTF 1x/2x refresh mode, an even number of REF2x commands must be issued because the last change of the refresh rate mode with an MRS command before the refresh rate can be changed by another MRS command.
- In the OTF1x/2x refresh rate mode, an even number of REF2x commands must be issued between any two REF1x commands.
- In the fixed 4x refresh rate mode or the OTF 1x/4x refresh mode, a multiple-of-four number of REF4x commands must be issued because the last change of the refresh rate with an MRS command before the refresh rate can be changed by another MRS command.
- In the OTF1x/4x refresh rate mode, a multiple-of-four number of REF4x commands must be issued between any two REF1x commands.

There are no special restrictions for the fixed 1x refresh rate mode. Switching between fixed and OTF modes keeping the same rate is not regarded as a refresh rate change.

Usage with TCR Mode

If the temperature controlled refresh mode is enabled, only the normal mode (fixed 1x mode, MR3[8:6] = 000) is allowed. If any other refresh mode than the normal mode is selected, the temperature controlled refresh mode must be disabled.

Self Refresh Entry and Exit

The device can enter self refresh mode anytime in 1x, 2x, and 4x mode without any restriction on the number of REFRESH commands that have been issued during the mode before the self refresh entry.

However, upon self refresh exit, extra REFRESH command(s) may be required, depending on the condition of the self refresh entry.

The conditions and requirements for the extra REFRESH command(s) are defined as follows:

- In the fixed 2x refresh rate mode or the enable-OTF 1x/2x refresh rate mode, it is recommended there be an even number of REF2x commands before entry into self refresh after the last self refresh exit, REF1x command, or MRS command that set the refresh mode. If this condition is met, no additional REFRESH commands are required upon self refresh exit. In the case that this condition is not met, either one extra REF1x command or two extra REF2x commands must be issued upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval (^{t}REFI).
- In the fixed 4x refresh rate mode or the enable-OTF 1x/4x refresh rate mode, it is recommended there be a multiple-of-four number of REF4x commands before entry into self refresh after the last self refresh exit, REF1x command, or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon self refresh exit. When this condition is not met, either one extra REF1x command or four extra REF4x commands must be issued upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval (^{t}REFI).

There are no special restrictions on the fixed 1x refresh rate mode.

This section does not change the requirement regarding postponed REFRESH commands. The requirement for the additional REFRESH command(s) described above is independent of the requirement for the postponed REFRESH commands.

Self refresh Operation

The SELF REFRESH command can be used to retain data in the device, even if the rest of the system is powered down. When in self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate SELF REFRESH operation. The SELF REFRESH command is defined by having CS_n, RAS_n, CAS_n, and CKE held LOW with WE_n and ACT_n HIGH at the rising edge of the clock.

Before issuing the SELF REFRESH ENTRY command, the device must be idle with all banks in the precharge state and tRP satisfied. Idle state is defined as: All banks are closed (^{t}RP, ^{t}DAL, and so on, satisfied), no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied (^{t}MRD, ^{t}MOD, ^{t}RFC, ^{t}ZQinit, ^{t}ZQoper, ^{t}ZQCS, and so on). After the SELF REFRESH ENTRY command is registered, CKE must be held LOW to keep the device in self refresh mode. The DRAM automatically disables ODT termination, regardless of the ODT pin, when it enters self refresh mode and automatically enables ODT upon exiting self refresh. During normal operation (DLL_on), the DLL is automatically disabled upon entering self refresh and is automatically enabled (including a DLL reset) upon exiting self refresh.

When the device has entered self refresh mode, all of the external control signals, except CKE and RESET_n, are “Don’t Care.” For proper Self-Refresh operation, all power supply and reference pins (V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}, V_{PP}, and V_{REFCA}) must be at valid levels. The DRAM internal V_{REFDQ} generator circuitry may remain on or be turned off depending on the MR6 bit 7 setting. If the internal V_{REFDQ} circuit is on in self refresh, the first WRITE operation or first write-leveling activity may occur after ^{t}XS time after self refresh exit. If the DRAM internal V_{REFDQ} circuitry is turned off in self refresh, it ensures that the V_{REFDQ} generator circuitry is powered up and stable within the ^{t}XSDLL period when the DRAM exits the self refresh state. The first WRITE operation or first write-leveling activity may not occur earlier than ^{t}XSDLL after exiting self refresh. The device initiates a minimum of one REFRESH command internally within the ^{t}CKE period once it enters self refresh mode.

The clock is internally disabled during a SELF REFRESH operation to save power. The minimum time that the device must remain in self refresh mode is tCKESR/tCKESR_PAR. The user may change the external clock frequency or halt the external clock tCKSRE/tCKSRE_PAR after self refresh entry is registered; however, the clock must be restarted and tCKSRX must be stable before the device can exit SELF REFRESH operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit command (SRX, combination of CKE going high and Deselect on command bus) is registered, following timing delay must be satisfied:

Commands that do not require locked DLL:

- ^{t}XS = ACT, PRE, PREA, REF, SRE, and PDE.
- ^{t}XS_FAST = ZQCL, ZQCS, and MRS commands. For an MRS command, only DRAM CL, WR/RTP register, and DLL reset in MR0; $R_{TT(NOM)}$ register in MR1; the CWL and $R_{TT(WR)}$ registers in MR2; and gear-down mode register in MR3; WRITE and READ preamble registers in MR4; $R_{TT(PARK)}$ register in MR5; Data rate and V_{REFDQ} calibration value registers in MR6 may be accessed provided the DRAM is not in per-DRAM mode. Access to other DRAM mode registers must satisfy ^{t}XS timing. WRITE commands (WR, WRS4, WRS8, WRA, WRAS4, and WRAS8) that require synchronous ODT and dynamic ODT controlled by the WRITE command require a locked DLL.

Commands that require locked DLL in the normal operating range:

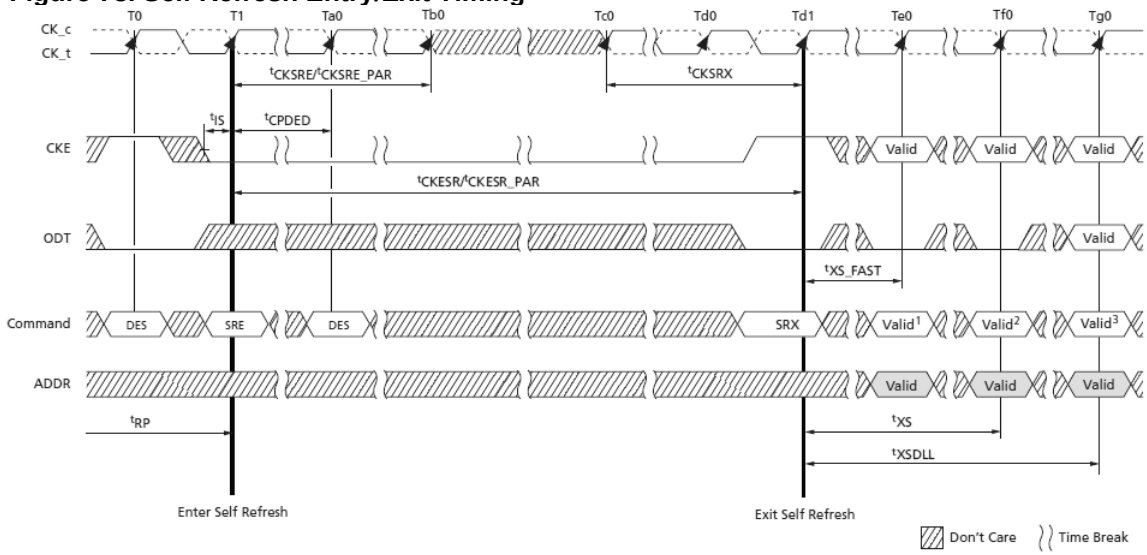
^{t}XSDLL - RD, RDS4, RDS8, RDA, RDAS4 and RDAS8 (unlike DDR3, WR, WRS4, WRS8, WRA, WRAS4 and WRAS8 because synchronous ODT is required).

Depending on the system environment and the amount of time spent in self refresh, ZQ CALIBRATION commands may be required to compensate for the voltage and temperature drift described in the ZQ CALIBRATION Commands section. To issue ZQ CALIBRATION commands, applicable timing requirements must be satisfied (see the ZQ Calibration Timing figure).

CKE must remain HIGH for the entire self refresh exit period ^{t}XSDLL for proper operation except for self refresh re-entry. Upon exit from self refresh, the device can be put back into self refresh mode or power-down mode after waiting at least ^{t}XS period and issuing one REFRESH command (refresh period of ^{t}RFC). The DESELECT command must be registered on each positive clock edge during the self refresh exit interval ^{t}XS. ODT must be turned off during ^{t}XSDLL.

The use of self refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self refresh mode. Upon exit from self refresh, the device requires a minimum of one extra REFRESH command before it is put back into self refresh mode.

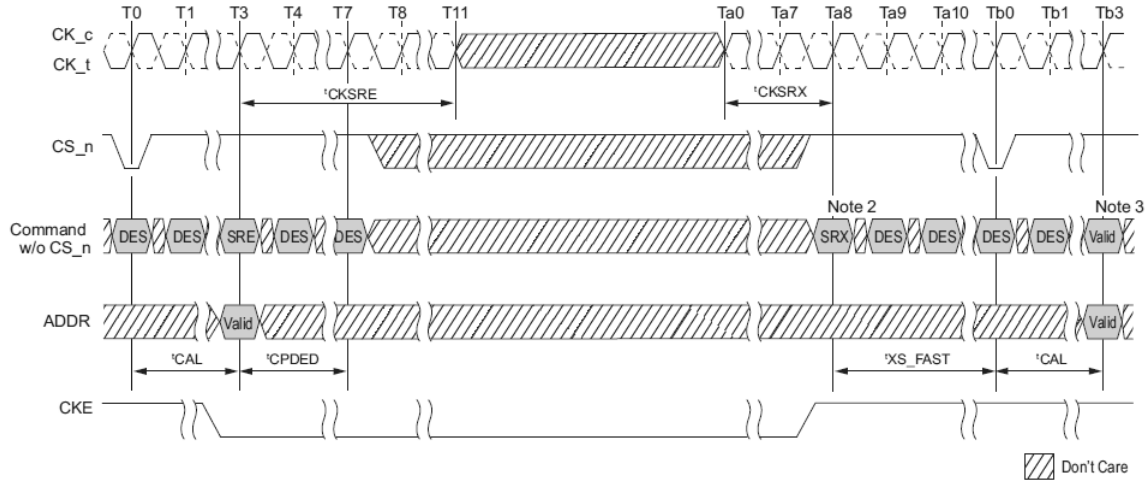
Figure 78. Self Refresh Entry/Exit Timing



Notes:

1. Only MRS (limited to those described in the SELF REFRESH Operation section), ZQCS, or ZQCL commands are allowed.
2. Valid commands not requiring a locked DLL.
3. Valid commands requiring a locked DLL.

Figure 79. Self Refresh Entry/Exit Timing with CAL Mode



Notes:

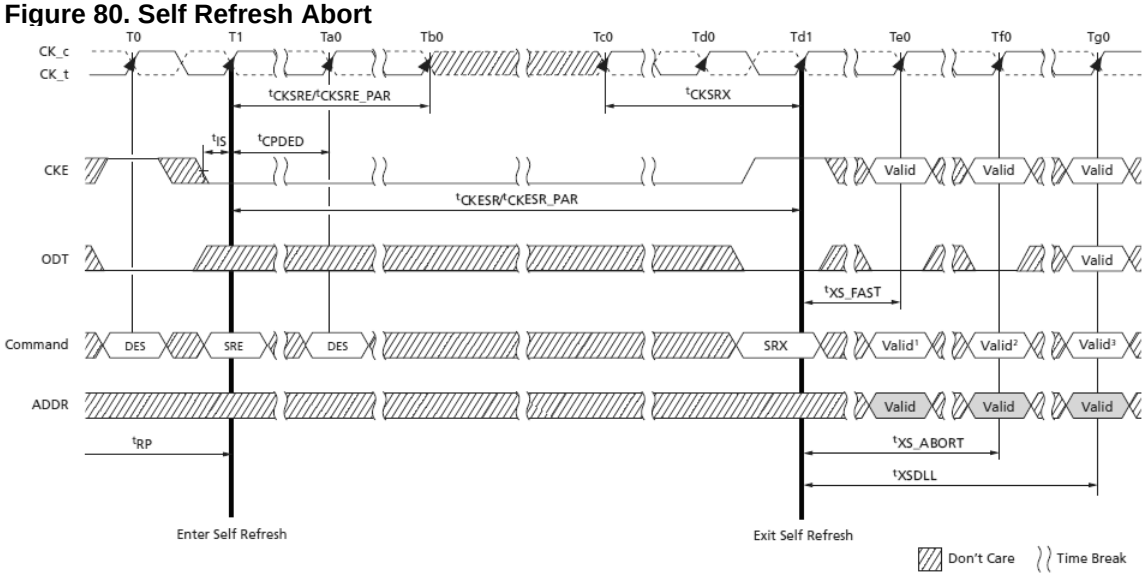
1. ^{t}CAL = 3*n*CK, ^{t}CPDED = 4*n*CK, ^{t}CKSRE/^{t}CKSRE_PAR = 8*n*CK, ^{t}CKSRX = 8*n*CK, ^{t}XS_FAST = ^{t}REFC4 (MIN) + 10ns.
2. CS_n = HIGH, ACT_n = "Don't Care," RAS_n/A16 = "Don't Care," CAS_n/A15 = "Don't Care," WE_n/A14 = "Don't Care."
3. Only MRS (limited to those described in the SELF REFRESH Operations section), ZQCS, or ZQCL commands are allowed.
4. The figure only displays ^{t}XS_FAST timing, but ^{t}CAL must also be added to any ^{t}XS and ^{t}XSDLL associated commands during CAL mode.

Self Refresh Abort

The exit timing from self refresh exit to the first valid command not requiring a locked DLL is ^{t}XS. The value of ^{t}XS is (^{t}RFC1 + 10ns). This delay allows any refreshes started by the device time to complete.

^{t}RFC continues to grow with higher density devices, so ^{t}XS will grow as well. An MRS bit enables the self refresh abort mode. If the bit is disabled, the controller uses ^{t}XS timings (location MR4, bit 9). If the bit is enabled, the device aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command not requiring a locked DLL after a delay of ^{t}XS_ABORT. Upon exit from self refresh, the device requires a minimum of one extra REFRESH command before it is put back into self refresh mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.

Figure 80. Self Refresh Abort



Notes:

1. Only MRS (limited to those described in the SELF REFRESH Operation section), ZQCS, or ZQCL commands are allowed.
2. Valid commands not requiring a locked DLL with self refresh abort mode enabled in the mode register.
3. Valid commands requiring a locked DLL.

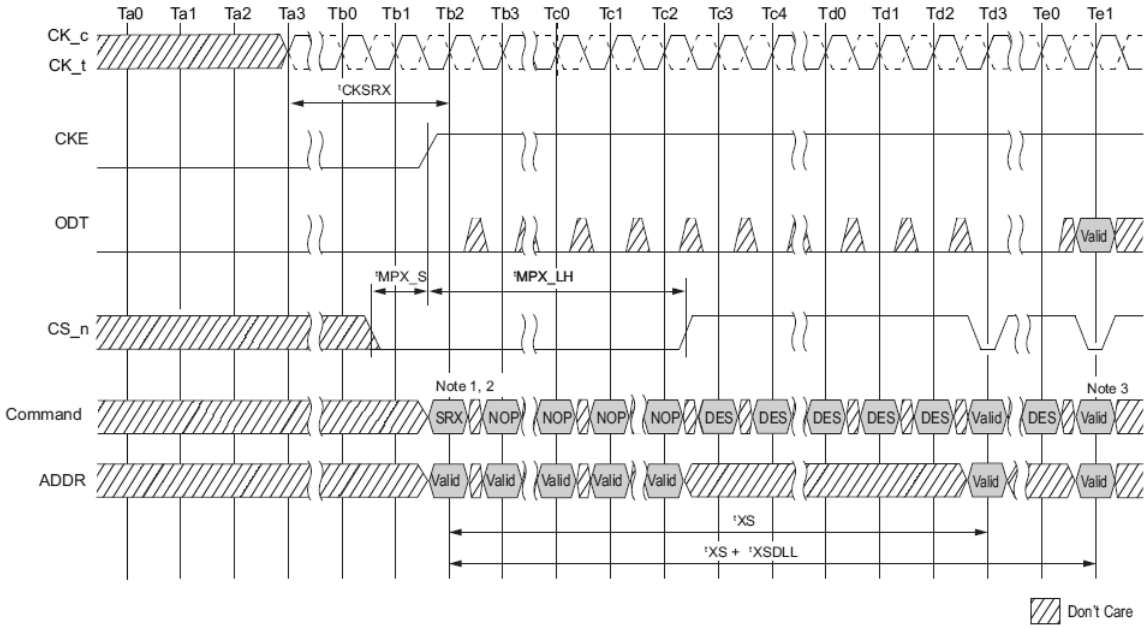
Self Refresh Exit with NOP Command

Exiting self refresh mode using the NO OPERATION command (NOP) is allowed under a specific system application. This special use of NOP allows for a common command/address bus between active DRAM devices and DRAM(s) in maximum power saving mode. Self refresh mode may exit with NOP commands provided:

- The device entered self refresh mode with CA parity, CAL, and gear-down disabled.
- ^{t}MPX_S and tMPX_LH are satisfied.
- NOP commands are only issued during ^{t}MPX_LH window.

No other command is allowed during the ^{t}MPX_LH window after an SELF REFRESH EXIT (SRX) command is issued.

Figure 81. Self Refresh Exit with NOP Command



Power-Down Mode

Power-down is synchronously entered when CKE is registered LOW (along with a DESELECT command). CKE is not allowed to go LOW when the following operations are in progress: MRS command, MPR operations, ZQCAL operations, DLL locking, or READ/WRITE operations. CKE is allowed to go LOW while any other operations, such as ROW ACTIVATION, PRECHARGE or auto precharge, or REFRESH, are in progress, but the power-down IDD specification will not be applied until those operations are complete. The timing diagrams that follow illustrate power-down entry and exit.

For the fastest power-down exit timing, the DLL should be in a locked state when power-down is entered. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper READ operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as the controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, CKE and RESET_n. In power-down mode, DRAM ODT input buffer deactivation is based on Mode Register 5, bit 5 (MR5[5]). If it is configured to 0b, ODT input buffer remains on and ODT input signal must be at valid logic level. If it is configured to 1b, ODT input buffer is deactivated and DRAM ODT input signal may be floating and DRAM does not provide $R_{TT(Nom)}$ termination. Note that DRAM continues to provide $R_{TT(Park)}$ termination if it is enabled in DRAM mode register MR5[8:6]. To protect DRAM internal delay on CKE line to block the input signals, multiple Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as ^{t}CPDED. CKE_low will result in deactivation of command and address receivers after ^{t}CPDED has expired.

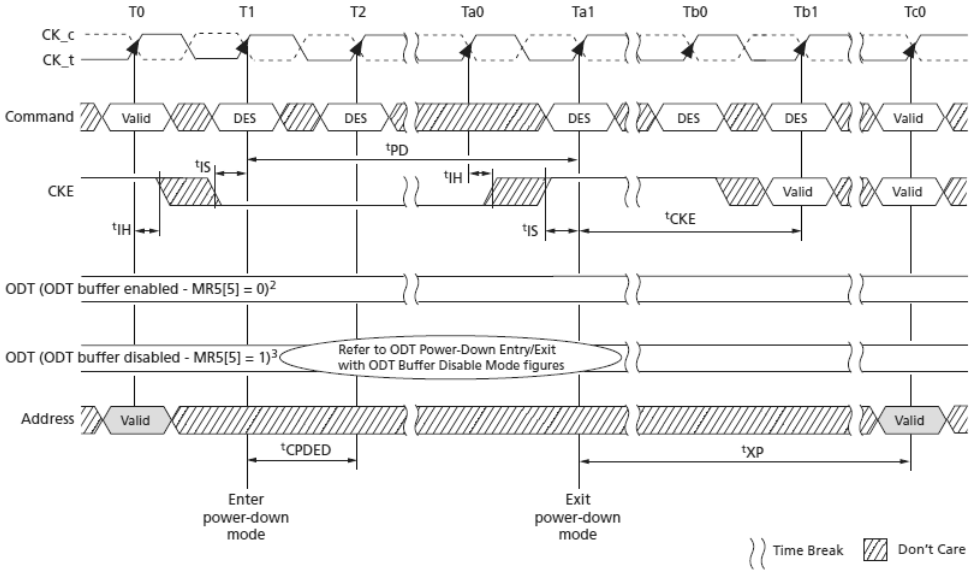
Table 51. Power-Down Entry Definitions

Status of DRAM	DLL	Power-Down Exit	Relevant Parameters
Active (A bank or more Open)	On	Fast	^{t}XP to any valid command
Precharged (All banks Precharged)	On	Fast	^{t}XP to any valid command.

The DLL is kept enabled during precharge power-down or active power-down. In power-down mode, CKE is LOW, RESET_n is HIGH, and a stable clock signal must be maintained at the inputs of the device. ODT should be in a valid state, but all other input signals are "Don't Care." (If RESET_n goes LOW during power-down, the device will be out of power-down mode and in the reset state.) CKE LOW must be maintained until ^{t}CKE has been satisfied. Power-down duration is limited by 9 x ^{t}REFI.

The power-down state is synchronously exited when CKE is registered HIGH (along with DES command). CKE HIGH must be maintained until ^{t}CKE has been satisfied. The ODT input signal must be at a valid level when the device exits from power-down mode, independent of MR1 bit [10:8] if $R_{TT(NOM)}$ is enabled in the mode register. If $R_{TT(NOM)}$ is disabled, the ODT input signal may remain floating. A valid, executable command can be applied with power-down exit latency, ^{t}XP, after CKE goes HIGH. Power-down exit latency is defined in the AC Specifications table.

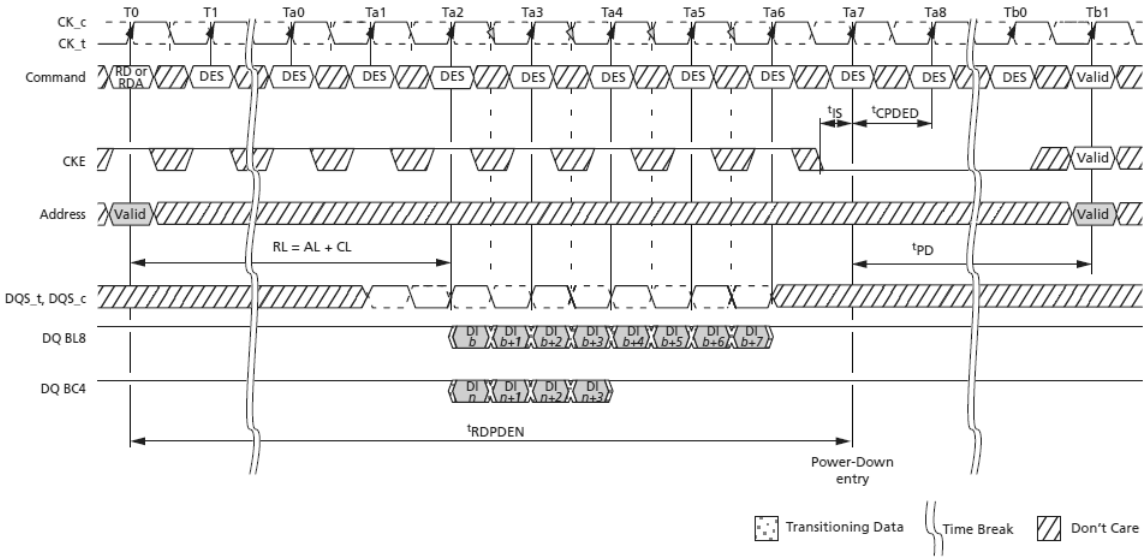
Figure 82. Active Power-Down Entry and Exit



Notes:

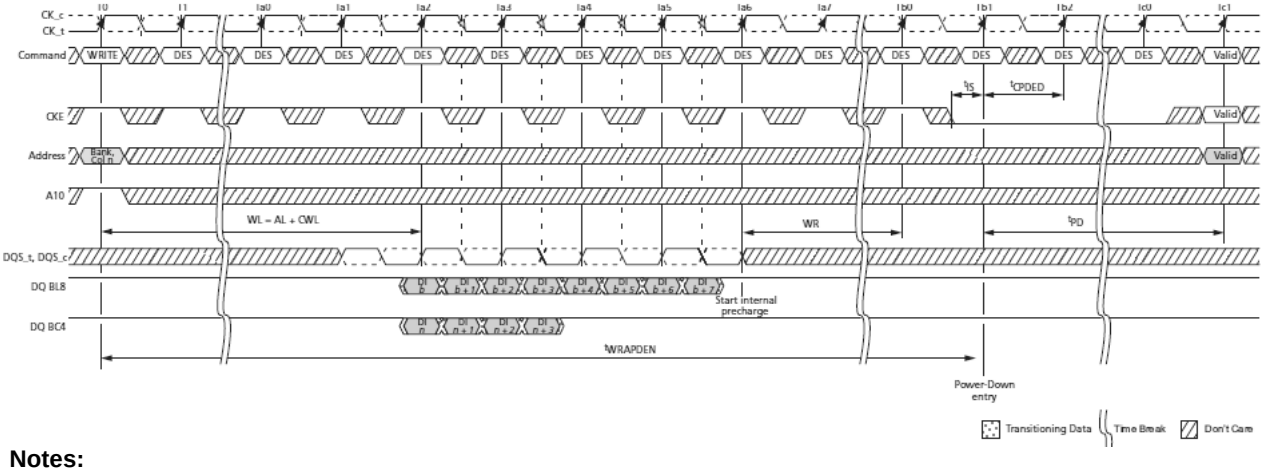
1. Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.
2. ODT pin driven to a valid state; MR5[5] = 0 (normal setting).
3. ODT pin drive/float timing requirements for the ODT input buffer disable option (for additional power savings during active power-down) is described in the section for ODT Input Buffer Disable Mode for Power-Down; MR5[5] = 1.

Figure 83. Power-Down Entry After Read and Read with Auto Precharge



Note: 1. DI n (or b) = data-in from column n (or b).

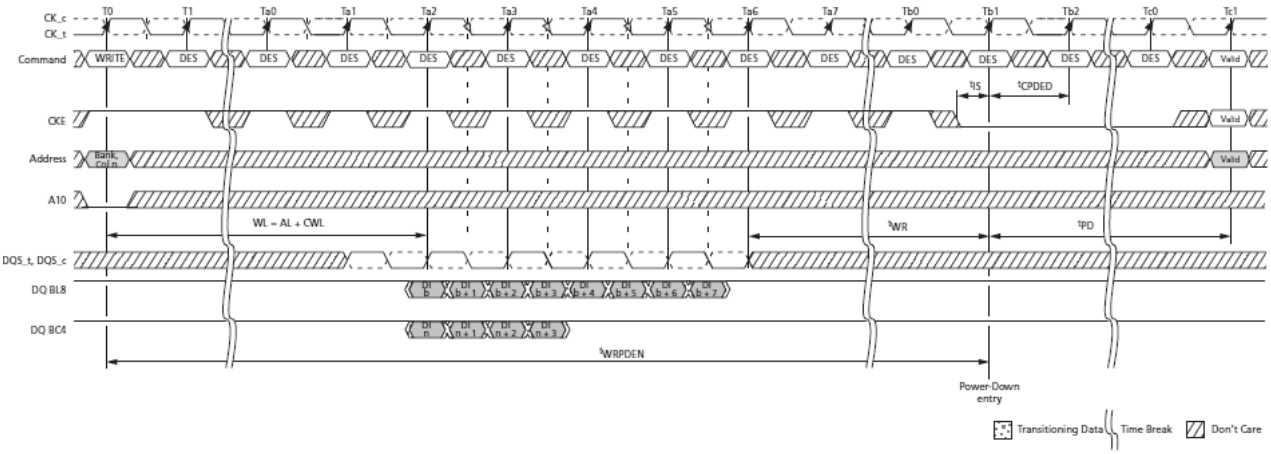
Figure 84. Power-Down Entry After Write and Write with Auto Precharge



Notes:

1. DI n (or b) = data-in from column n (or b).
2. Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.

Figure 85. Power-Down Entry After Write



Note: 1. DI n (or b) = data-in from column n (or b).

Figure 86. Precharge Power-Down Entry and Exit

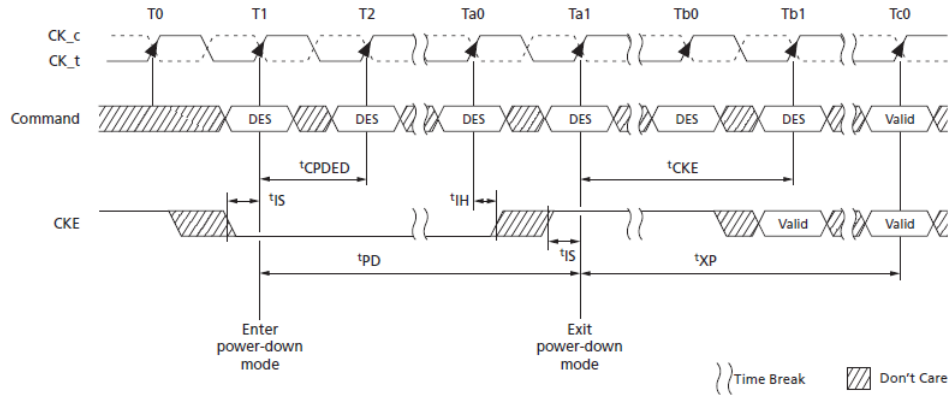


Figure 87. Refresh Command to Power-Down Entry

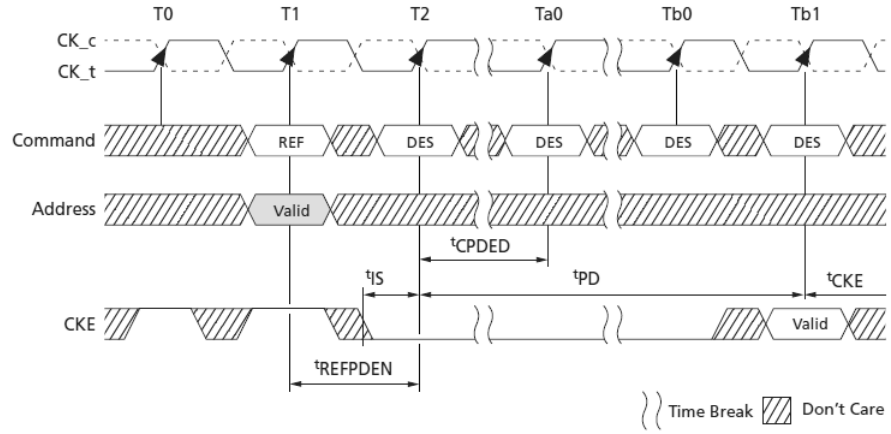


Figure 88. Activate Command to Power-Down Entry

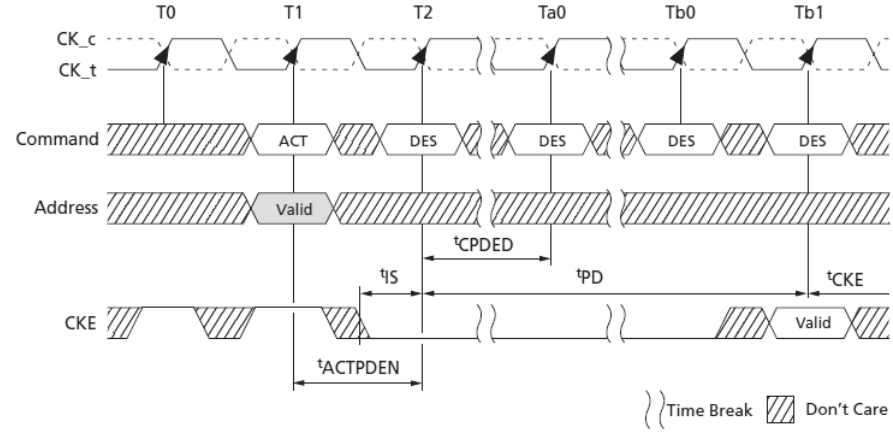


Figure 89. Precharge/Precharge all Command to Power-Down Entry

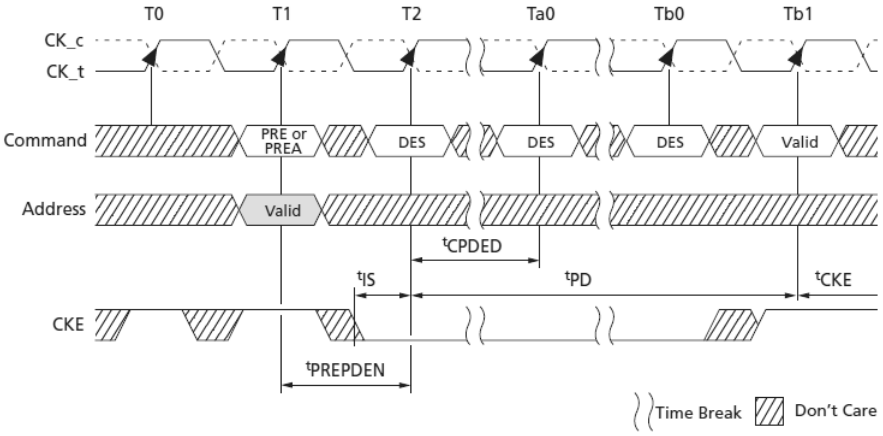
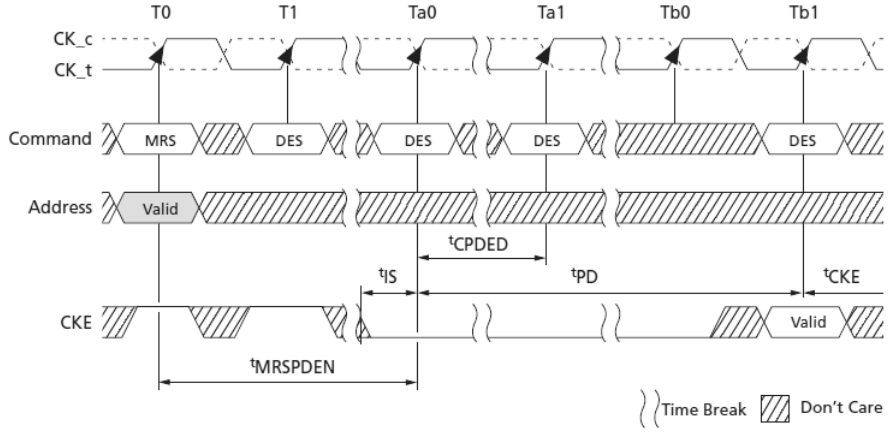


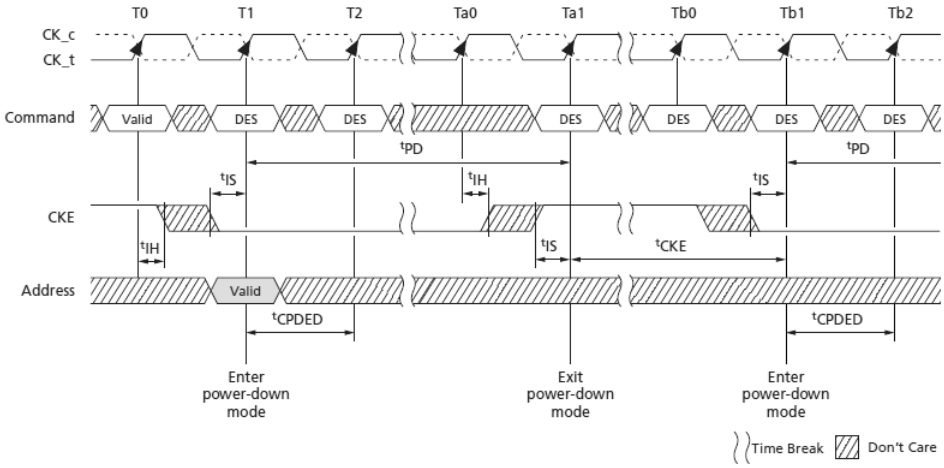
Figure 90. MRS Command to Power-Down Entry



Power-Down clarifications – Case 1

When CKE is registered LOW for power-down entry, ^{t}PD (MIN) must be satisfied before CKE can be registered HIGH for power-down exit. The minimum value of parameter ^{t}PD (MIN) is equal to the minimum value of parameter ^{t}CKE (MIN) as shown in the Timing Parameters by Speed Bin table. A detailed example of Case 1 follows.

Figure 91. Power-Down Entry/Exit Clarification – Case 1



Power-Down Entry, Exit Timing with CAL

Command/Address latency is used and additional timing restrictions are required when entering power-down, as noted in the following figures.

Figure 92. Active Power-Down Entry and Exit Timing with CAL

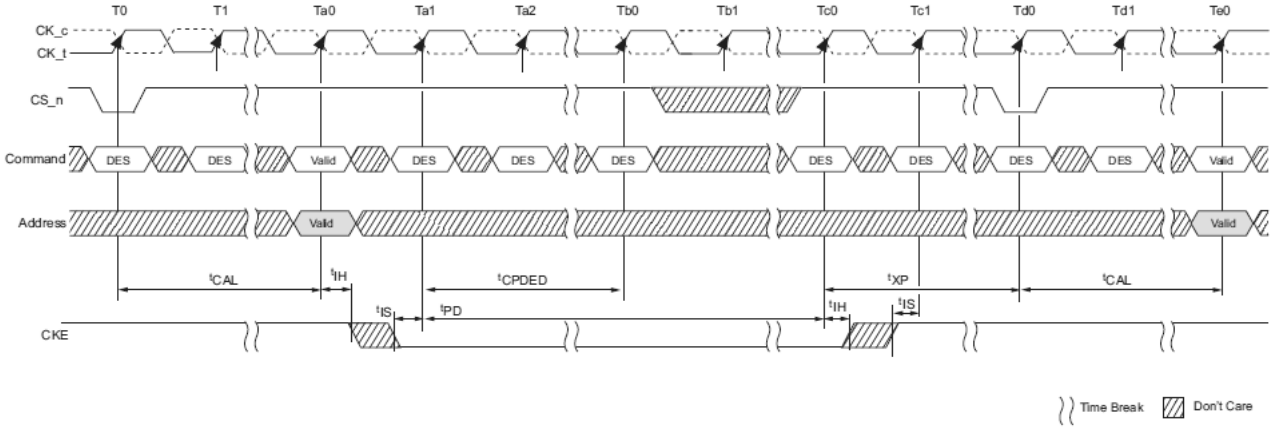
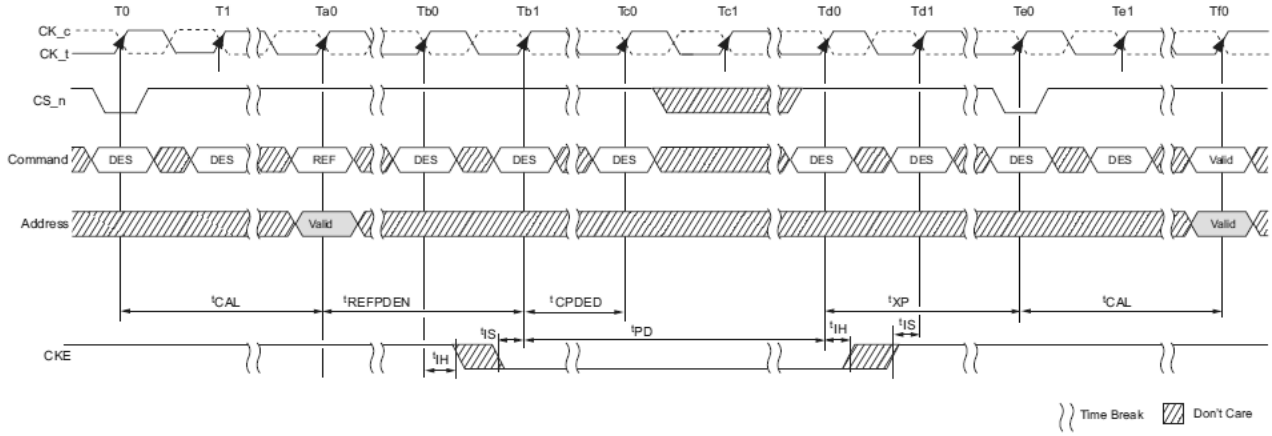


Figure 93. REFRESH Command to Power-Down Entry with CAL



ODT Input Buffer Disable Mode for Power-Down

DRAM does not provide R_{TT_NOM} termination during power-down when ODT input buffer deactivation mode is enabled in MR5 bit A5.

To account for DRAM internal delay on CKE line to disable the ODT buffer and block the sampled output, the host controller must continuously drive ODT to either low or high when entering power down (from ^{t}DODTLoff+1 prior to CKE low till ^{t}CPDED after CKE low).

The ODT signal is allowed to float after ^{t}CPDEDmin has expired. In this mode, R_{TT_NOM} termination corresponding to sampled ODT at the input when CKE is registered low (and tANPD before that) may be either R_{TT_NOM} or R_{TT_PARK}. ^{t}ANPD is equal to (WL-1) and is counted backwards from PDE.

Figure 94. ODT Power-Down Entry with ODT Buffer Disable Mode

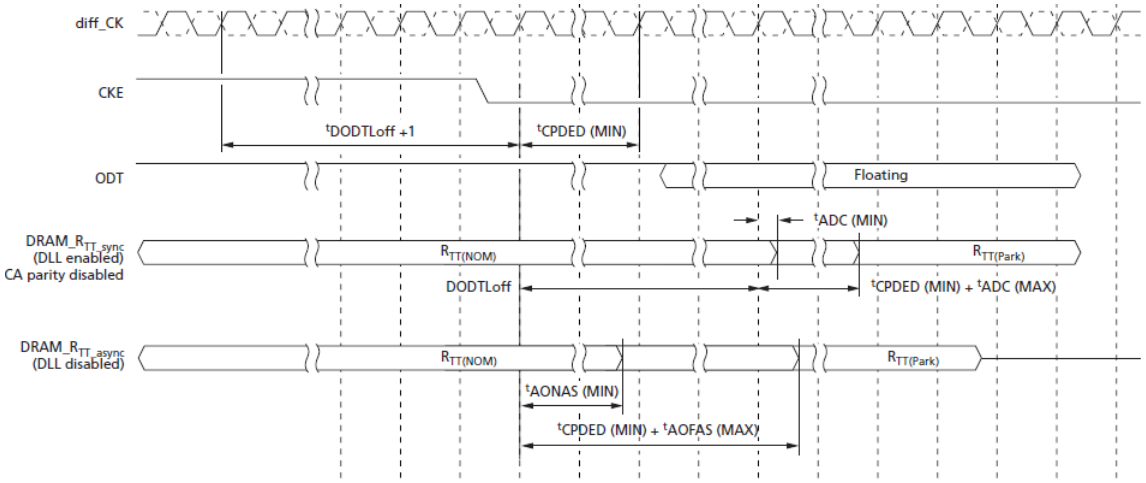
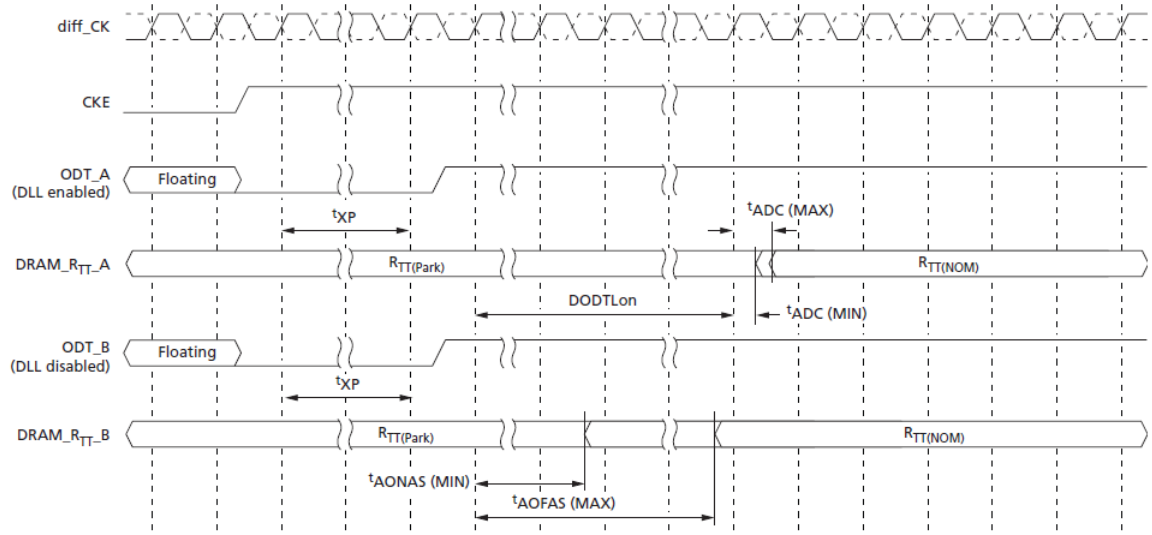


Figure 95. ODT Power-Down Exit with ODT Buffer Disable Mode

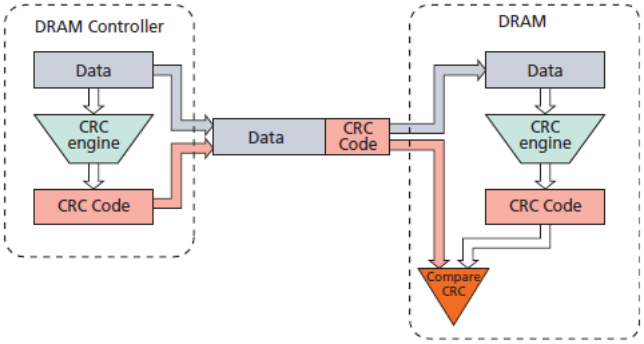


CRC Write Data Feature

CRC Write Data

The CRC write data feature takes the CRC generated data from the DRAM controller and compares it to the internally CRC generated data and determines whether the two match (no CRC error) or do not match (CRC error).

Figure 96. CRC Write Data Operation



WRITE CRC DATA Operation

A DRAM controller generates a CRC checksum using a 72-bit CRC tree and forms the write data frames, as shown in the following CRC data mapping tables for the x4, x8, and x16 configurations. A x4 device has a CRC tree with 32 input data bits used, and the remaining upper 40 bits D[71:32] being 1s. A x8 device has a CRC tree with 64 input data bits used, and the remaining upper 8 bits dependant upon whether DM_n/DBI_n is used (1s are sent when not used). A x16 device has two identical CRC trees each, one for the lower byte and one for the upper byte, with 64 input data bits used by each, and the remaining upper 8 bits on each byte dependant upon whether DM_n/DBI_n is used (1s are sent when not used). For a x8 and x16 DRAMs, the DRAM memory controller must send 1s in transfer 9 location whether or not DM_n/DBI_n is used.

The DRAM checks for an error in a received code word D[71:0] by comparing the received checksum against the computed checksum and reports errors using the ALERT_n signal if there is a mismatch.

The DRAM can write data to the DRAM core without waiting for the CRC check for full writes when DM is disabled. If bad data is written to the DRAM core, the DRAM memory controller will try to overwrite the bad data with good data; this means the DRAM controller is responsible for data coherency when DM is disabled. However, in the case where both CRC and DM are enabled via MRS (that is, persistent mode), the DRAM will not write bad data to the core when a CRC error is detected.

DBI_n and CRC Both Enabled

The DRAM computes the CRC for received written data D[71:0]. Data is not inverted back based on DBI before it is used for computing CRC. The data is inverted back based on DBI before it is written to the DRAM core.

DM_n and CRC Both Enabled

When both DM and write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array. If there is a CRC error, the DRAM blocks the WRITE operation and discards the data. If a CRC error is encountered from a WRITE with auto precharge (WRA), the DRAM will not block the precharge. The Nonconsecutive WRITE (BL8/BC4-OTF) with 2^{t}CK Preamble and Write CRC in Same or Different Bank Group and the WRITE (BL8/BC4-OTF/Fixed) with 1^{t}CK Preamble and Write CRC in Same or Different BankGroup figures in the WRITE Operation section show timing differences when DM is enabled.

DM_n and DBI_n Conflict During Writes with CRC Enabled

Both write DBI_n and DM_n can not be enabled at the same time; read DBI_n and DM_n can be enabled at the same time.

CRC and Write Preamble Restrictions

When write CRC is enabled:

- And 1^{t}CK WRITE preamble mode is enabled, a ^{t}CCD_S or ^{t}CCD_L of 4 clocks is not allowed.
- And 2^{t}CK WRITE preamble mode is enabled, a ^{t}CCD_S or ^{t}CCD_L of 6 clocks is not allowed.

CRC Simultaneous Operation Restrictions

When write CRC is enabled, neither MPR writes nor per-DRAM mode is allowed.

CRC Polynomial

The CRC polynomial used by DDR4 is the ATM-8 HEC, $X^8 + X^2 + X^1 + 1$.
A combinatorial logic block implementation of this 8-bit CRC for 72 bits of data includes 272 two-input XOR gates contained in eight 6-XOR-gate-deep trees.
The CRC polynomial and combinatorial logic used by DDR4 is the same as used on GDDR5.
The error coverage from the DDR4 polynomial used is shown in the following table.

Table 52. CRC Error Detection Coverage

Error Type	Detection Capability
Random single-bit errors	100%
Random double-bit errors	100%
Random odd count errors	100%
Random multibit UI vertical column error detection excluding DBI bits	100%

CRC Combinatorial Logic Equations

```
module CRC8_D72;
// polynomial: (0 1 2 8)
// data width: 72
// convention: the first serial data bit is D[71]
//initial condition all 0 implied
// "^" = XOR
function [7:0]
nextCRC8_D72;
input [71:0] Data;
input [71:0] D;
reg [7:0] CRC;
begin
D = Data;
```

CRC[0] =
D[69]^D[68]^D[67]^D[66]^D[64]^D[63]^D[60]^D[56]^D[54]^D[53]^D[52]^D[50]^D[49]^D[48]^D[45]
^D[43]^D[40]^D[39]^D[35]^D[34]^D[31]^D[30]^D[28]^D[23]^D[21]^D[19]^D[18]^D[16]^D[14]^D[12]^D[8]^D[7]^D[6]^D[0];

CRC[1] =
D[70]^D[66]^D[65]^D[63]^D[61]^D[60]^D[57]^D[56]^D[55]^D[52]^D[51]^D[48]^D[46]^D[45]^D[44]^D[43]^D[41]^D[39]^D[36]^D[34
]^D[32]^D[30]^D[29]^D[28]^D[24]^D[23]^D[22]^D[21]^D[20]^D[18]^D[17]^D[16]^D[15]^D[14]^D[13]^D[12]^D[9]^D[6]^D[1]^D[0];

CRC[2] =
D[71]^D[69]^D[68]^D[63]^D[62]^D[61]^D[60]^D[58]^D[57]^D[54]^D[50]^D[48]^D[47]^D[46]^D[44]^D[43]^D[42]^D[39]^D[37]^D[34
]^D[33]^D[29]^D[28]^D[25]^D[24]^D[22]^D[17]^D[15]^D[13]^D[12]^D[10]^D[8]^D[6]^D[2]^D[1]^D[0];

CRC[3] =
D[70]^D[69]^D[64]^D[63]^D[62]^D[61]^D[59]^D[58]^D[55]^D[51]^D[49]^D[48]^D[47]^D[45]^D[44]^D[43]^D[40]^D[38]^D[35]^D[34
]^D[30]^D[29]^D[26]^D[25]^D[23]^D[18]^D[16]^D[14]^D[13]^D[11]^D[9]^D[7]^D[3]^D[2]^D[1];

CRC[4] =
D[71]^D[70]^D[65]^D[64]^D[63]^D[62]^D[60]^D[59]^D[56]^D[52]^D[50]^D[49]^D[48]^D[46]^D[45]^D[44]^D[41]^D[39]^D[36]^D[35
]^D[31]^D[30]^D[27]^D[26]^D[24]^D[19]^D[17]^D[15]^D[14]^D[12]^D[10]^D[8]^D[4]^D[3]^D[2];

CRC[5] =
D[71]^D[66]^D[65]^D[64]^D[63]^D[61]^D[60]^D[57]^D[53]^D[51]^D[50]^D[49]^D[47]^D[46]^D[45]^D[42]^D[40]^D[37]^D[36]^D[32
]^D[31]^D[28]^D[27]^D[25]^D[20]^D[18]^D[16]^D[15]^D[13]^D[11]^D[9]^D[5]^D[4]^D[3];

CRC[6] =
D[67]^D[66]^D[65]^D[64]^D[62]^D[61]^D[58]^D[54]^D[52]^D[51]^D[50]^D[48]^D[47]^D[46]^D[43]^D[41]^D[38]^D[37]^D[33]^D[32
]^D[29]^D[28]^D[26]^D[21]^D[19]^D[17]^D[16]^D[14]^D[12]^D[10]^D[6]^D[5]^D[4];

CRC[7] =
D[68]^D[67]^D[66]^D[65]^D[63]^D[62]^D[59]^D[55]^D[53]^D[52]^D[51]^D[49]^D[48]^D[47]^D[44]^D[42]^D[39]^D[38]^D[34]^D[33
]^D[30]^D[29]^D[27]^D[22]^D[20]^D[18]^D[17]^D[15]^D[13]^D[11]^D[7]^D[6]^D[5];

```
nextCRC8_D72 = CRC;
```

Burst Ordering for BL8

DDR4 supports fixed WRITE burst ordering [A2:A1:A0 = 0:0:0] when write CRC is enabled in BL8 (fixed).

CRC Data Bit Mapping

A x16 device is treated as two x8 devices; a x16 device will have two identical CRC trees implemented.
CRC[7:0] covers data bits D[71:0], and CRC[15:8] covers data bits D[143:72].

Table 53. CRC Data Mapping for x16 Devices, BL8

Function	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
DML_n / DBIL_n	D64	D65	D66	D67	D68	D69	D70	D71	1	1
DQ8	D72	D73	D74	D75	D76	D77	D78	D79	CRC8	1
DQ9	D80	D81	D82	D83	D84	D85	D86	D87	CRC9	1
DQ10	D88	D89	D90	D91	D92	D93	D94	D95	CRC10	1
DQ11	D96	D97	D98	D99	D100	D101	D102	D103	CRC11	1
DQ12	D104	D105	D106	D107	D108	D109	D110	D111	CRC12	1
DQ13	D112	D113	D114	D115	D116	D117	D118	D119	CRC13	1
DQ14	D120	D121	D122	D123	D124	D125	D126	D127	CRC14	1
DQ15	D128	D129	D130	D131	D132	D133	D134	D135	CRC15	1
DMU_n / DBIU_n	D136	D137	D138	D139	D140	D141	D142	D143	1	1

CRC Enabled With BC4

If CRC and BC4 are both enabled, then address bit A2 is used to transfer critical data first for BC4 writes.

CRC with BC4 Data Bit Mapping

There are two identical CRC trees for x16 devices, each have CRC tree inputs of 36 bits.

When A2 = 0, input bits D[67:64] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[67:64] are 1s. The input bits D[139:136] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[139:136] are 1s.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs for D[11:8], and so forth, for the CRC tree. Input bits D[71:68] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[71:68] are 1s. The input bits D[143:140] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[143:140] are 1s.

Table 54. CRC Data Mapping for x16 Devices, BC4

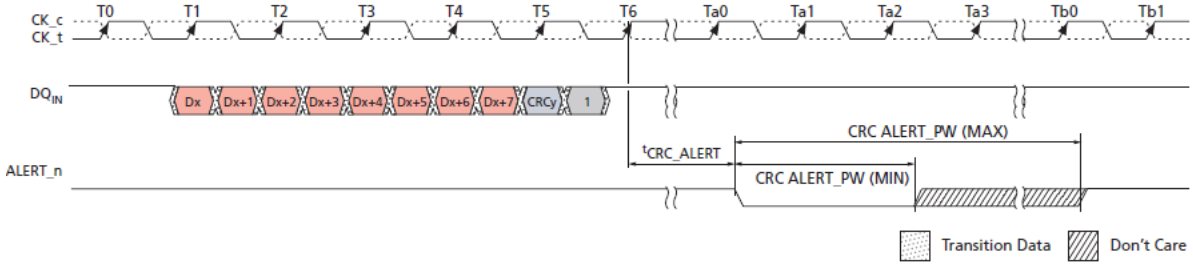
Function	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1
DML_n / DBIL_n	D64	D65	D66	D67	1	1	1	1	1	1
DQ8	D72	D73	D74	D75	1	1	1	1	CRC8	1
DQ9	D80	D81	D82	D83	1	1	1	1	CRC9	1
DQ10	D88	D89	D90	D91	1	1	1	1	CRC10	1
DQ11	D96	D97	D98	D99	1	1	1	1	CRC11	1
DQ12	D104	D105	D106	D107	1	1	1	1	CRC12	1
DQ13	D112	D113	D114	D115	1	1	1	1	CRC13	1
DQ14	D120	D121	D122	D123	1	1	1	1	CRC14	1
DQ15	D128	D129	D130	D131	1	1	1	1	CRC15	1
DMU_n / DBIU_n	D136	D137	D138	D139	1	1	1	1	1	1

CRC Error Handling

The CRC error mechanism shares the same ALERT_n signal as CA parity for reporting write errors to the DRAM. The controller has two ways to distinguish between CRC errors and CA parity errors: 1) Read DRAM mode/MPR registers, and 2) Measure time ALERT_n is LOW. To speed up recovery for CRC errors, CRC errors are only sent back as a "short" pulse; the maximum pulse width is roughly ten clocks (unlike CA parity where ALERT_n is LOW longer than 45 clocks). The ALERT_n LOW could be longer than the maximum limit at the controller if there are multiple CRC errors as the ALERT_n signals are connected by a daisy chain bus. The latency to ALERT_n signal is defined as ^{t}CRC_ALERT in the following figure.

The DRAM will set the error status bit located at MR5[3] to a 1 upon detecting a CRC error, which will subsequently set the CRC error status flag in the MPR error log HIGH (MPR Page1, MPR3[7]). The CRC error status bit (and CRC error status flag) remains set at 1 until the DRAM controller clears the CRC error status bit using an MRS command to set MR5[3] to a 0. The DRAM controller, upon seeing an error as a pulse width, will retry the write transactions. The controller should consider the worst-case delay for ALERT_n (during initialization) and backup the transactions accordingly. The DRAM controller may also be made more intelligent and correlate the write CRC error to a specific rank or a transaction.

Figure 97. CRC Error Reporting

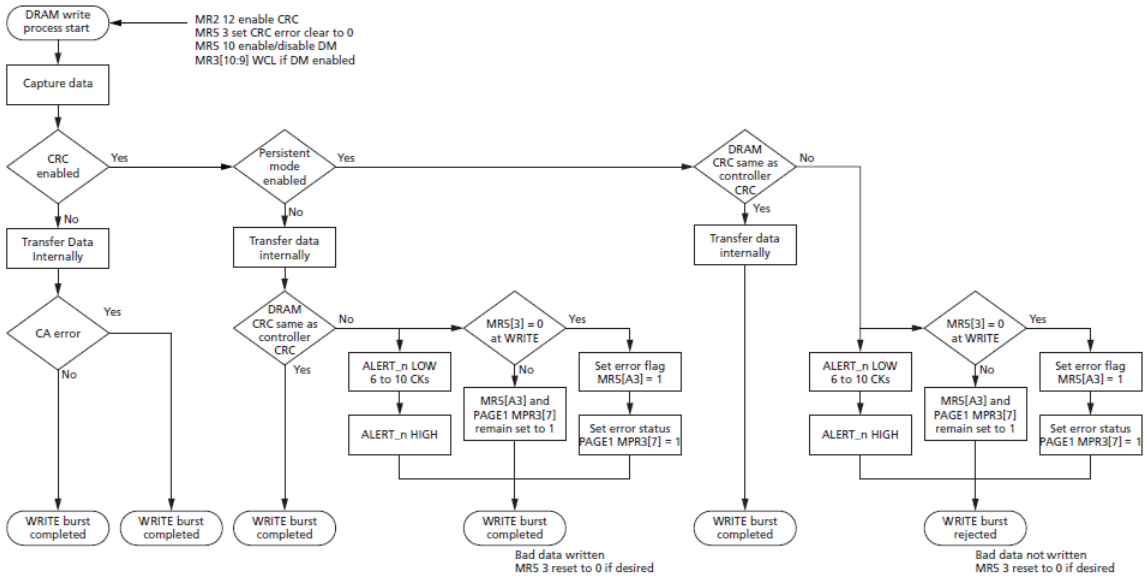


Note:

1. D[71:1] CRC computed by DRAM did not match CRC[7:0] at T5 and started error generating process at T6.
2. CRC ALERT_PW is specified from the point where the DRAM starts to drive the signal LOW to the point where the DRAM driver releases and the controller starts to pull the signal up.
3. Timing diagram applies to x4, x8, and x16 devices.

CRC Write Data Flow Diagram

Figure 98. CA Parity Flow Diagram



Data Bus Inversion (DBI)

The DATA BUS INVERSION (DBI) function is supported only for x16 configurations. DBI opportunistically inverts data bits, and in conjunction with the DBI_n I/O, less than half of the DQs will switch LOW for a given DQS strobe edge. The DBI function shares a common pin with the DATA MASK (DM) and TDQS functions. The DBI function applies to either or both READ and WRITE operations: Write DBI cannot be enabled at the same time the DM function is enabled, and DBI is not allowed during MPR READ operation. Valid configurations for DM and DBI functions are shown below.

Table 55. DBI vs. DM Function Matrix

Read DBI	Write DBI	Data Mask (DM)
Enabled (or Disabled) **MR5[12]=1** (or MR5[12] = 0)	Disabled MR5[11] = 0	Disabled MR5[10] = 0
	Enabled MR5[11] = 1	Disabled MR5[10] = 0
	Disabled MR5[11] = 0	**Enabled** MR5[10] = 1
Disabled MR5[12] = 0	Disabled MR5[11] = 0	Disabled MR5[10] = 0

DBI During a WRITE Operation

If DBI_n is sampled LOW on a given byte lane during a WRITE operation, the DRAM inverts write data received on the DQ inputs prior to writing the internal memory array. If DBI_n is sampled HIGH on a given byte lane, the DRAM leaves the data received on the DQ inputs noninverted. The write DQ frame format is shown below for x16 configurations.

Table 56. DBI Write, DQ Frame Format (x16)

Function	Transfer, Lower (L) and Upper(U)							
	0	1	2	3	4	5	6	7
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
DML_n or DBIL_n	DML0 or DBIL0	DML1 or DBIL1	DML2 or DBIL2	DML3 or DBIL3	DML4 or DBIL4	DML5 or DBIL5	DML6 or DBIL6	DML7 or DBIL7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
DMU_n or DBIU_n	DMU0 or DBIU0	DMU1 or DBIU1	DMU2 or DBIU2	DMU3 or DBIU3	DMU4 or DBIU4	DMU5 or DBIU5	DMU6 or DBIU6	DMU7 or DBIU7

DBI During a READ Operation

If the number of 0 data bits within a given byte lane is greater than four during a READ operation, the DRAM inverts read data on its DQ outputs and drives the DBI_n pin LOW; otherwise, the DRAM does not invert the read data and drives the DBI_n pin HIGH. The read DQ frame format is shown below for x16 configurations.

Table 57. DBI Read, DQ Frame Format (x16)

Function	Transfer, Lower (L) and Upper(U)							
	0	1	2	3	4	5	6	7
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
DML_n or DBIL_n	DBIL0	DBIL1	DBIL2	DBIL3	DBIL4	DBIL5	DBIL6	DBIL7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
DMU_n or DBIU_n	DBIU0	DBIU1	DBIU2	DBIU3	DBIU4	DBIU5	r DBIU6	DBIU7

Data Mask (DS)

The DATA MASK (DM) function, also described as PARTIAL WRITE, is supported only for x16 configurations. The DM function shares a common pin with the DBI_n functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the WRITE DBI function is enabled. The valid configurations for the DM and DBI functions are shown here.

Table 58. DM vs. DBI Function Matrix

Data Mask (DM)	Write DBI	Read DBI
Enabled MR5[10] = 1	Disabled MR5[11] = 0	**Enabled** (or Disabled) MR5[12]=1 (or MR5[12] = 0)
Disabled MR5[10] = 0	Disabled MR5[11] = 0	Disabled MR5[12] = 0
	Enabled MR5[11] = 1	**Enabled** (or Disabled) MR5[12]=1 (or MR5[12] = 0)
	Disabled MR5[11] = 0	**Enabled** (or Disabled) MR5[12]=1 (or MR5[12] = 0)

When enabled, the DM function applies during a WRITE operation. If DM_n is sampled LOW on a given byte lane, the DRAM masks the write data received on the DQ inputs. If DM_n is sampled HIGH on a given byte lane, the DRAM does not mask the data and writes this data into the DRAM core. The DQ frame format for x16 configurations is shown below. If both CRC write and DM are enabled (via MRS), the CRC will be checked and valid prior to the DRAM writing data into the DRAM core. If a CRC error occurs while the DM feature is enabled, CRC write persistent mode will be enabled and data will not be written into the DRAM core. In the case of CRC write enabled and DM disabled (via MRS), that is, CRC write nonpersistent mode, data is written to the DRAM core even if a CRC error occurs.

Table 59. Data Mask, DQ Frame Format (x16)

Function	Transfer, Lower (L) and Upper(U)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
DML_n or DBIL_n	DML0 or DBIL0	DML1 or DBIL1	DML2 or DBIL2	DML3 or DBIL3	DML4 or DBIL4	DML5 or DBIL5	DML6 or DBIL6	DML7 or DBIL7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
DMU_n or DBIU_n	DMU0 or DBIU0	DMU1 or DBIU1	DMU2 or DBIU2	DMU3 or DBIU3	DMU4 or DBIU4	DMU5 or DBIU5	DMU6 or DBIU6	DMU7 or DBIU7

Programmable Preamble Modes and DQS Postambles

The device supports programmable WRITE and READ preamble modes, either the normal 1^{t}CK preamble mode or special 2^{t}CK preamble mode. The 2^{t}CK preamble mode places special timing constraints on many operational features as well as being supported for data rates of DDR4-2400 and faster. The WRITE preamble 1^{t}CK or 2^{t}CK mode can be selected independently from READ preamble 1^{t}CK or 2^{t}CK mode.

READ preamble training is also supported; this mode can be used by the DRAM controller to train or "read level" the DQS receivers.

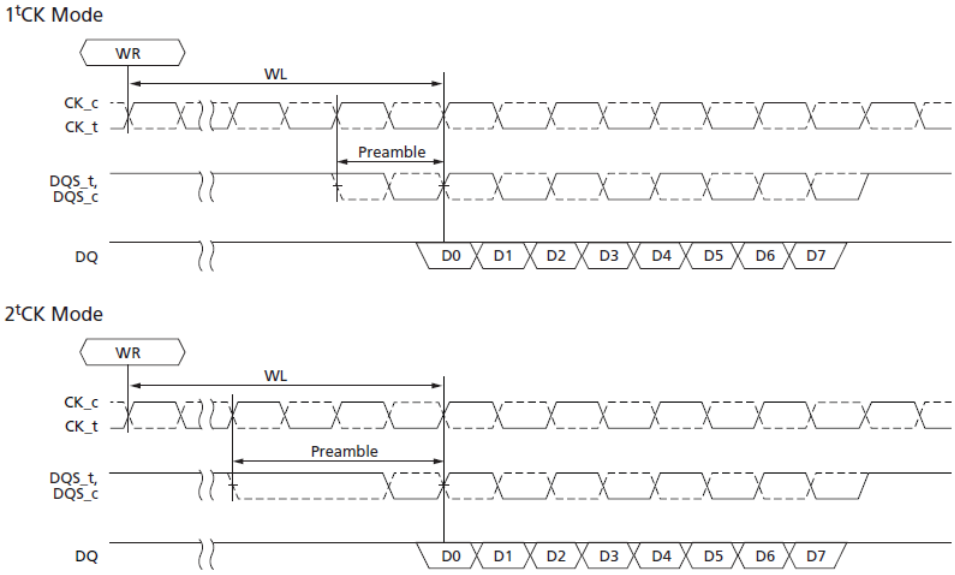
There are ^{t}CCD restrictions under some circumstances:

- When 2^{t}CK READ preamble mode is enabled, a ^{t}CCD_S or ^{t}CCD_L of 5 clocks is not allowed.
- When 2^{t}CK WRITE preamble mode is enabled and write CRC is *not* enabled, a ^{t}CCD_S or ^{t}CCD_L of 5 clocks is not allowed.
- When 2^{t}CK WRITE preamble mode is enabled and write CRC is enabled, a ^{t}CCD_S or ^{t}CCD_L of 6 clocks is not allowed.

WRITE Preamble Mode

MR4[12] = 0 selects 1^{t}CK WRITE preamble mode while MR4[12] = 1 selects 2^{t}CK WRITE preamble mode. Examples are shown in the figures below.

Figure 99. 1^{t}CK vs. 2^{t}CK WRITE Preamble Mode



CWL has special considerations when in the 2tCK WRITE preamble mode. The CWL value selected in MR2[5:3], as seen in table below, requires at least one additional clock when the primary CWL value and 2tCK WRITE preamble mode are used; no additional clocks are required when the alternate CWL value and 2tCK WRITE preamble mode are used.

Table 60. CWL Selection

Seed Bin	CWL - Primary Choice		CWL - Alternate Choice	
	1tCK Preamble	2tCK Preamble	1tCK Preamble	2tCK Preamble
DDR4-1600	9	N/A	11	N/A
DDR4-1866	10	N/A	12	N/A
DDR4-2133	11	N/A	14	N/A
DDR4-2400	12	14	16	16
DDR4-2666	14	16	18	18
DDR4-2933	16	18	20	20
DDR4-3200	16	18	20	20

Note: 1. CWL programmable requirement for MR2[5:3].

When operating in 2tCK WRITE preamble mode, tWTR (command based) and tWR (MR0[11:9]) must be programmed to a value 1 clock greater than the tWTR and tWR setting normally required for the applicable speed bin to be JEDEC compliant; however, DDR4 DRAMs do not require these additional tWTR and tWR clocks. The CAS_n-to-CAS_n command delay to either a different bank group (tCCD_S) or the same bank group (tCCD_L) have minimum timing requirements that must be satisfied between WRITE commands and are stated in the Timing Parameters by Speed Bin tables.

Figure 100. 1tCK vs. 2tCK WRITE Preamble Mode, tCCD = 4

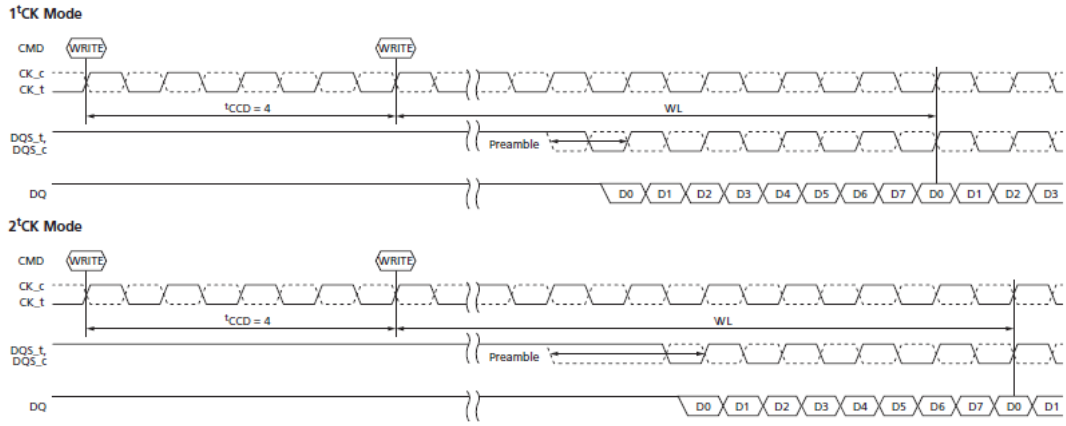
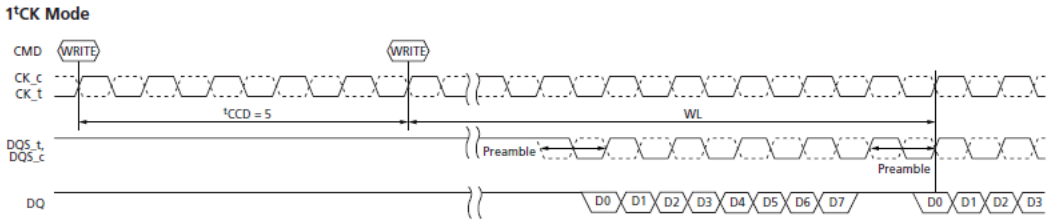
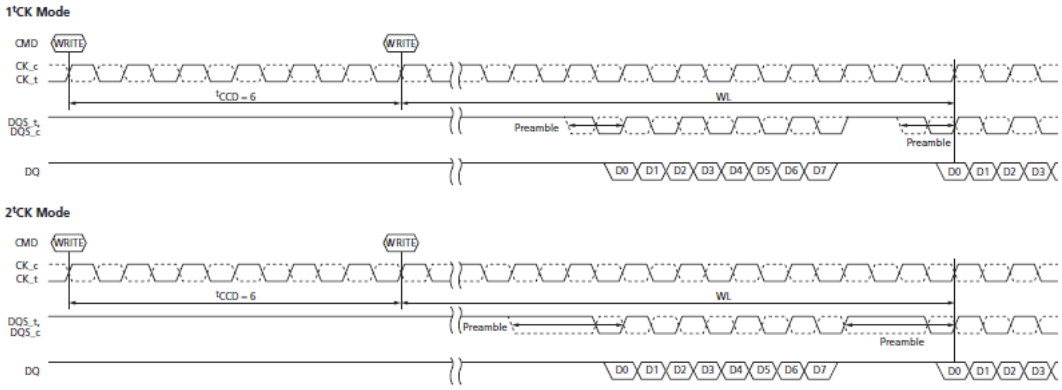


Figure 101. 1tCK vs. 2tCK WRITE Preamble Mode, tCCD = 5



Note: 1. tCCD_S and tCCD_L = 5 tCKs is not allowed when in 2tCK WRITE preamble mode.

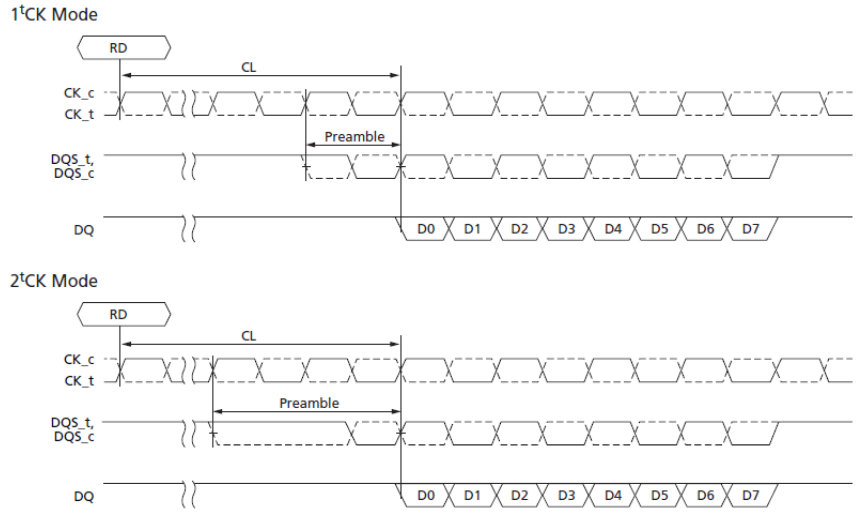
Figure 102. 1tCK vs. 2tCK WRITE Preamble Mode, tCCD = 6



READ Preamble Mode

MR4[11] = 0 selects 1tCK READ preamble mode and MR4[11] = 1 selects 2tCK READ preamble mode. Examples are shown in the following figure.

Figure 103. 1tCK vs. 2tCK WRITE Preamble Mode

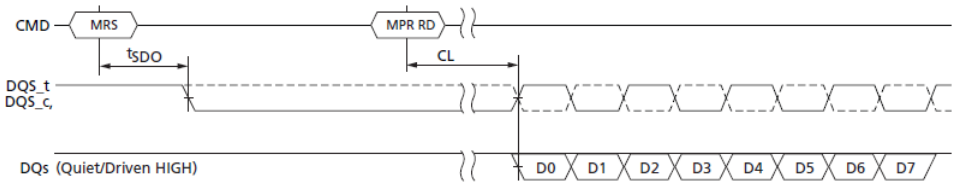


READ Preamble Training

DDR4 supports READ preamble training via MPR reads; that is, READ preamble training is allowed only when the DRAM is in the MPR access mode. The READ preamble training mode can be used by the DRAM controller to train or "read level" its DQS receivers. READ preamble training is entered via an MRS command (MR4[10] = 1 is enabled and MR4[10] = 0 is disabled). After the MRS command is issued to enable READ preamble training, the DRAM DQS signals are driven to a valid level by the time ^{t}SDO is satisfied. During this time, the data bus DQ signals are held quiet, that is, driven HIGH. The DQS_t signal remains driven LOW and the DQS_c signal remains driven HIGH until an MPR Page0 READ command is issued (MPR0 through MPR3 determine which pattern is used), and when CAS latency (CL) has expired, the DQS signals will toggle normally depending on the burst length setting.

To exit READ preamble training mode, an MRS command must be issued, MR4[10] = 0.

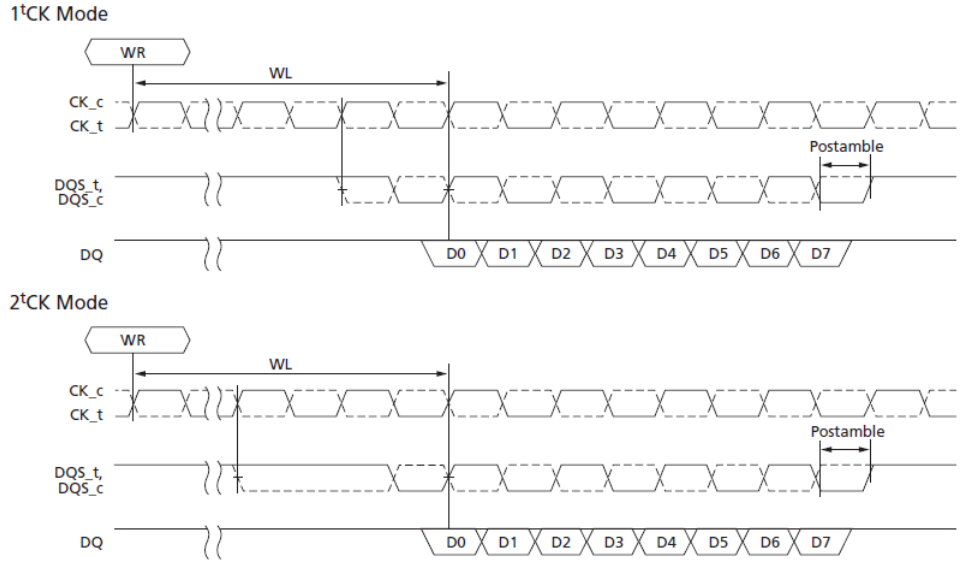
Figure 104. READ Preamble Training



WRITE Postamble

Whether the 1^{t}CK or 2^{t}CK WRITE preamble mode is selected, the WRITE postamble remains the same at $^{1}/_{2}{}^{t}$CK.

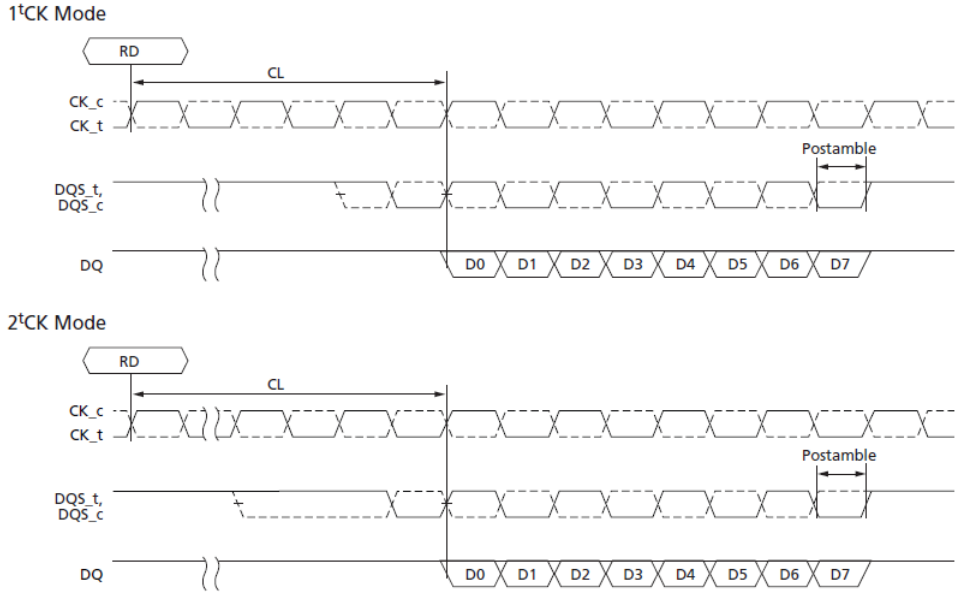
Figure 105. WRITE Postamble



READ Postamble

Whether the 1tCK or 2tCK READ preamble mode is selected, the READ postamble remains the same at $^{1}/_{2}$tCK.

Figure 106. READ Postamble



Bank Access Operation

DDR4 supports bank grouping: x16 DRAMs have two bank groups (BG[0]), and each bank group is comprised of four subbanks. Bank accesses to different banks' groups require less time delay between accesses than bank accesses to within the same bank's group. Bank accesses to different bank groups require tCCD_S (or short) delay between commands while bank accesses within the same bank group require tCCD_L (or long) delay between commands.

Splitting the banks into bank groups with subbanks improved some bank access timings and increased others. However, considering DDR4 did not increase the prefetch from 8*n* to 16*n*, the penalty for staying 8*n* prefetch was significantly mitigated by using bank groups. The table below summarizes the timings affected (values listed as x*n*CK or yns means the larger of the two values).

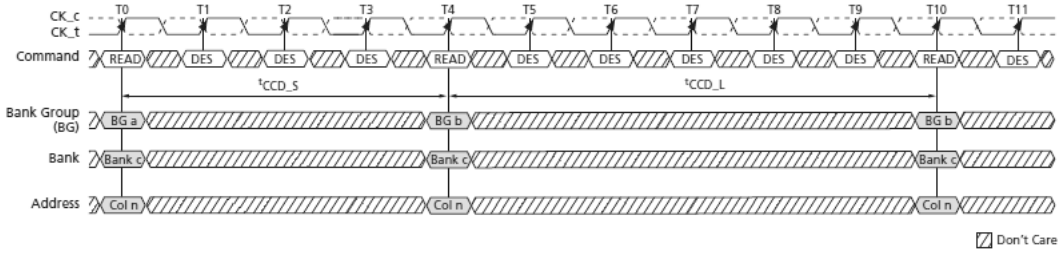
Table 61. DDR4 Bank Group Timing Examples

Parameter	DDR4-1600	DDR4-2133	DDR4-2400
^{t}CCD_S	4*n*CK	4*n*CK	4*n*CK
^{t}CCD_L	4*n*CK or 6.25ns	4*n*CK or 5.355ns	4*n*CK or 5ns
^{t}RRD_S $^{1}/_{2}$K	4*n*CK or 5ns	4*n*CK or 3.7ns	4*n*CK or 3.3ns
^{t}RRD_L $^{1}/_{2}$K	4*n*CK or 6ns	4*n*CK or 5.3ns	4*n*CK or 4.9ns
^{t}RRD_S (1K)	4*n*CK or 5ns	4*n*CK or 3.7ns	4*n*CK or 3.3ns
^{t}RRD_L (1K)	4*n*CK or 6ns	4*n*CK or 5.3ns	4*n*CK or 4.9ns
^{t}RRD_S (2K)	4*n*CK or 6ns	4*n*CK or 5.3ns	4*n*CK or 5.3ns
^{t}RRD_L (2K)	4*n*CK or 7.5ns	4*n*CK or 6.4ns	4*n*CK or 6.4ns
^{t}WTR_S	2*n*CK or 2.5ns	2*n*CK or 2.5ns	2*n*CK or 2.5ns
^{t}WTR_L	4*n*CK or 7.5ns	4*n*CK or 7.5ns	4*n*CK or 7.5ns

Note:

1. Refer to Timing Tables for actual specification values, these values are shown for reference only and are not verified for accuracy.
2. Timings with both *n*CK and ns require both to be satisfied; that is, the larger time of the two cases must be satisfied.

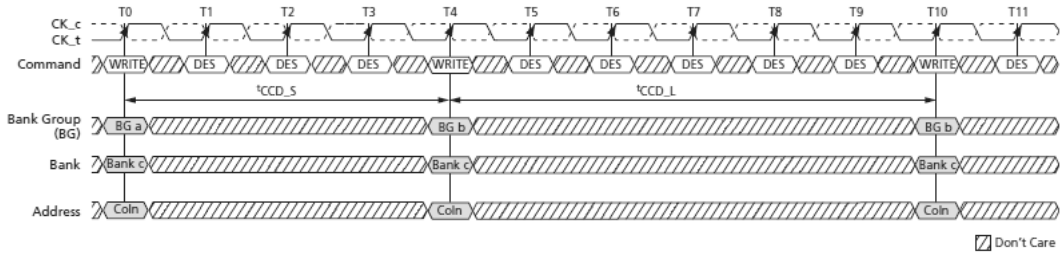
Figure 107. READ Burst ^{t}CCD_S and ^{t}CCD_L Examples



Note:

1. ^{t}CCD_S; CAS_n-to-CAS_n delay (short). Applies to consecutive CAS_n to different bank groups (T0 to T4).
2. ^{t}CCD_L; CAS_n-to-CAS_n delay (long). Applies to consecutive CAS_n to the same bank group (T4 to T10).

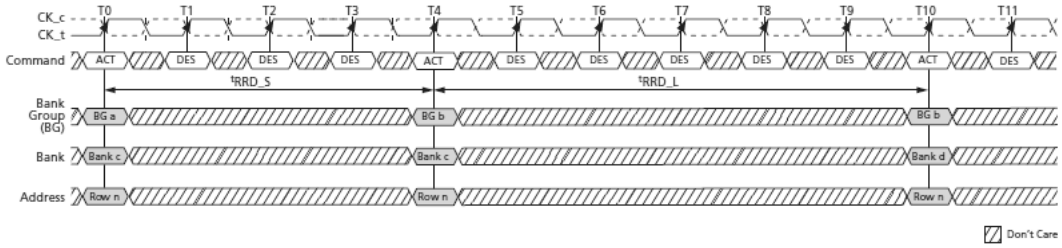
Figure 108. WRITE Burst ^{t}CCD_S and ^{t}CCD_L Examples



Note:

1. ^{t}CCD_S; CAS_n-to-CAS_n delay (short). Applies to consecutive CAS_n to different bank groups (T0 to T4).
2. ^{t}CCD_L; CAS_n-to-CAS_n delay (long). Applies to consecutive CAS_n to the same bank group (T4 to T10)

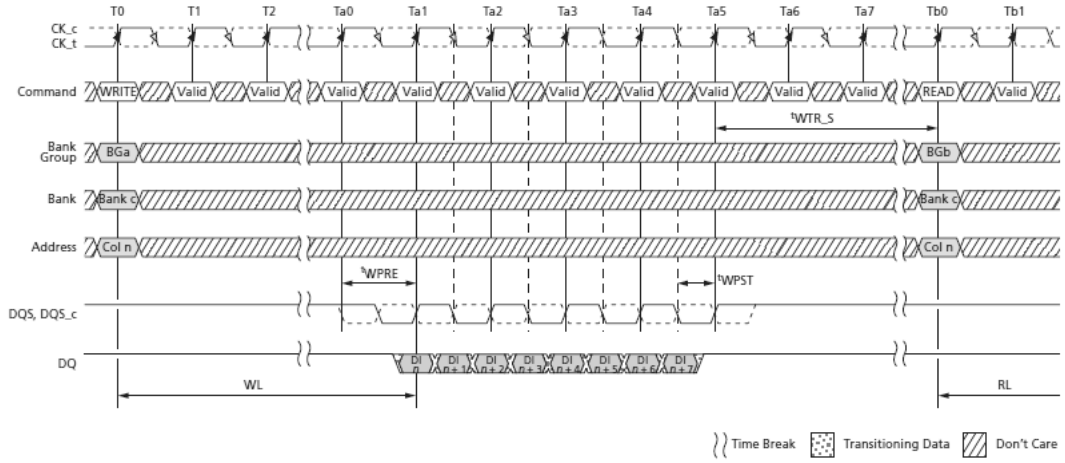
Figure 109. ^{t}RRD Timing



Note:

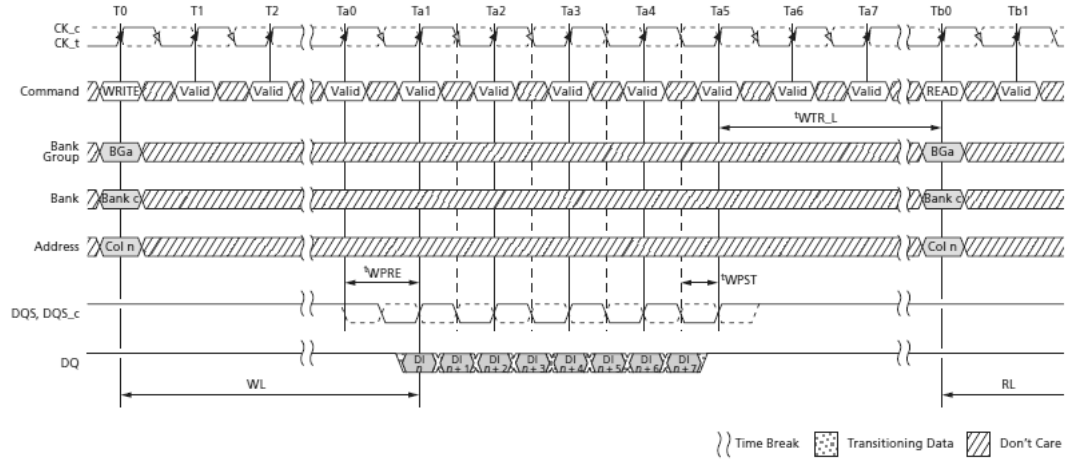
1. ^{t}RRD_S; ACTIVATE-to-ACTIVATE command period (short); applies to consecutive ACTIVATE commands to different bank groups (T0 and T4).
2. ^{t}RRD_L; ACTIVATE-to-ACTIVATE command period (long); applies to consecutive ACTIVATE commands to the different banks in the same bank group (T4 and T10).

Figure 110. ^{t}WTR_S Timing (WRITE-to-READ, Different Bank Group, CRC and DM Disabled)



Note: 1. ^{t}WTR_S: delay from start of internal write transaction to internal READ command to a different bank group.

Figure 111. ^{t}WTR_L Timing (WRITE-to-READ, Same Bank Group, CRC and DM Disabled)



Note: 1. ^{t}WTR_L: delay from start of internal write transaction to internal READ command to the same bank group.

READ Operation

Read Timing Definitions

The read timings shown below are applicable in normal operation mode, that is, when the DLL is enabled and locked.
Note: ^{t}DQSQ = both rising/falling edges of DQS; no ^{t}AC defined.

Rising data strobe edge parameters:

- ^{t}DQSCK (MIN)/(MAX) describes the allowed range for a rising data strobe edge relative to CK.
- ^{t}DQSCK is the actual position of a rising strobe edge relative to CK.
- ^{t}QSH describes the DQS differential output HIGH time.
- ^{t}DQSQ describes the latest valid transition of the associated DQ pins.
- ^{t}QH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- ^{t}QSL describes the DQS differential output LOW time.
- ^{t}DQSQ describes the latest valid transition of the associated DQ pins.
- ^{t}QH describes the earliest invalid transition of the associated DQ pins.

Figure 112. Read Timing Definition

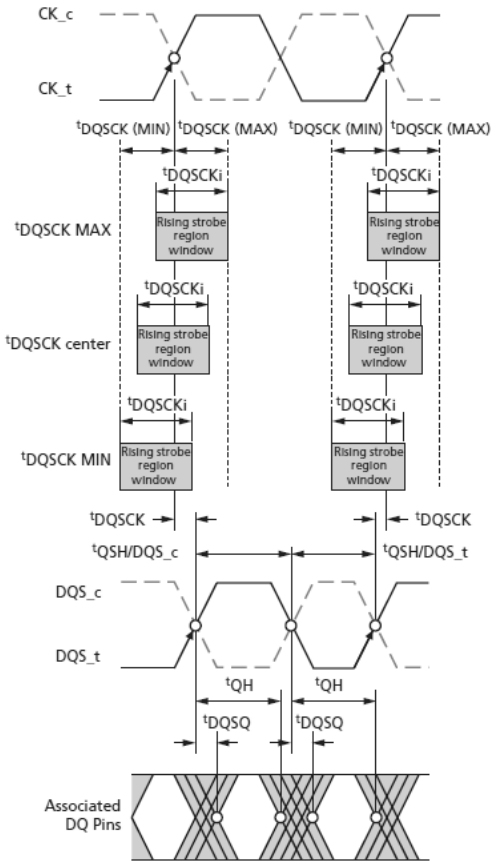


Table 62. Read-to-Write and Write-to-Read Command Intervals

Access Type	Bank Group	Timing Parameters	Note
Read-to-Write, minimum	Same	CL - CWL + RBL/2 + 1^{t}CK + ^{t}WPRE	1, 2
	Different	CL - CWL + RBL/2 + 1^{t}CK + ^{t}WPRE	1, 2
Write-to-Read, minimum	Same	CWL + WBL/2 + ^{t}WTR_L	1, 3
	Different	CWL + WBL/2 + ^{t}WTR_S	1, 3

Note:

1. These timings require extended calibrations times ^{tZ}Qinit and ^{t}ZQCS.
2. RBL: READ burst length associated with READ command, RBL = 8 for fixed 8 and on-the-fly mode 8 and RBL = 4 for fixed BC4 and on-the-fly mode BC4.
3. WBL: WRITE burst length associated with WRITE command, WBL = 8 for fixed 8 and on-the-fly mode 8 or BC4 and WBL = 4 for fixed BC4 only.

Read Timing – Clock-to-Data Strobe Relationship

The clock-to-data strobe relationship shown below is applicable in normal operation mode, that is, when the DLL is enabled and locked.

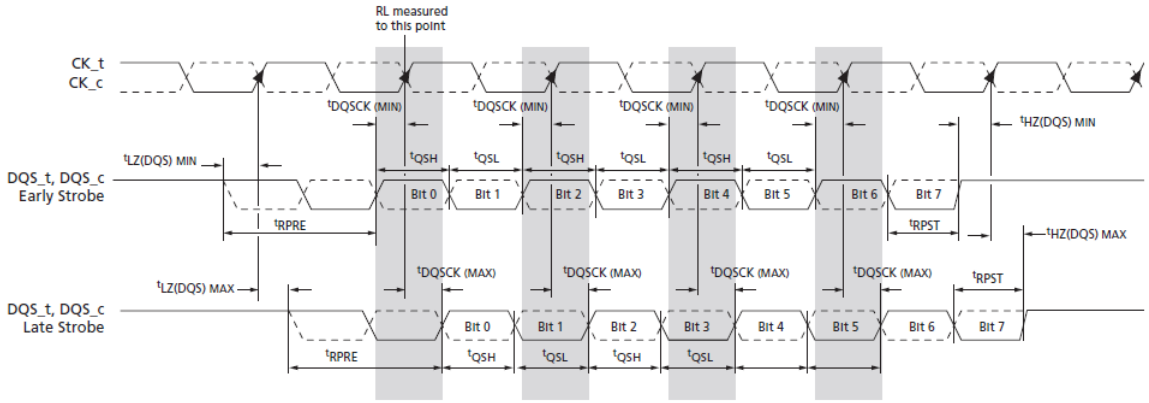
Rising data strobe edge parameters:

- ^{t}DQSCK (MIN)/(MAX) describes the allowed range for a rising data strobe edge relative to CK.
- ^{t}DQSCK is the actual position of a rising strobe edge relative to CK.
- ^{t}QSH describes the data strobe high pulse width.
- ^{t}HZ(DQS) DQS strobe going to high, nondrive level (shown in the postamble section of the figure below).

Falling data strobe edge parameters:

- ^{t}QSL describes the data strobe low pulse width.
- ^{t}LZ(DQS) DQS strobe going to low, initial drive level (shown in the preamble section of the figure below).

Figure 113. Clock-to-Data Strobe Relationship



Note:

1. Within a burst, the rising strobe edge will vary within ^{t}DQSCKi while at the same voltage and temperature. However, when the device, voltage, and temperature variations are incorporated, the rising strobe edge variance window can shift between ^{t}DQSCK (MIN) and ^{t}DQSCK (MAX). A timing of this window's right edge (latest) from rising CK_t, CK_c is limited by a device's actual ^{t}DQSCK (MAX). A timing of this window's left inside edge (earliest) from rising CK_t, CK_c is limited by ^{t}DQSCK (MIN).
2. Notwithstanding Note 1, a rising strobe edge with tDQSCK (MAX) at T(n) can not be immediately followed by a rising strobe edge with tDQSCK (MIN) at T(n + 1) because other timing relationships (^{t}QSH, ^{t}QSL) exist: if ^{t}DQSCK(n + 1) < 0: ^{t}DQSCK(n) < 1.0 tCK - (^{t}QSH (MIN) + ^{t}QSL (MIN)) - |^{t}DQSCK(n + 1) |.
3. The DQS_t, DQS_c differential output HIGH time is defined by tQSH, and the DQS_t, DQS_c differential output LOW time is defined by ^{t}QSL.
4. ^{t}LZ(DQS) MIN and ^{t}HZ(DQS) MIN are not tied to ^{t}DQSCK (MIN) (early strobe case), and ^{t}LZ(DQS) MAX and ^{t}HZ(DQS) MAX are not tied to ^{t}DQSCK (MAX) (late strobe case).
5. The minimum pulse width of READ preamble is defined by ^{t}RPRE (MIN).
6. The maximum READ postamble is bound by tDQSCK (MIN) plus ^{t}QSH (MIN) on the left side and ^{t}HZDSQ (MAX) on the right side.
7. The minimum pulse width of READ postamble is defined by ^{t}RPST (MIN).
8. The maximum READ preamble is bound by ^{t}LZDQS (MIN) on the left side and ^{t}DQSCK (MAX) on the right side.

Read Timing – Data Strobe-to-Data Relationship

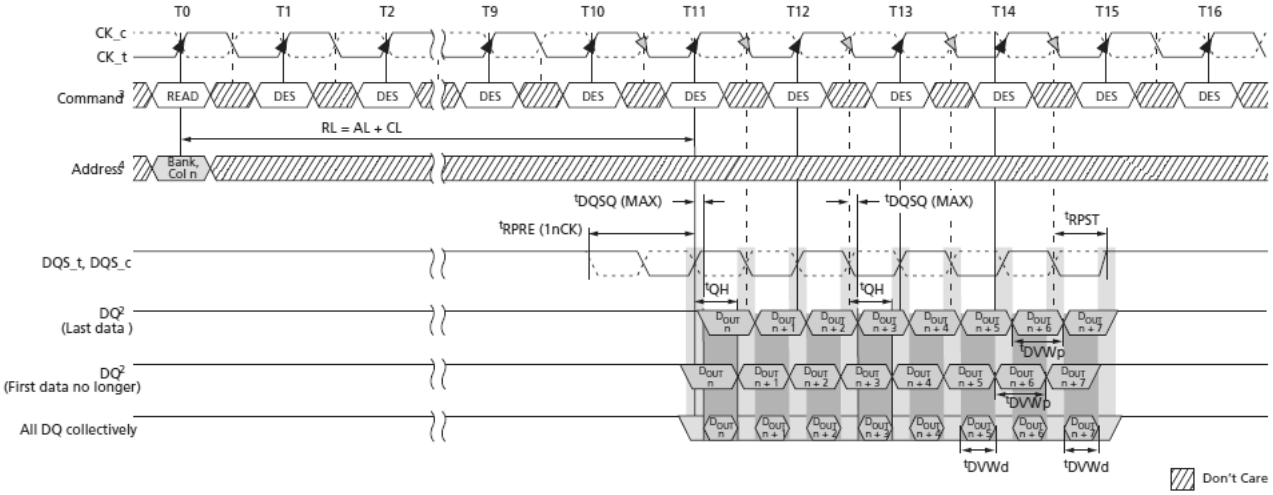
The data strobe-to-data relationship is shown below and is applied when the DLL is enabled and locked.
Note: ^{t}DQSQ: both rising/falling edges of DQS; no ^{t}AC defined.

Rising data strobe edge parameters:
- ^{t}DQSQ describes the latest valid transition of the associated DQ pins.
- ^{t}QH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:
- ^{t}DQSQ describes the latest valid transition of the associated DQ pins.
- ^{t}QH describes the earliest invalid transition of the associated DQ pins.

Data valid window parameters:
- ^{t}DVWd is the Data Valid Window per device per UI and is derived from [^{t}QH - ^{t}DQSQ] of each UI on a given DRAM
- ^{t}DVWp is the Data Valid Window per pin per UI and is derived [^{t}QH - ^{t}DQSQ] of each UI on a pin of a given DRAM

Figure 114. Data Strobe-to-Data Relationship



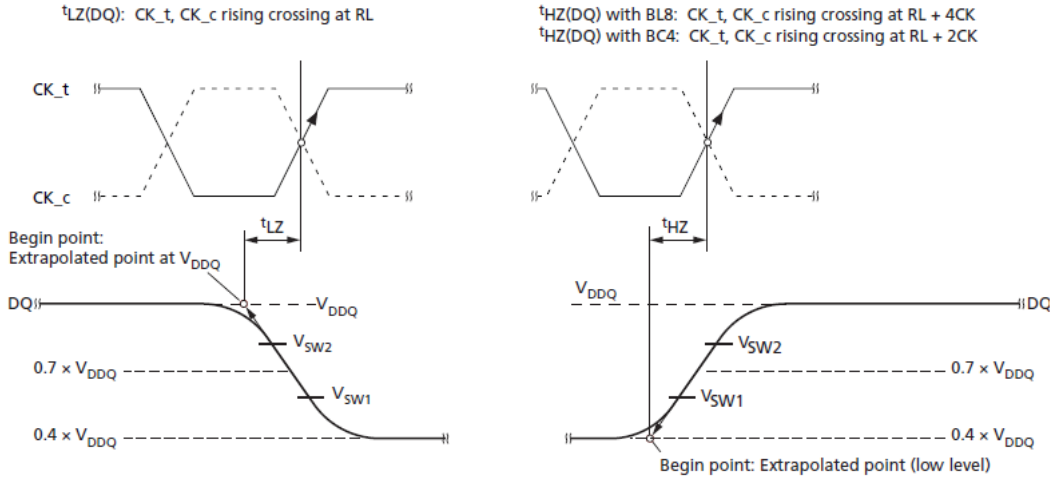
Note:

1. BL = 8, RL = 11 (AL = 0, CL = 1), Premable = 1tCK.
2. DOUT *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0.
5. Output timings are referenced to V_{DDQ}, and DLL on for locking.
6. ^{t}DQSQ defines the skew between DQS to data and does not define DQS to clock.
7. Early data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

^{t}LZ(DQS), ^{t}LZ(DQ), ^{t}HZ(DQS), ^{t}HZ(DQ) Calculations

^{t}HZ and ^{t}LZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving ^{t}HZ(DQS) and ^{t}HZ(DQ), or begins driving ^{t}LZ(DQS), ^{t}LZ(DQ). Figure of ^{t}LZ(DQ) and ^{t}HZ(DQ) method for calculating transitions and begin points shows a method to calculate the point when the device is no longer driving ^{t}HZ(DQS) and ^{t}HZ(DQ), or begins driving ^{t}LZ(DQS), ^{t}LZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters ^{t}LZ(DQS), ^{t}LZ(DQ), ^{t}HZ(DQS), and ^{t}HZ(DQ) are defined as single ended parameters.

Figure 115. ^{t}LZ(DQ) and ^{t}HZ(DQ) method for calculating transitions and begin points

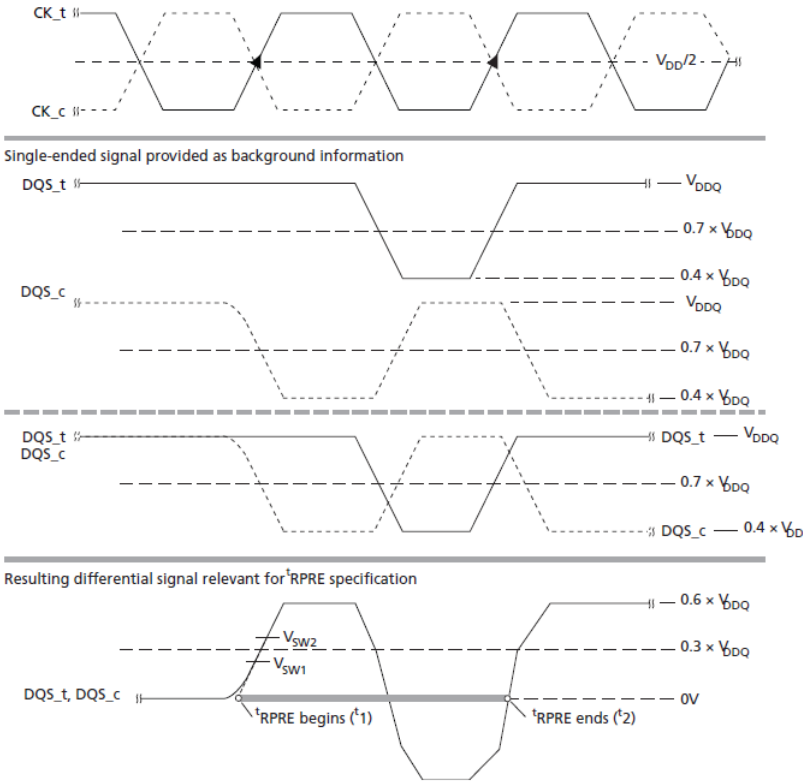


Note:

1. V_{sw1} = (0.70 - 0.04) x V_{DDQ} for both ^{t}LZ and ^{t}HZ.
2. V_{sw2} = (0.70 + 0.04) x V_{DDQ} for both ^{t}LZ and ^{t}HZ.
3. Extrapolated point (low level) = V_{DDQ}/(50 + 34) x 34 = 0.4 x V_{DDQ}
   Driver impedance = R_{ZQ}/7 = 34Ω
   V_{TT} test load = 50Ω to V_{DDQ}.

tRPRE Calculation

Figure 116. tRPRE Method for Calculating Transitions and Endpoints

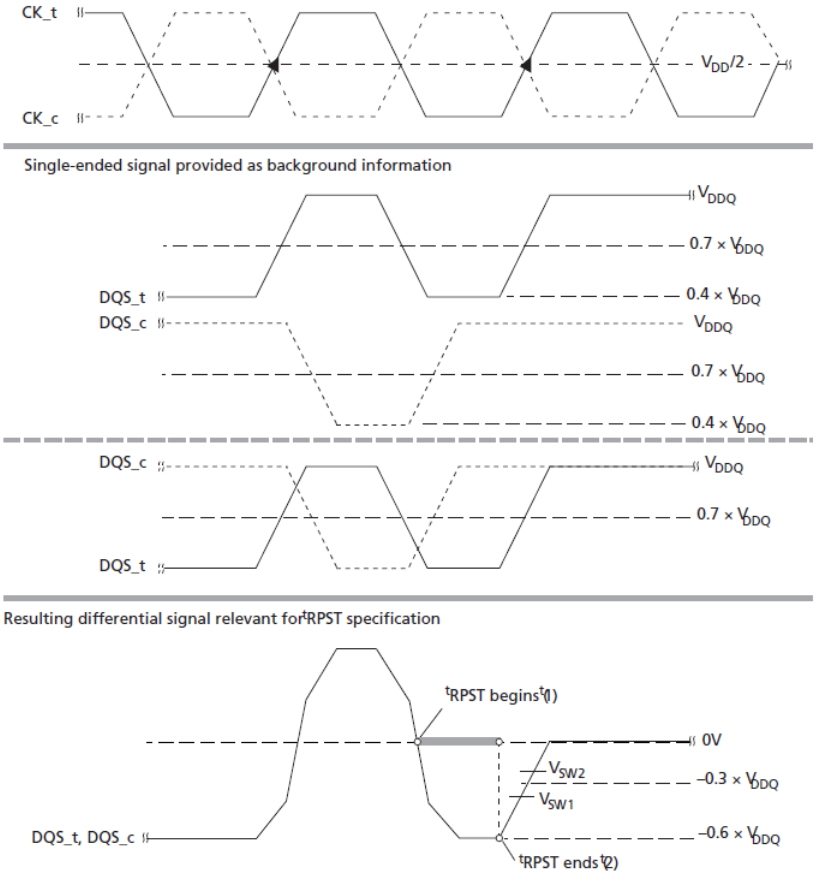


Note:

1. V_{sw1} = (0.3 - 0.04) x V_{DDQ}.
2. V_{sw2} = (0.30 + 0.04) x V_{DDQ}.
3. DQS_t and DQS_c low level = V_{DDQ}/(50 + 34) x 34 = 0.4 x V_{DDQ}
   Driver impedance = R_{ZQ}/7 = 34Ω
   V_{TT} test load = 50Ω to V_{DDQ}.

tRPST Calculation

Figure 117. tRPST Method for Calculating Transitions and Endpoints



Note:

1. V_{SW1} = (-0.3 - 0.04) x V_{DDQ}.
2. V_{SW2} = (-0.30 + 0.04) x V_{DDQ}.
3. DQS_t and DQS_c low level = V_{DDQ}/(50 + 34) x 34 = 0.4 x V_{DDQ}
   Driver impedance = R_{ZQ}/7 = 34Ω
   V_{TT} test load = 50Ω to V_{DDQ}.

READ Burst Operation

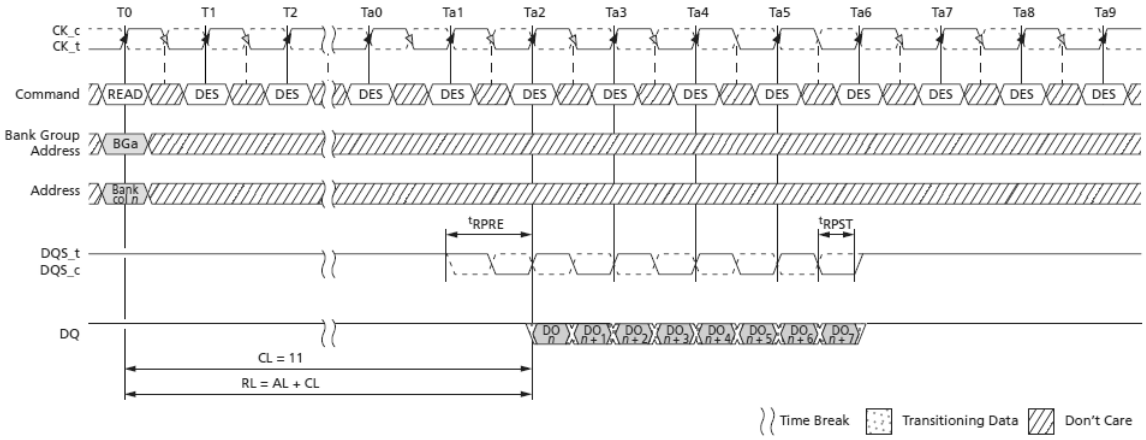
DDR4 READ commands support bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF when OTF is enabled:

- A12 = 0, BC4 (BC4 = burst chop)
- A12 = 1, BL8

READ commands can issue precharge automatically with a READ with auto precharge command (RDA), and is enabled by A10 HIGH:

- READ command with A10 = 0 (RD) performs standard read, bank remains active after READ burst.
- READ command with A10 = 1 (RDA) performs read with auto precharge, bank goes in to precharge after READ burst.

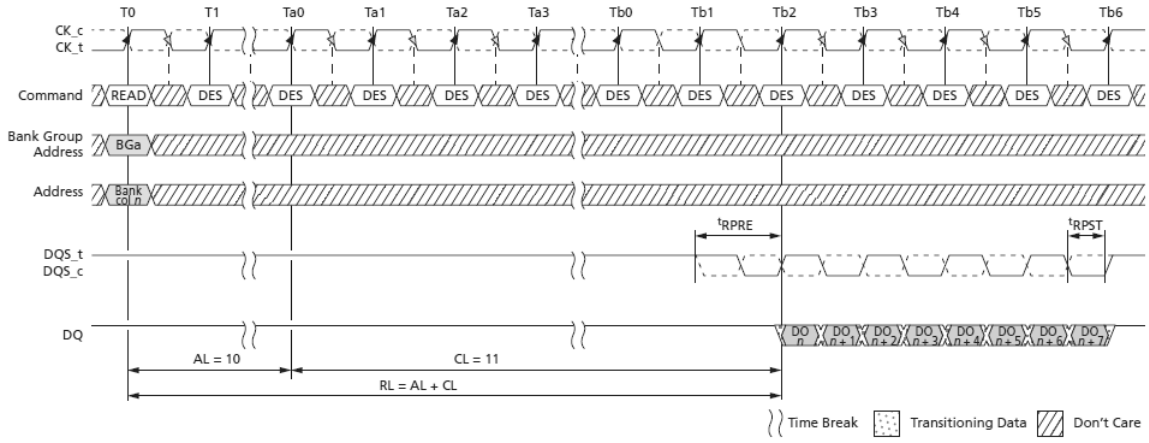
Figure 118. READ Burst Operation, RL = 11 (AL = 0, CL = 11, BL8)



Note:

1. BL8, RL = 0, AL = 0, CL = 11, Preamble = 1^{t}CK.
2. DO *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 119. READ Burst Operation, RL = 21 (AL = 10, CL = 11, BL8)

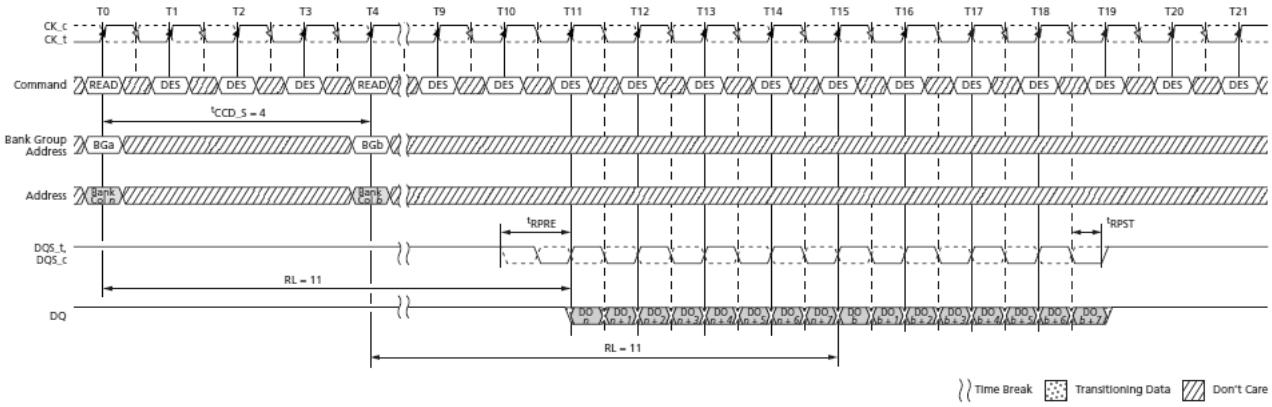


Note:

1. BL8, RL = 21, AL = (CL-1), CL = 11, Preamble = 1^{t}CK.
2. DO *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

READ Operation Followed by Another READ Operation

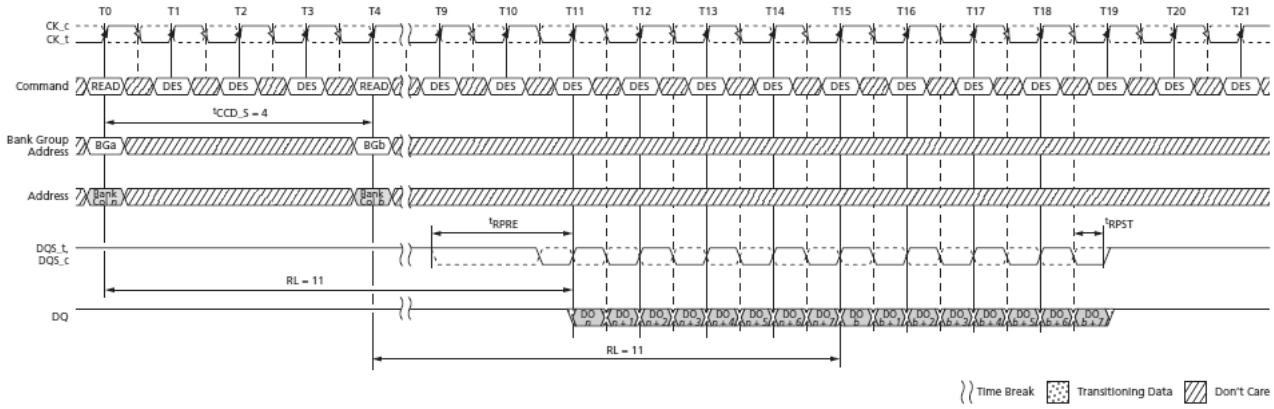
Figure 120. Consecutive READ (BL8) with 1^{t}CK Preamble in Different Bank Group



Note:

1. BL8, AL = 0, CL = 11, Preamble = 1^{t}CK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

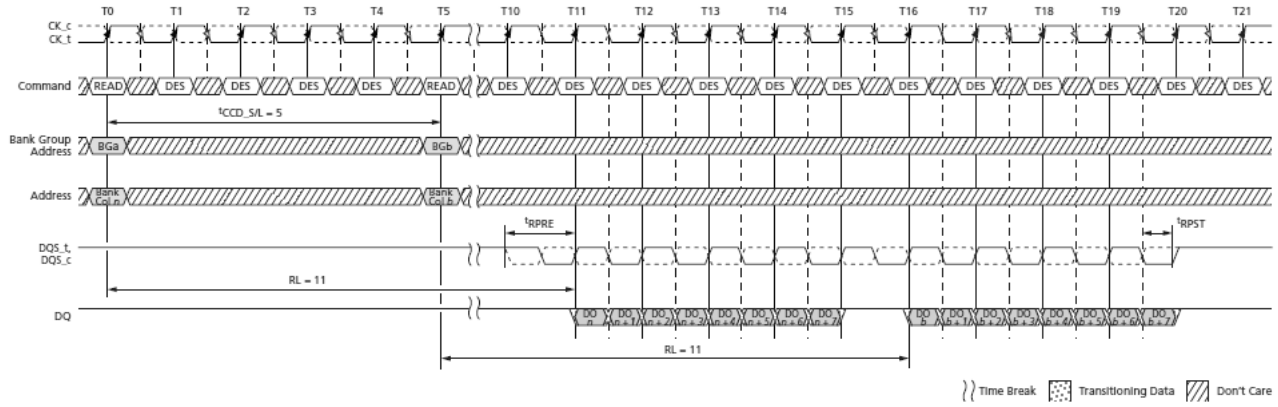
Figure 121. Consecutive READ (BL8) with 2tCK Preamble in Different Bank Group



Note:

1. BL8, AL = 0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

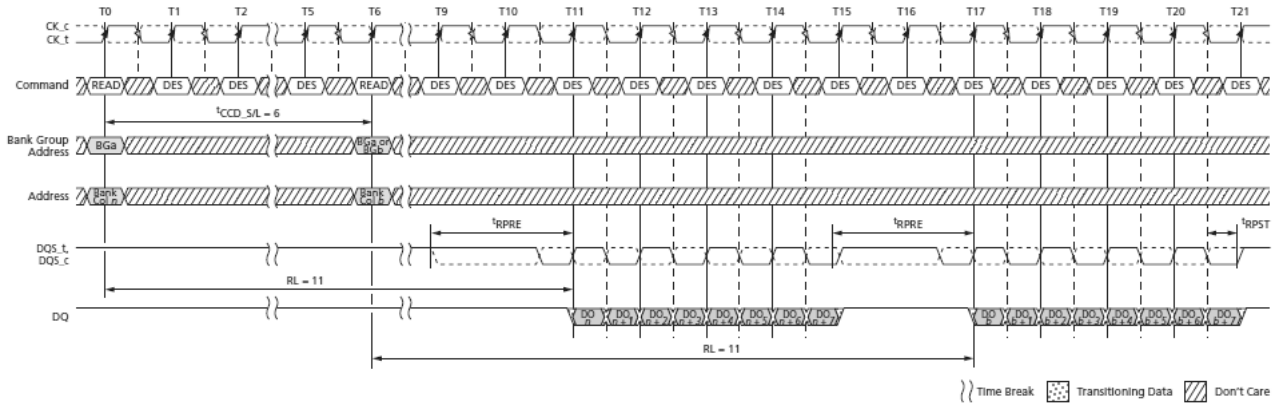
Figure 122. Nonconsecutive READ (BL8) with 1tCK Preamble in Same or Different Bank Group



Note:

1. BL8, AL = 0, CL = 11, Preamble = 1tCK, tCCD_S/L = 5.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T5.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

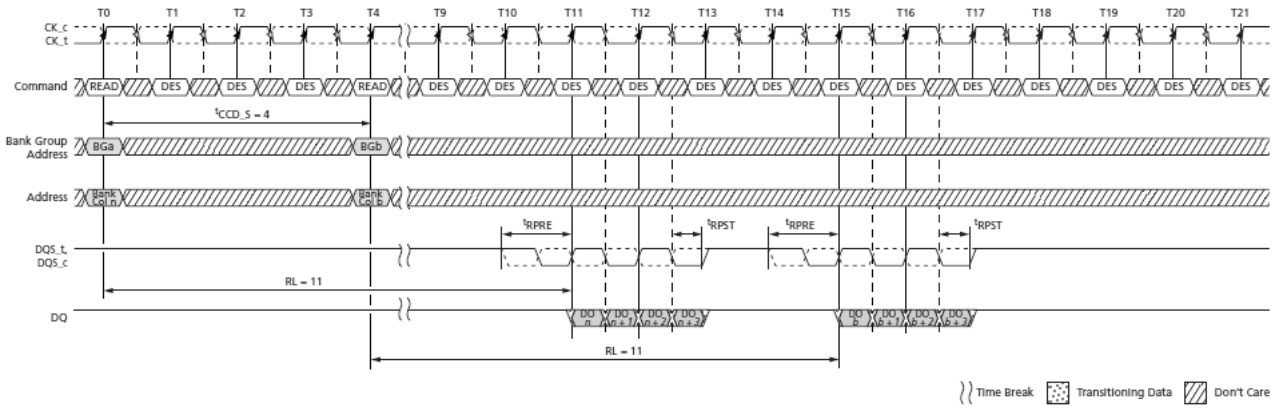
Figure 123. Nonconsecutive READ (BL8) with 2tCK Preamble in Same or Different Bank Group



Note:

1. BL8, AL = 0, CL = 11, Preamble = 2tCK, tCCD_S/L = 6.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T6.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.
6. 6 tCCD_S/L = 5 isn't allowed in 2tCK preamble mode.

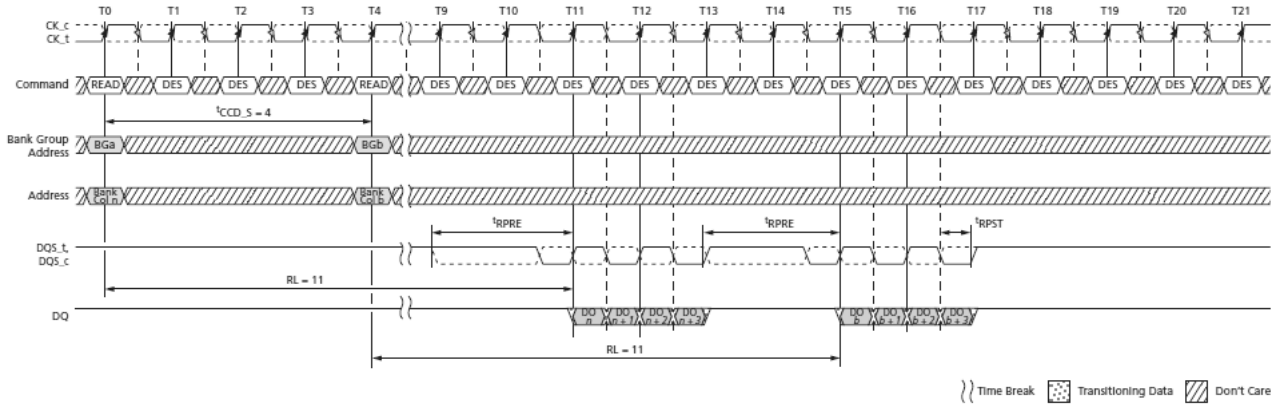
Figure 124. READ (BC4) to READ (BC4) with 1tCK Preamble in Different Bank Group



Note:

1. BL8, AL = 0, CL = 11, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

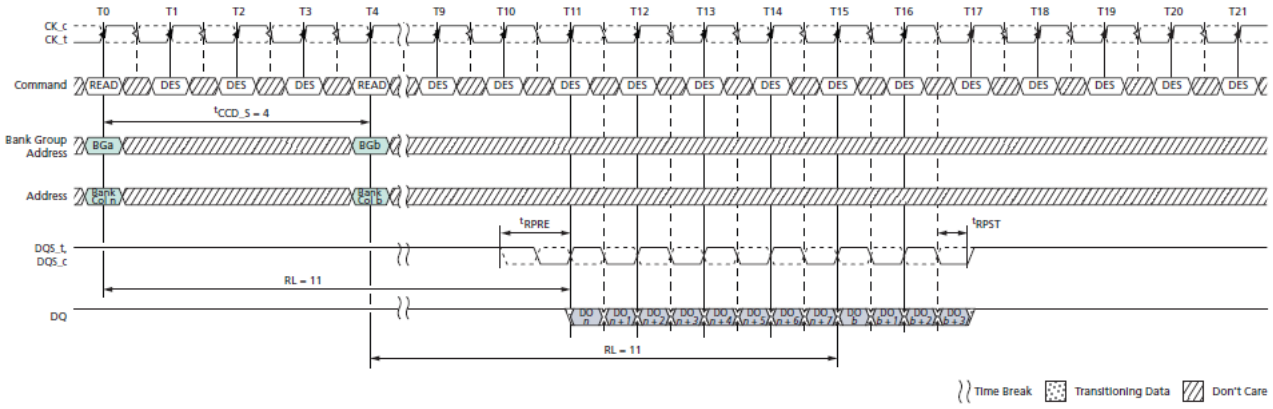
Figure 125. READ (BC4) to READ (BC4) with 2tCK Preamble in Different Bank Group



Note:

1. BL8, AL = 0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

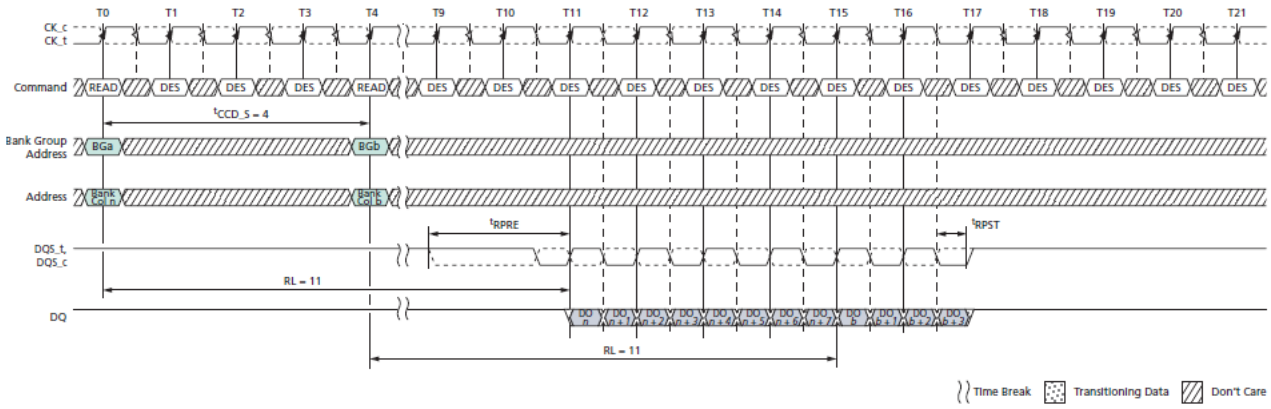
Figure 126. READ (BL8) to READ (BC4) OTF with 1tCK Preamble in Different Bank Group



Note:

1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

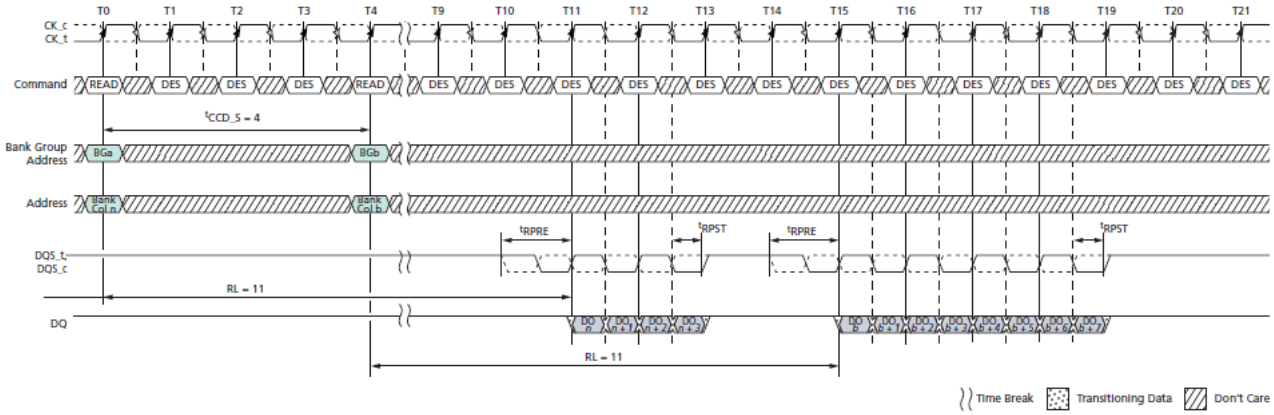
Figure 127. READ (BL8) to READ (BC4) OTF with 2tCK Preamble in Different Bank Group



Note:

1. BL = 8, AL =0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

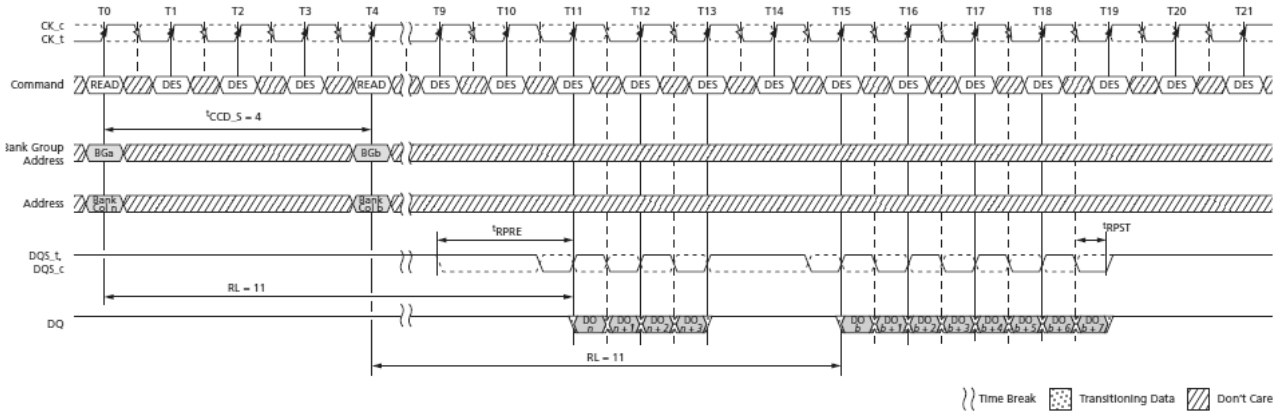
Figure 128. READ (BC4) to READ (BL8) OTF with 1tCK Preamble in Different Bank Group



Note:

1. BL = 8, AL =0, CL = 11, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 129. READ (BC4) to READ (BL8) OTF with 2tCK Preamble in Different Bank Group

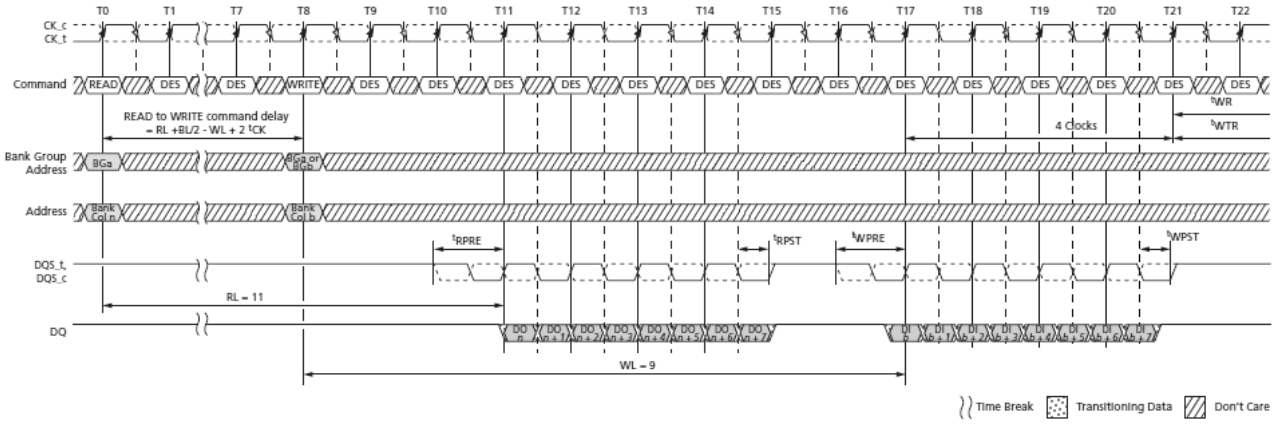


Note:

1. BL = 8, AL = 0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

READ Operation Followed by WRITE Operation

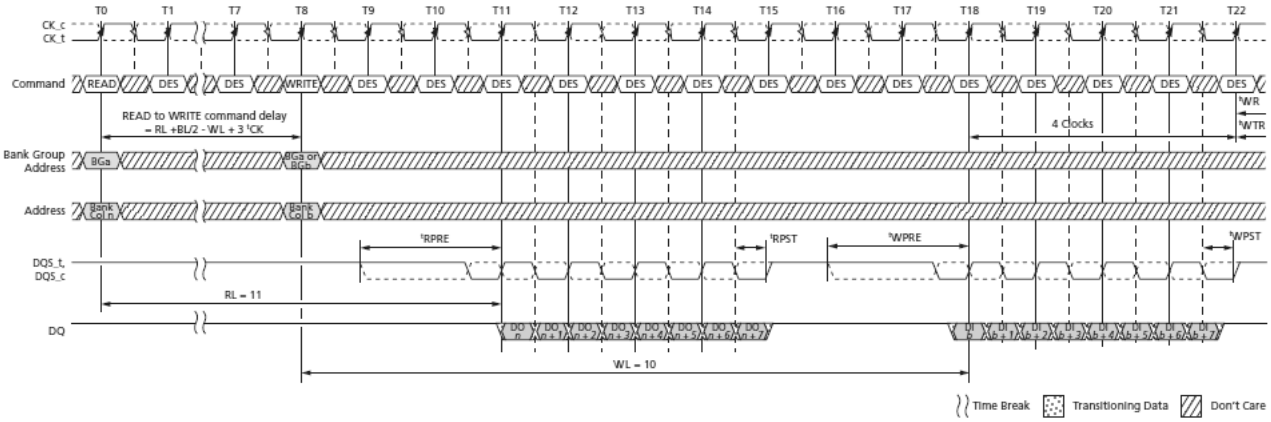
Figure 130. READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



Note:

1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE commands at T8.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

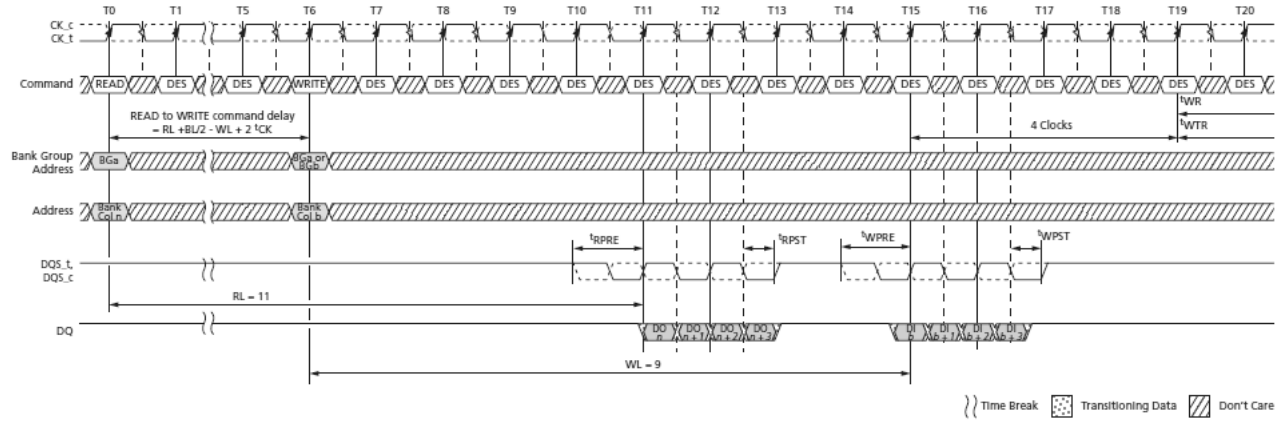
Figure 131. READ (BL8) to WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



Note:

1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 2tCK, WL = 10 (CWL = 9+1 [see Note 5], AL = 0), WRITE preamble = 2tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
1. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE commands at T8.
4. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

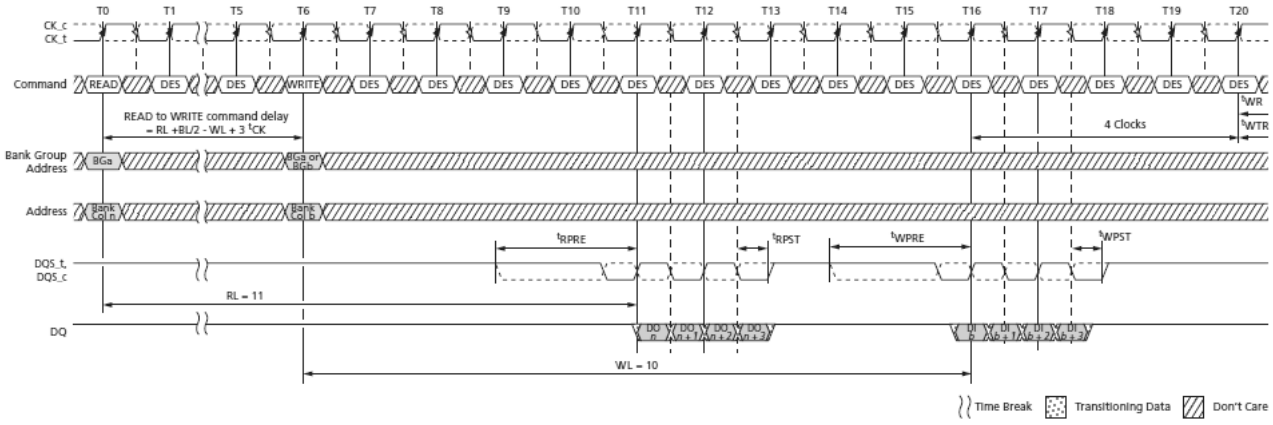
Figure 132. READ (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



Note:

1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 (OTF) setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and WRITE commands at T6.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

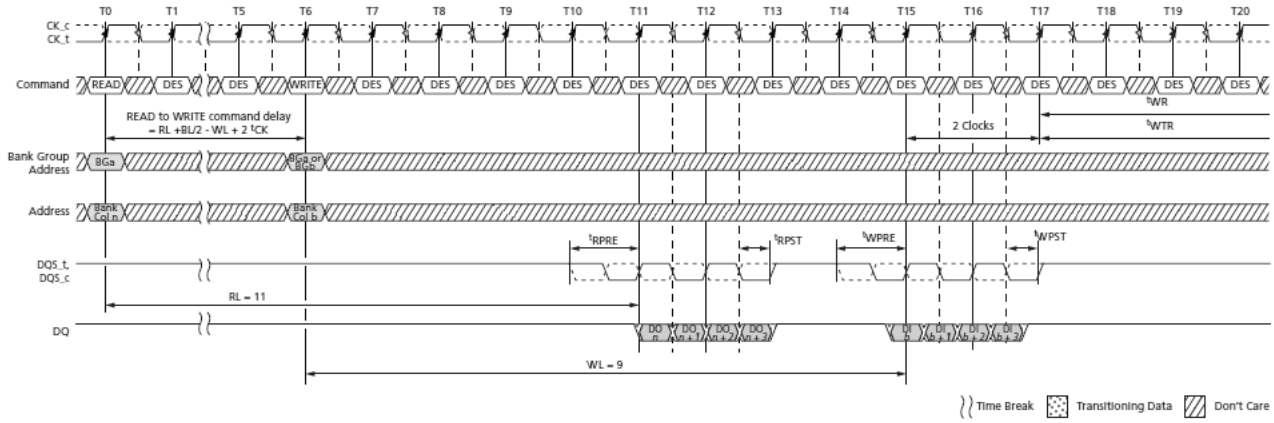
Figure 133. READ (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



Note:

1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 2tCK, WL = 10 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 (OTF) setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and WRITE commands at T6.
5. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

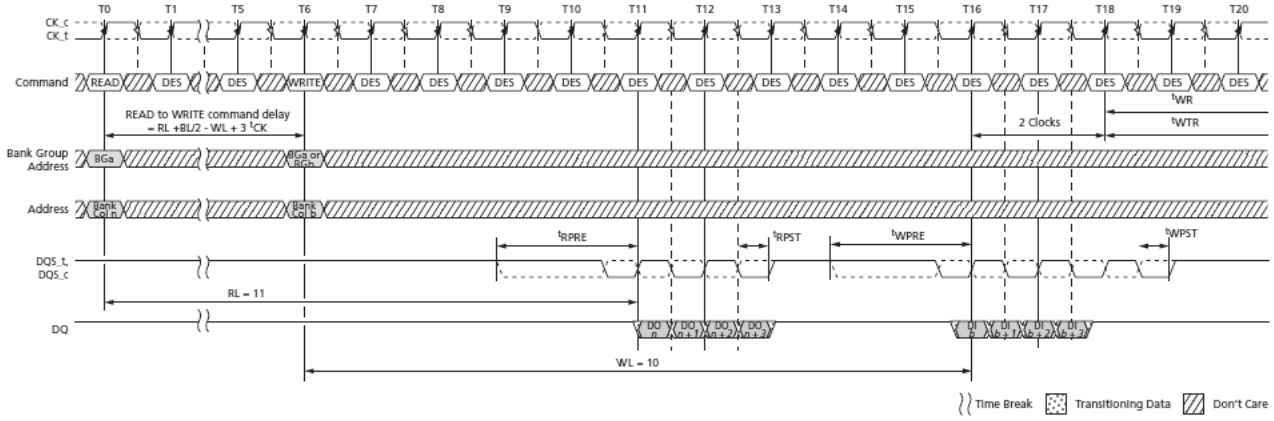
Figure 134. READ (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Same or Different Bank Group



Note:

1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK
2. DO n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(Fixed) setting activated by MR0[1:0] = 01.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

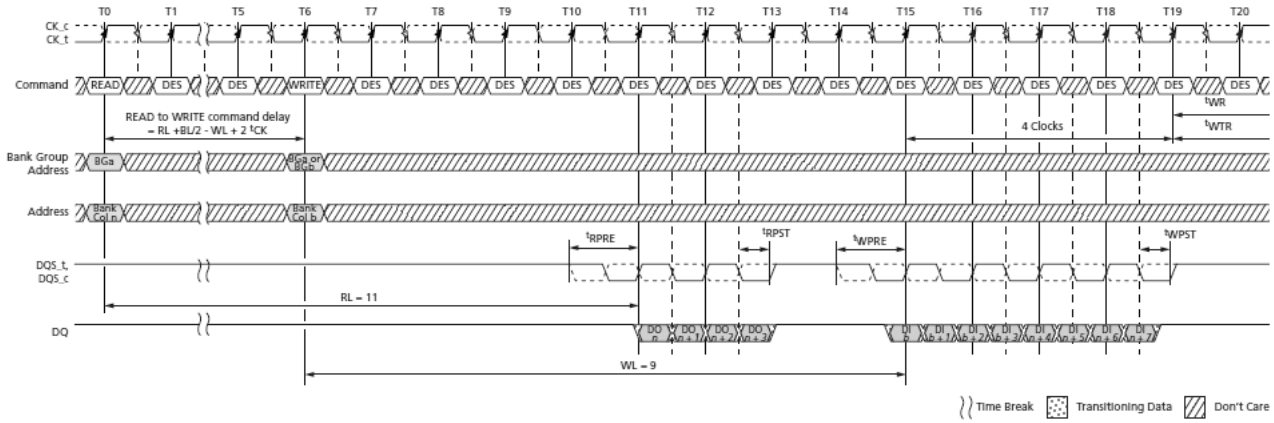
Figure 135. READ (BC4) Fixed to WRITE (BC4) Fixed with 2tCK Preamble in Same or Different Bank Group



Note:

1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1*5, AL = 0), Write Preamble = 2tCK
2. DO n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(Fixed) setting activated by MR0[1:0] = 10.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

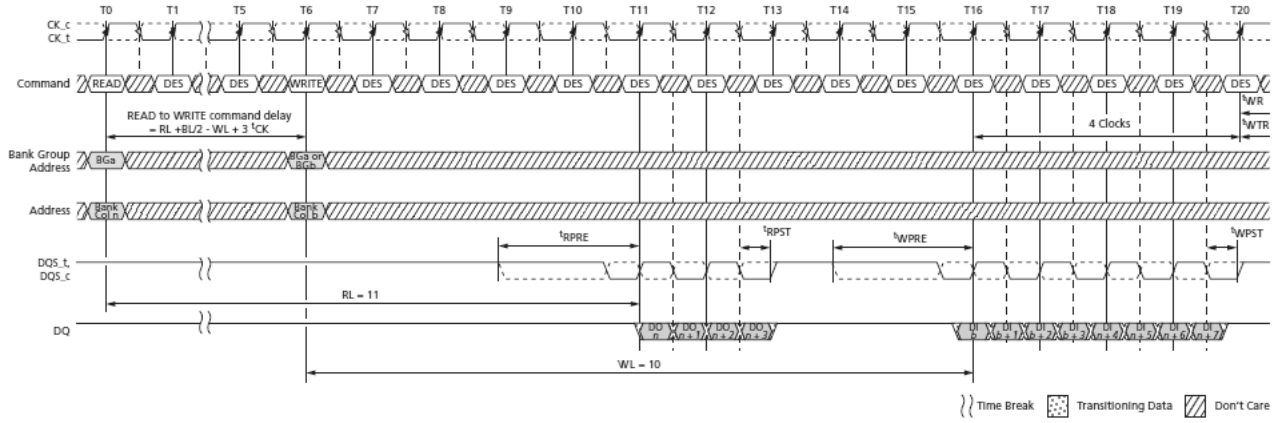
Figure 136. READ (BC4) to WRITE (BL8) OTF with 1tCK Preamble in Same or Different Bank Group



Note:

1. BC = 4, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0 = 01] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[1:0 = 01] and A12 = 1 during WRITE command at T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

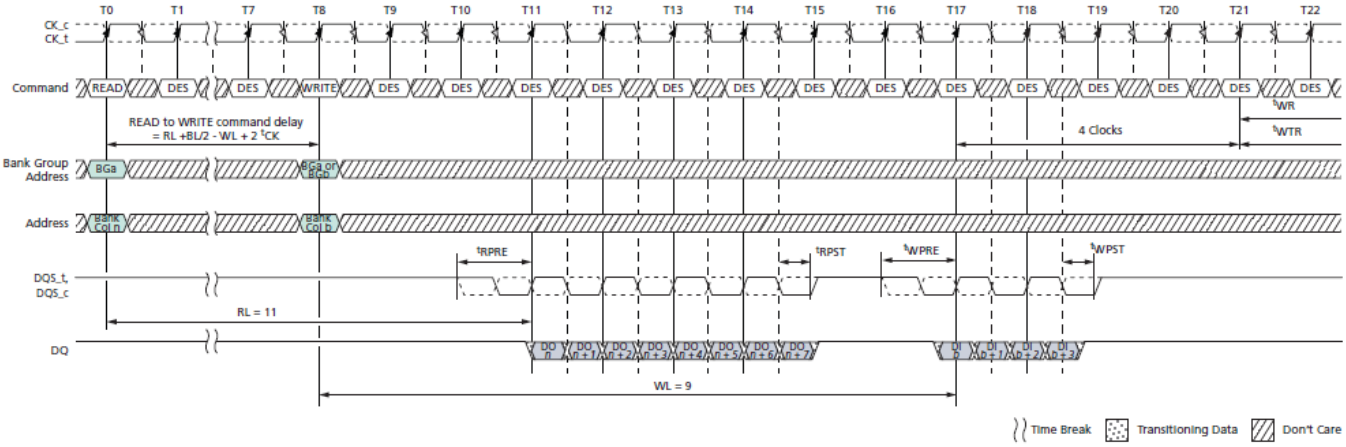
Figure 137. READ (BC4) to WRITE (BL8) OTF with 2tCK Preamble in Same or Different Bank Group



Note:

1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1*5, AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0 = 01] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[1:0 = 01] and A12 = 1 during WRITE command at T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

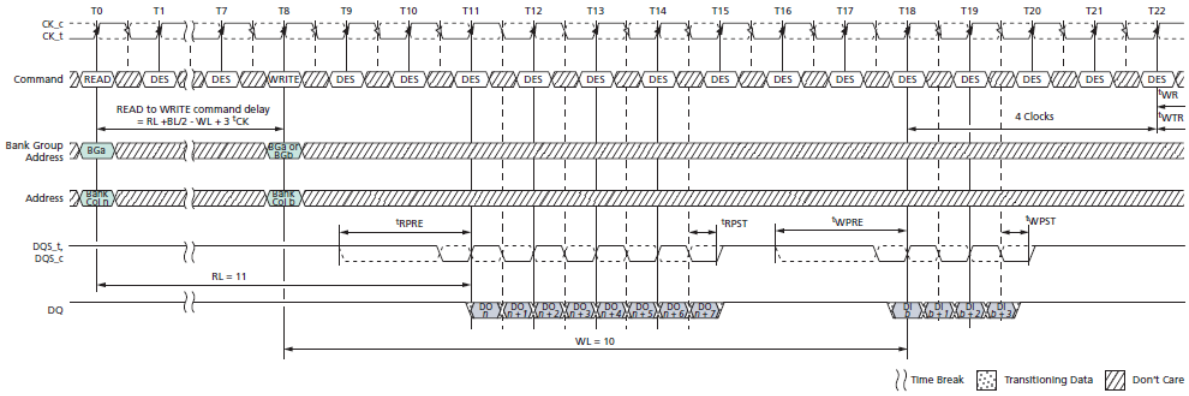
Figure 138. READ (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



Note:

1. BL = 8, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0 = 01] and A12 = 1 during READ command at T0.
   BC4 setting activated by MR0[1:0 = 01] and A12 = 0 during WRITE command at T8.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 139. READ (BL8) to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



Note:

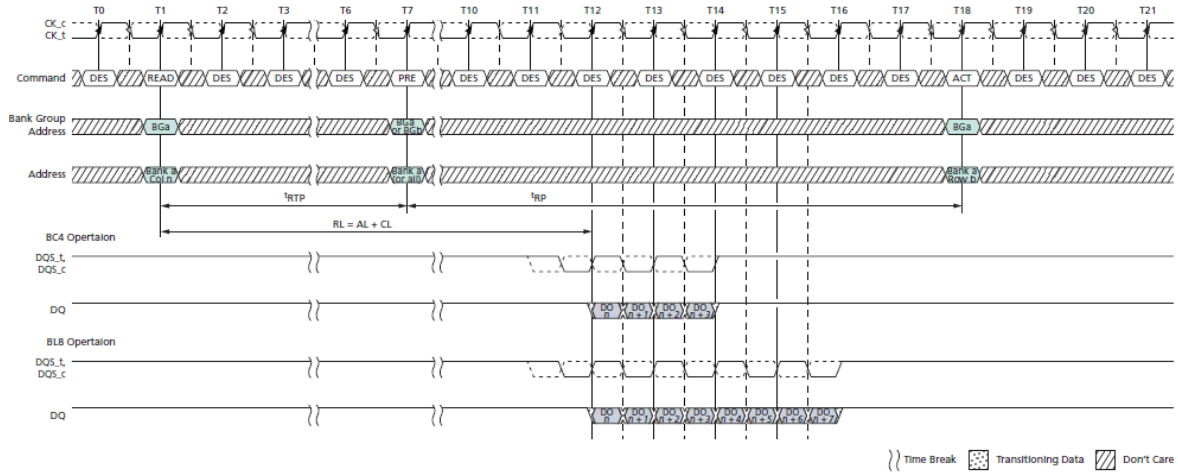
1. BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1*5, AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0 = 01] and A12 = 1 during READ command at T0.
   BC4 setting activated by MR0[1:0 = 01] and A12 = 0 during WRITE command at T8.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ Operation Followed by PRECHARGE Operation

The minimum external READ command to PRECHARGE command spacing to the same bank is equal to AL + tRTP with tRTP being the internal READ command to PRECHARGE command delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the internal READ command to PRECHARGE command delay is given by tRTP (MIN) = MAX (4 x *n*CK, 7.5ns). A new bank ACTIVATE command may be issued to the same bank if the following two conditions are satisfied simultaneously:

- The minimum RAS precharge time (tRP [MIN]) has been satisfied from the clock at which the precharge begins.
- The minimum RAS cycle time (tRC [MIN]) from the previous bank activation has been satisfied.

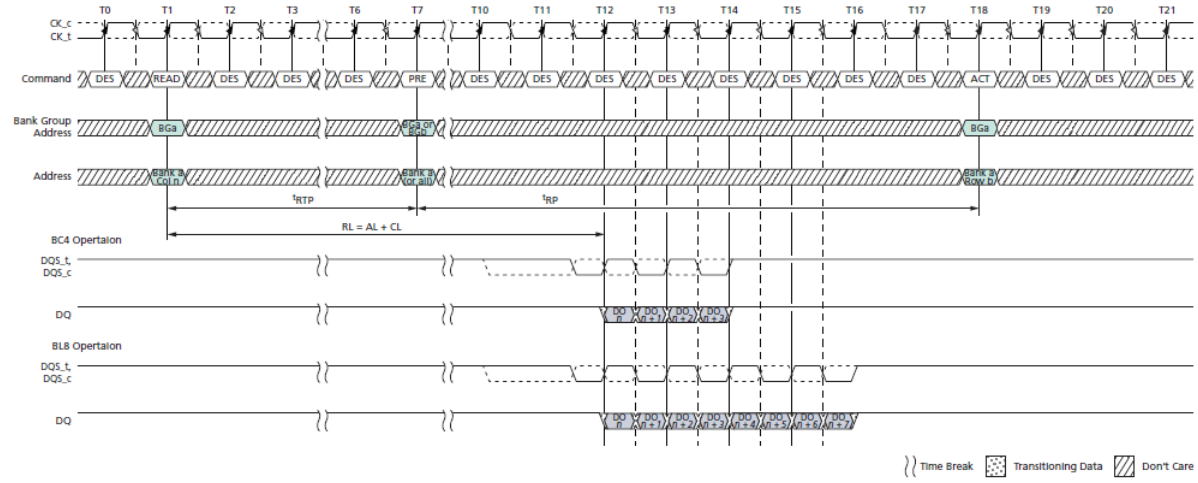
Figure 140. READ to PRECHARGE with 1tCK Preamble



Note:

1. BL = 8, RL = 11 (CL = 11, AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DO n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time T7) and that tRC. MIN is satisfied at the next Active command time T18).
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

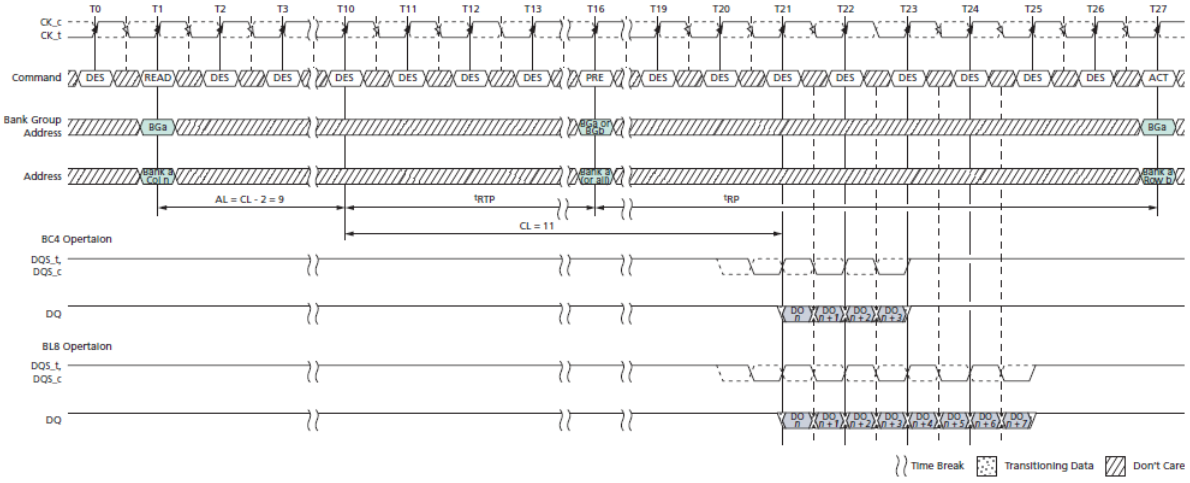
Figure 141. READ to PRECHARGE with 2tCK Preamble



Note:

1. BL = 8, RL = 11 (CL = 11, AL = 0), Preamble = 2tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

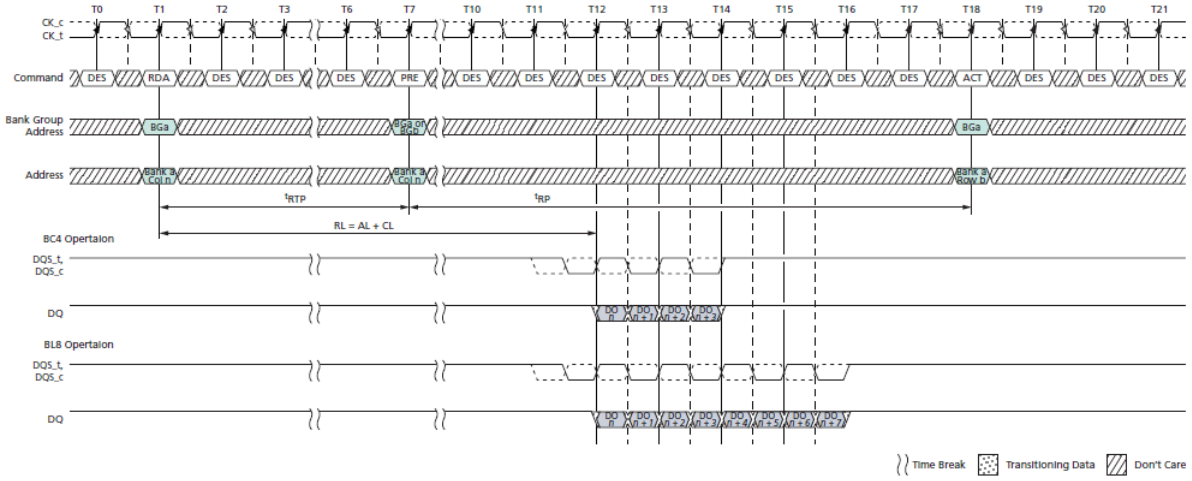
Figure 142. READ to PRECHARGE with Additive Latency and 1tCK Preamble



Note:

1. BL = 8, RL = 20 (CL = 11, AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time(T16) and that tRC. MIN is satisfied at the next Active command time(T27).
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

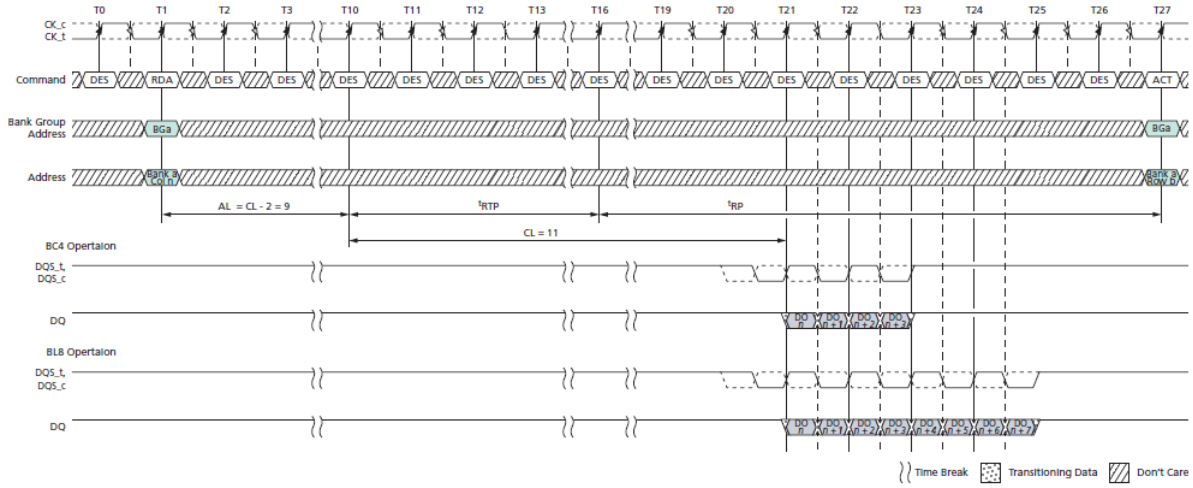
Figure 143. READ with Auto Precharge and 1tCK Preamble



Note:

1. BL = 8, RL = 11 (CL = 11, AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRTP = 6 setting activated by MR0[A11:9 = 001]
5. The example assumes tRC. MIN is satisfied at the next Active command time(T18).
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 144. READ with Auto Precharge, Additive Latency and 1tCK Preamble

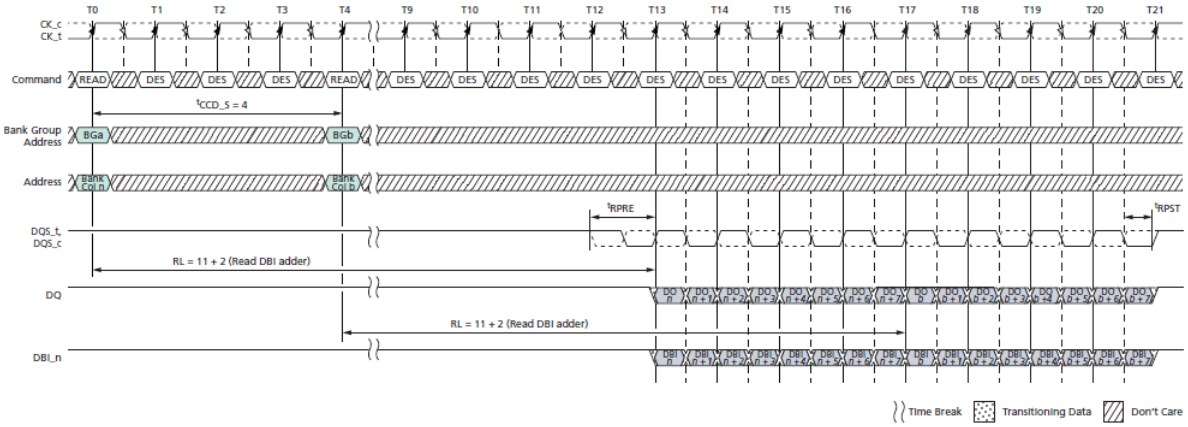


Note:

1. BL = 8, RL = 20 (CL = 11, AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRTP = 6 setting activated by MR0[A11:9 = 001]
5. The example assumes tRC. MIN is satisfied at the next Active command time(T27).
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

READ Operation with Read Data Bus Inversion (DBI)

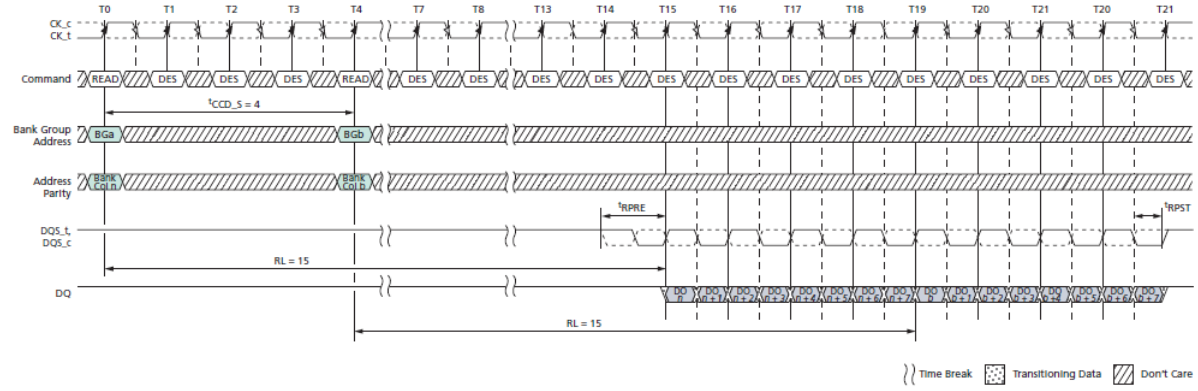
Figure 145. Consecutive READ (BL8) with 1tCK Preamble and DBI in Different Bank Group



Note:

1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK, tDBI = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 00] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Enable.

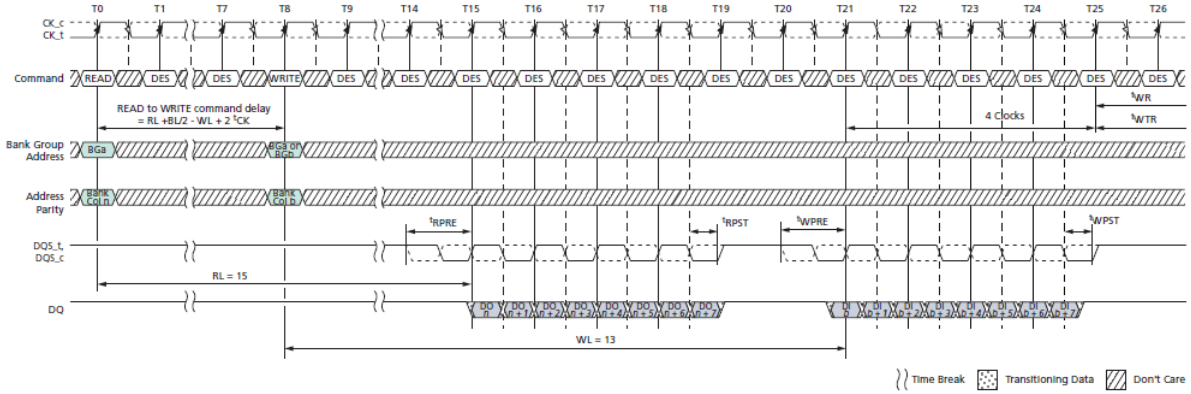
Figure 146. Consecutive READ (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



Note:

1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.
5. CA Parity =Enable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 147. READ (BL8) to WRITE (BL8) with 1tCK Preamble and CA parity in Same or Different Bank Group

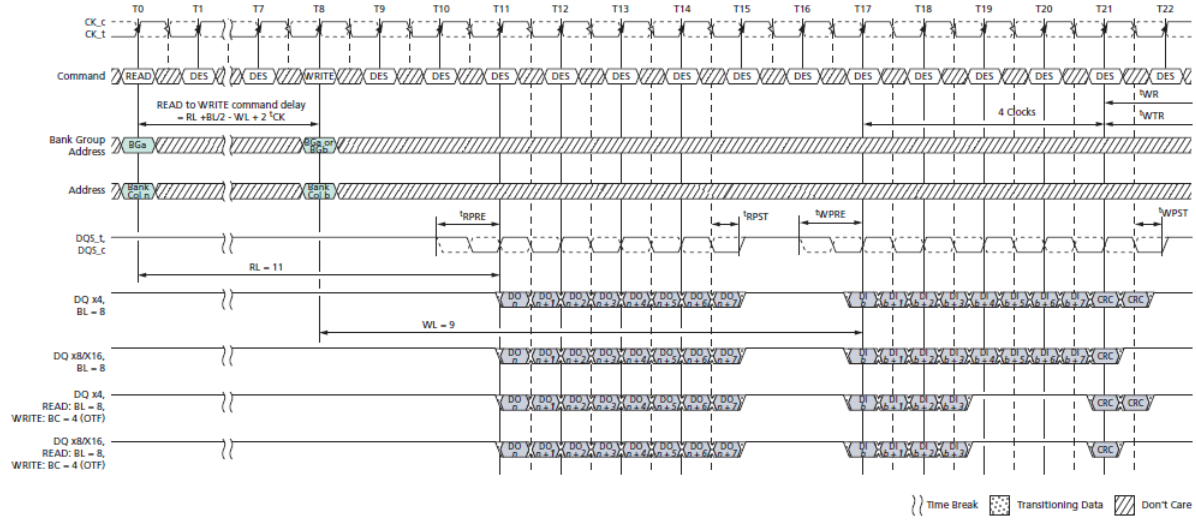


Note:

1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Read Preamble = 1tCK, CWL=9, AL=0, PL=4, (WL=CWL+AL+PL=13), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.
5. CA Parity = Enable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ Followed by WRITE with CRC Enabled

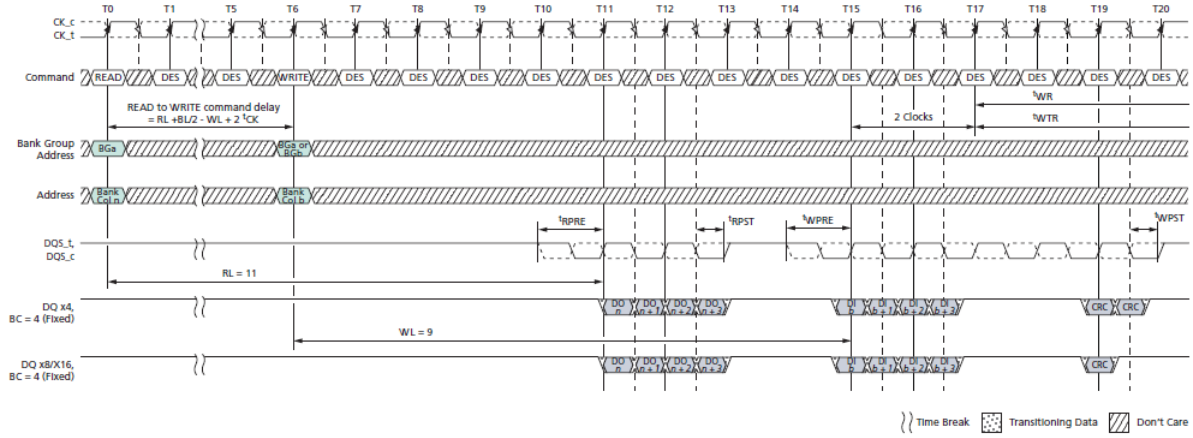
Figure 148. READ (BL8) to WRITE (BL8 or BC4:OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



Note:

1. BL = 8 (or BC = 4 : OTF for Write), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n. DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.
5. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during Write command at T8.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

Figure 149. READ (BC4: Fixed) to WRITE (BC4: Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group

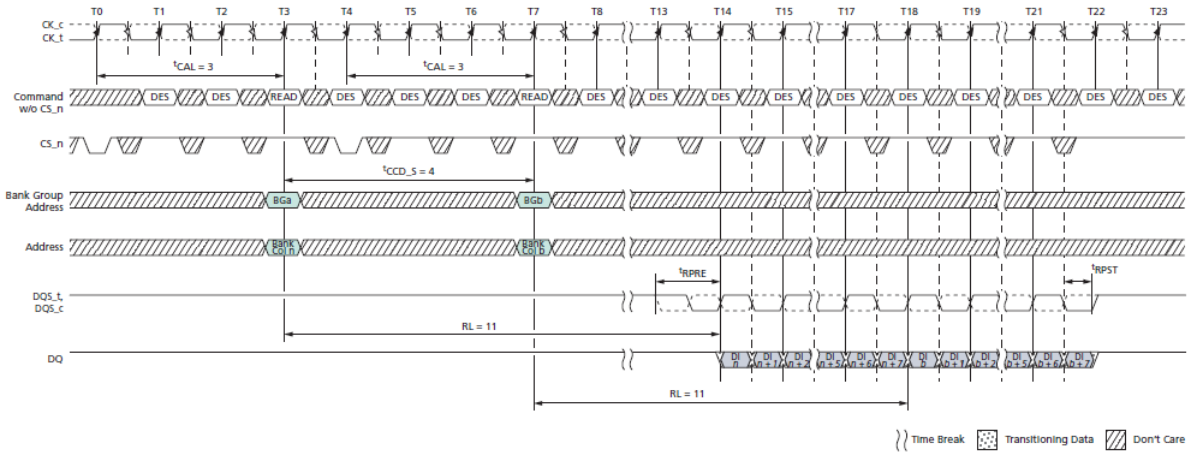


Note:

1. BC = 4 (Fixed), RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*, DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

READ Operation with Command/Address Latency (CAL) Enabled

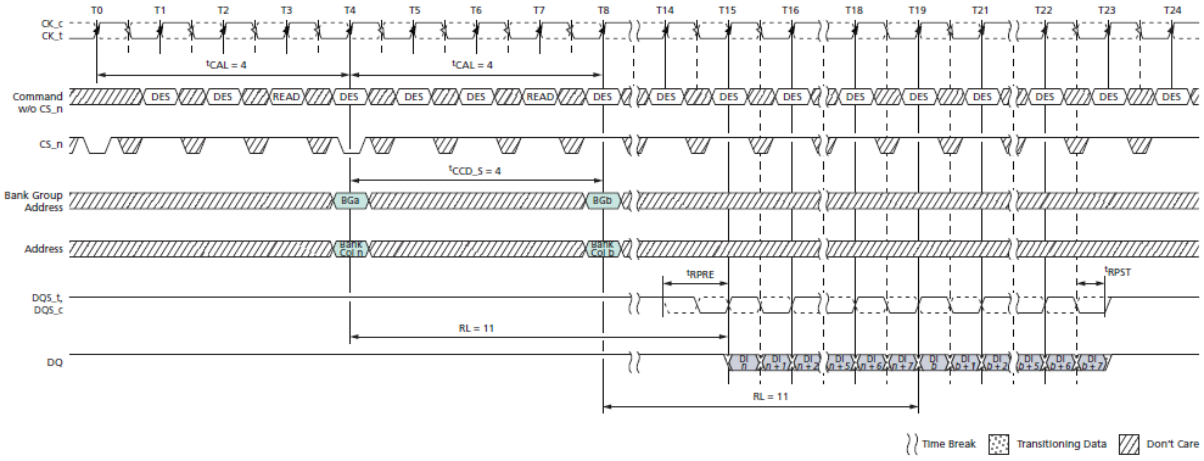
Figure 150. Consecutive READ (BL8) with CAL (3tCK) and 1tCK Preamble in Different Bank Group



Note:

1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T3 and T7.
5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. Enabling CAL mode does not impact ODT control timings. The same timing relationship relative to the command/address bus as when CAL is disabled should be maintained.

Figure 151. Consecutive READ (BL8) with CAL (4tCK) and 1tCK Preamble in Different Bank Group



Note:

1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T3 and T8.
5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. Enabling CAL mode does not impact ODT control timings. The same timing relationship relative to the command/address bus as when CAL is disabled should be maintained.

WRITE Operation

Write Timing Definitions

The write timings shown in the following figures are applicable in normal operation mode, that is, when the DLL is enabled and locked.

Write Timing – Clock-to-Data Strobe Relationship

The clock-to-data strobe relationship is shown below and is applicable in normal operation mode, that is, when the DLL is enabled and locked.

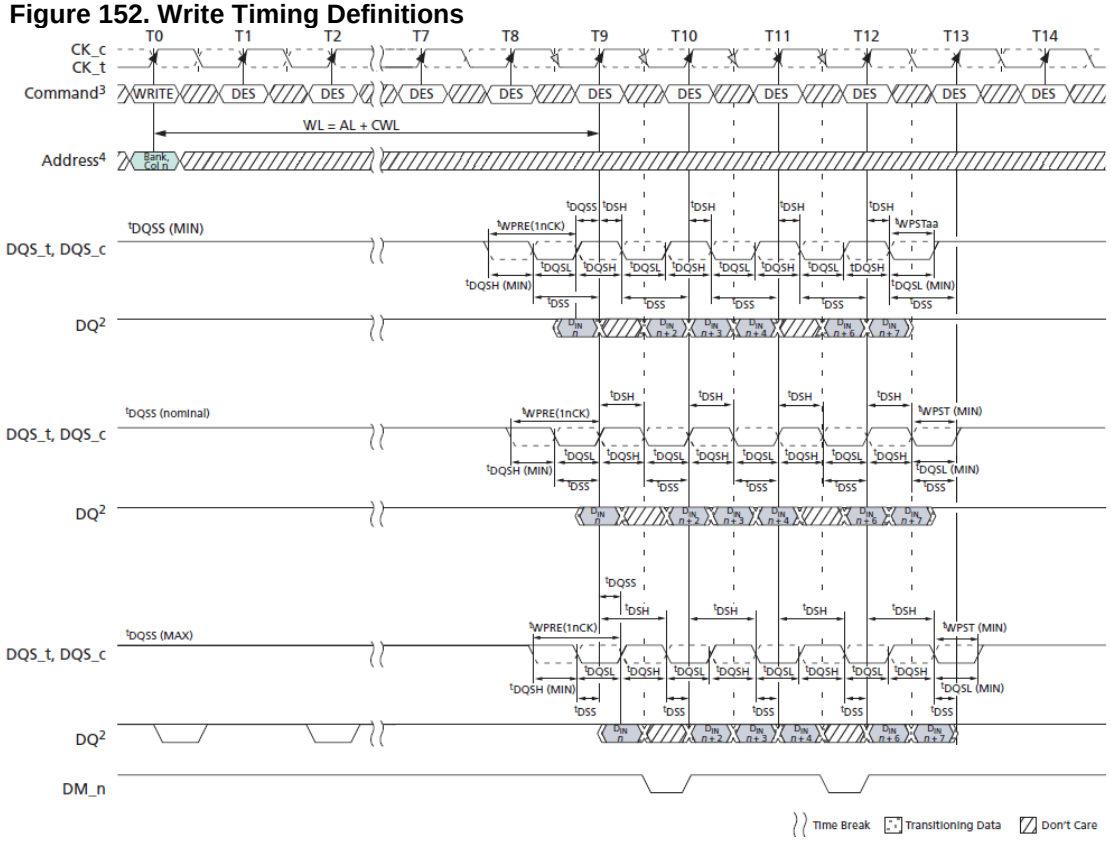
Rising data strobe edge parameters:

- tDQSS (MIN) to tDQSS (MAX) describes the allowed range for a rising data strobe edge relative to CK.
- tDQSS is the actual position of a rising strobe edge relative to CK.
- tDQSH describes the data strobe high pulse width.
- tWPST strobe going to HIGH, nondrive level (shown in the postamble section of the graphic below).

Falling data strobe edge parameters:

- tDQSL describes the data strobe low pulse width.
- tWPRE strobe going to LOW, initial drive level (shown in the preamble section of the graphic below).

Figure 152. Write Timing Definitions

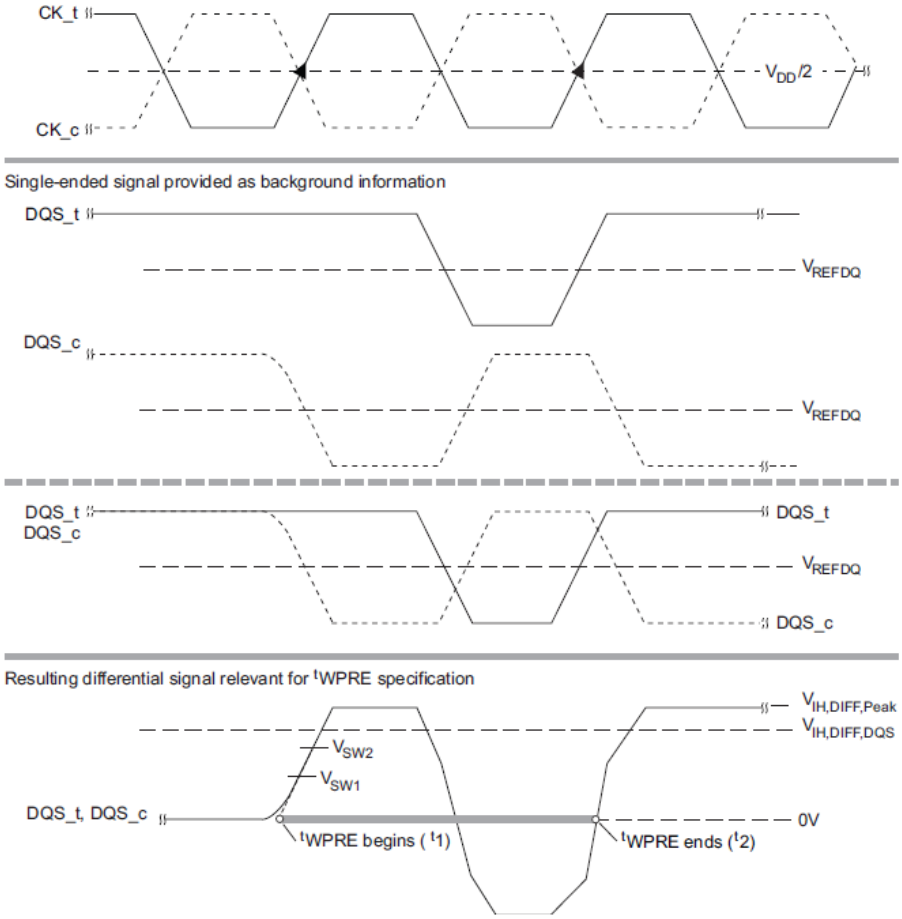


Note:

1. BL8, WL = 9 (AL = 0, CWL = 9).
2. DIN *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. ^{t}DQSS must be met at each rising clock edge.

tWPRE Calculation

Figure 153. tWPRE Method for Calculating Transitions and Endpoints

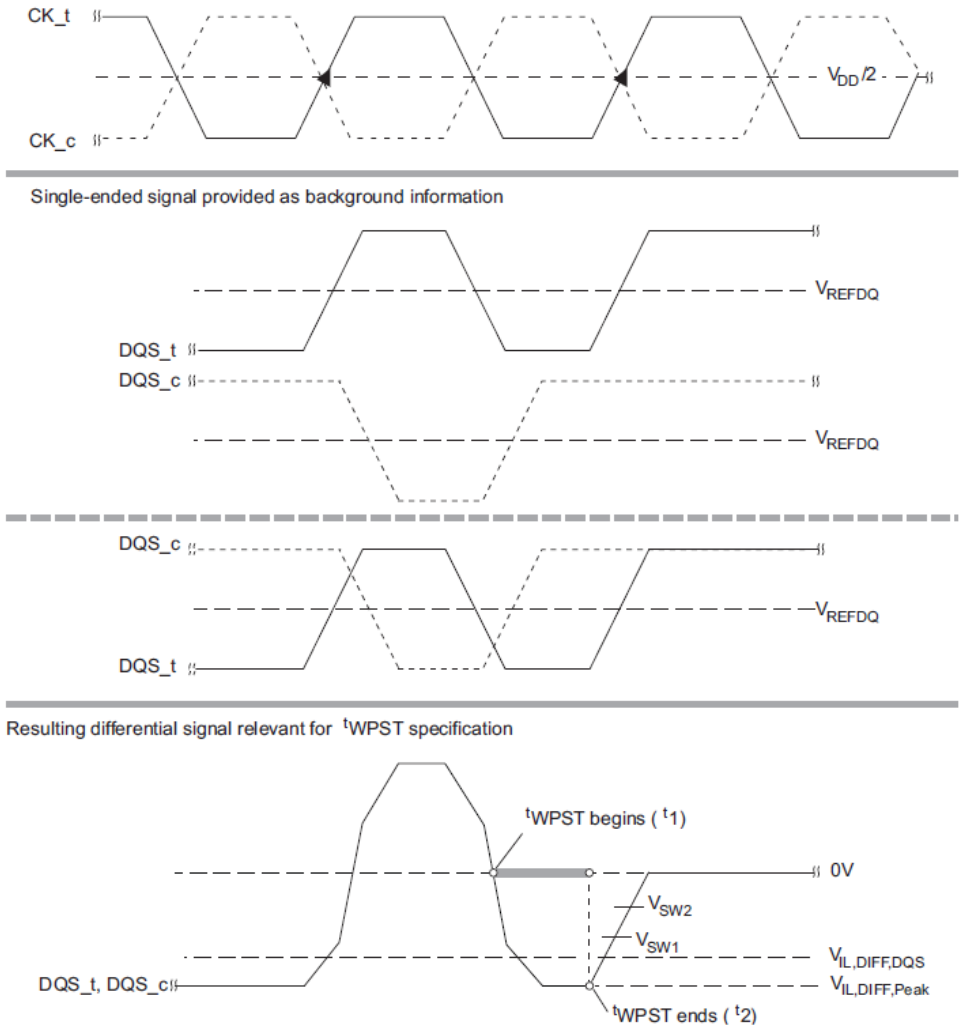


Note:

1. V_{sw1} = (0.1) x $V_{IH,diff,DQS}$.
2. V_{sw2} = (0.9) x $V_{IH,diff,DQS}$.

tWPST Calculation

Figure 154. tWPST Method for Calculating Transitions and Endpoints



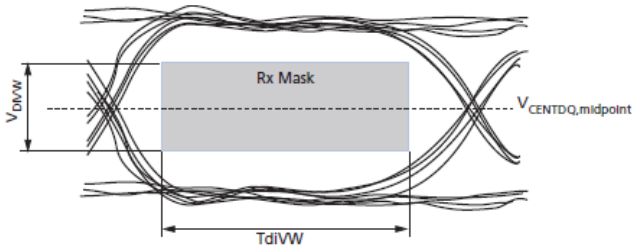
Note:

1. V_{sw1} = (0.9) x $V_{IL,diff,DQS}$.
2. V_{sw2} = (0.1) x $V_{IL,diff,DQS}$.

Write Timing –Data Strobe-to-Data Relationship

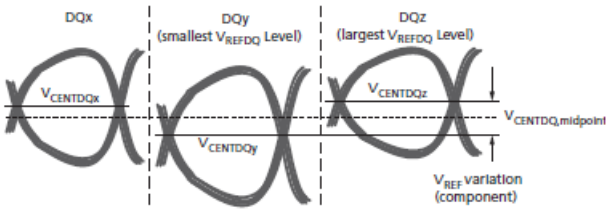
The DQ input receiver uses a compliance mask (Rx) for voltage and timing as shown in the figure below. The receiver mask (Rx mask) defines the area where the input signal must not encroach in order for the DRAM input receiver to be able to successfully capture a valid input signal. The Rx mask is not the valid data-eye. T_{diVW} and V_{diVW} define the absolute maximum Rx mask.

Figure 155. Rx Compliance Mask



$V_{CENTDQ,midpoint}$ is defined as the midpoint between the largest V_{REFDQ} voltage level and the smallest V_{REFDQ} voltage level across all DQ pins for a given DRAM. Each DQ pin's VREFDQ is defined by the center (widest opening) of the cumulative data input eye as depicted in the following figure. This means a DRAM's level variation is accounted for within the DRAM Rx mask. The DRAM V_{REFDQ} level will be set by the system to account for R_{ON} and ODT settings.

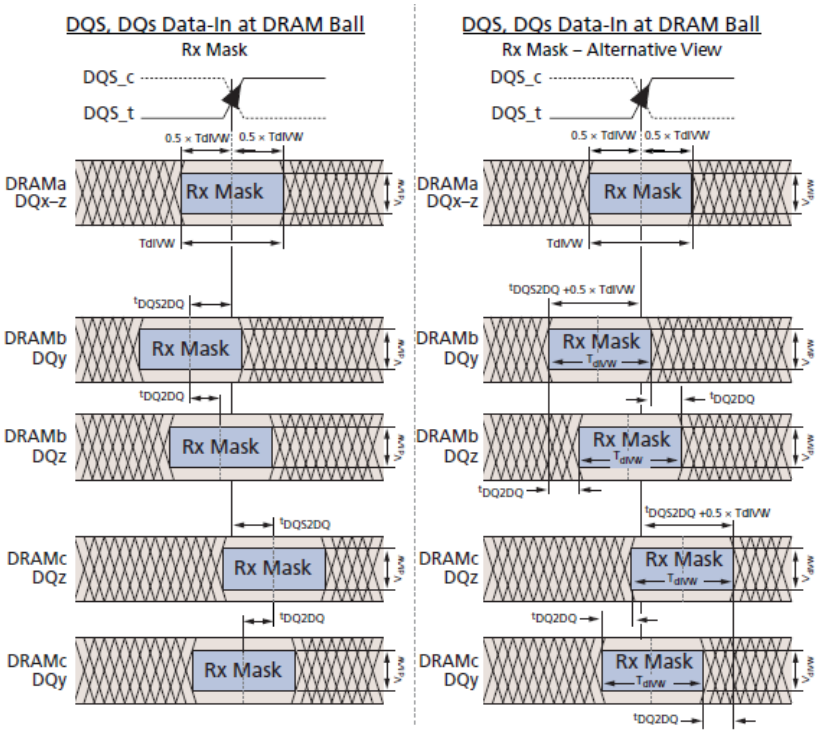
Figure 156. V_{CENT_DQ} V_{REFDQ} Voltage Variation



The following figure shows the Rx mask requirements both from a midpoint-to-midpoint reference (left side) and from an edge-to-edge reference. The intent is not to add any new requirement or specification between the two but rather how to convert the relationship between the two methodologies.

The minimum data-eye shown in the composite view is not actually obtainable due to the minimum pulse width requirement.

Figure 157. Rx Mask DQ-to-DQS Timings

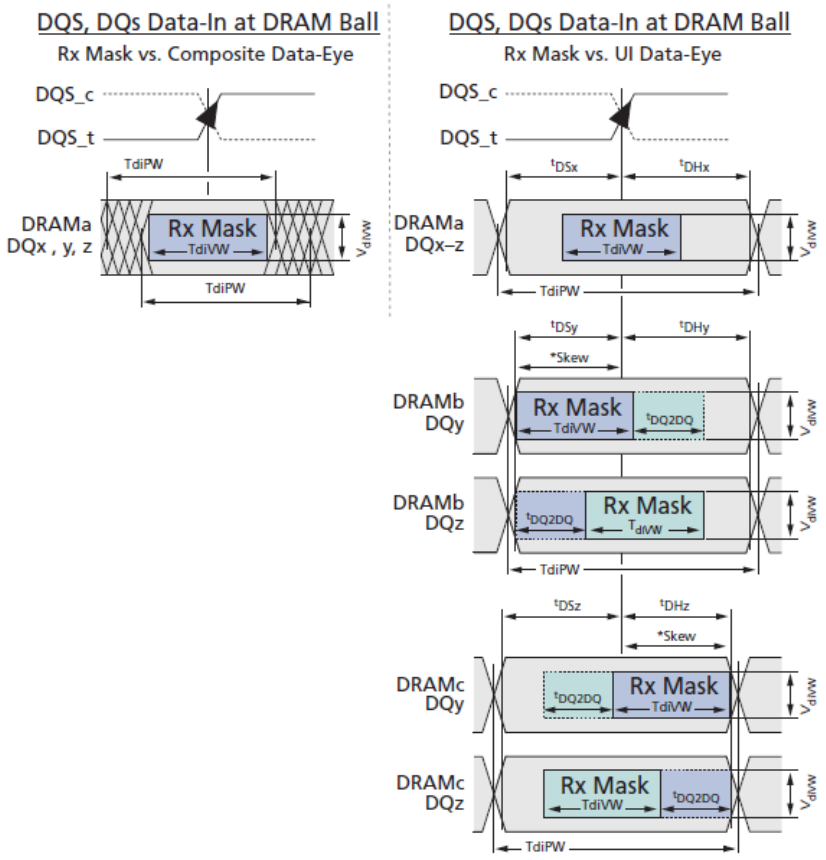


Note:

1. DQx represents an optimally centered mask.
   DQy represents earliest valid mask.
   DQz represents latest valid mask.
2. DRAMa represents a DRAM without any DQS/DQ skews.
   DRAMb represents a DRAM with early skews (negative ^{t}DQS2DQ).
   DRAMc represents a DRAM with delayed skews (positive ^{t}DQS2DQ).
3. This figure shows the skew allowed between DRAM-to-DRAM and between DQ-to-DQ for a DRAM. Signals assume data is center-aligned at DRAM latch.
   T_{diPW} is not shown; composite data-eyes shown would violate T_{diPW}.
   $V_{CENTDQ,midpoint}$ is not shown but is assumed to be midpoint of V_{diVW}.

The previous figure shows the basic Rx mask requirements. Converting the Rx mask requirements to a classical DQ-to-DQS relationship is shown in the following figure. It should become apparent that DRAM write training is required to take full advantage of the Rx mask.

Figure 158. Rx Mask DQ-to-DQS DRAM-Based Timings

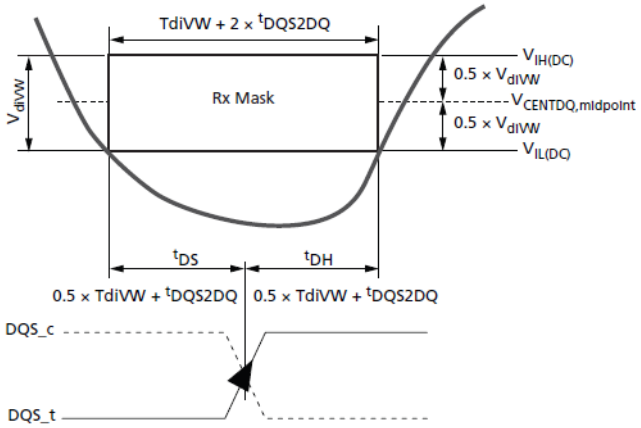


Note:

1. DQx represents an optimally centered mask.
   DQy represents earliest valid mask.
   DQz represents latest valid mask.
2. *Skew = ^{t}DQS2DQ + 0.5 x T_{diVW}
   DRAMa represents a DRAM without any DQS/DQ skews.
   DRAMb represents a DRAM with the earliest skews (negative ^{t}DQS2DQ, ^{t}DQSy > *Skew).
   DRAMc represents a DRAM with the latest skews (positive ^{t}DQS2DQ, ^{t}DQHz > *Skew).
3. ^{t}DS/^{t}DH are traditional data-eye setup/hold edges at DC levels.
   ^{t}DS and ^{t}DH are not specified; ^{t}DH and ^{t}DS may be any value provided the pulse width and Rx mask limits are not violated.
   ^{t}DH (MIN) > T_{diVW} + ^{t}DS (MIN) + ^{t}DQ2DQ.

The DDR4 SDRAM's input receivers are expected to capture the input data with an Rx mask of T_{diVW} provided the minimum pulse width is satisfied. The DRAM controller will have to train the data input buffer to utilize the Rx mask specifications to this maximum benefit. If the DRAM controller does not train the data input buffers, then the worst case limits have to be used for the Rx mask (T_{diVW} + 2 x ^{t}DQS2DQ), which will generally be the classical minimum (^{t}DS and ^{t}DH) and is required as well.

Figure 159. Example of Data Input Requirements Without Training



WRITE Burst Operation

The following write timing diagrams are intended to help understand each write parameter's meaning and are only examples. Each parameter will be defined in detail separately. In these write timing diagrams, CK and DQS are shown aligned, and DQS and DQ are shown center-aligned for the purpose of illustration.

DDR4 WRITE command supports bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF when OTF is enabled:

- A12 = 0, BC4 (BC4 = burst chop)
- A12 = 1, BL8

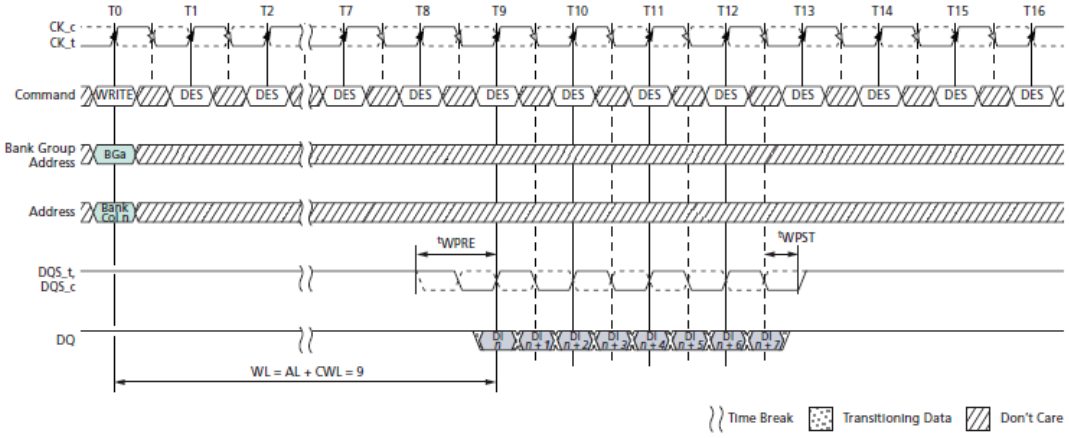
WRITE commands can issue precharge automatically with a WRITE with auto precharge (WRA) command, which is enabled by A10 HIGH.

- WRITE command with A10 = 0 (WR) performs standard write, bank remains active after WRITE burst
- WRITE command with A10 = 1 (WRA) performs write with auto precharge, bank goes into precharge after WRITE burst

The DATA MASK (DM) function is supported for the x16 configurations only.
The DM function shares a common pin with the DBI_n functions. The DM function only applies to WRITE operations and cannot be enabled at the same time the DBI function is enabled.

- If DM_n is sampled LOW on a given byte lane, the DRAM masks the write data received on the DQ inputs.
- If DM_n is sampled HIGH on a given byte lane, the DRAM does not mask the data and writes this data into the DRAM core.
- If CRC write is enabled, then DM enabled (via MRS) will be selected between write CRC nonpersistent mode (DM disabled) and write CRC persistent mode (DM enabled).

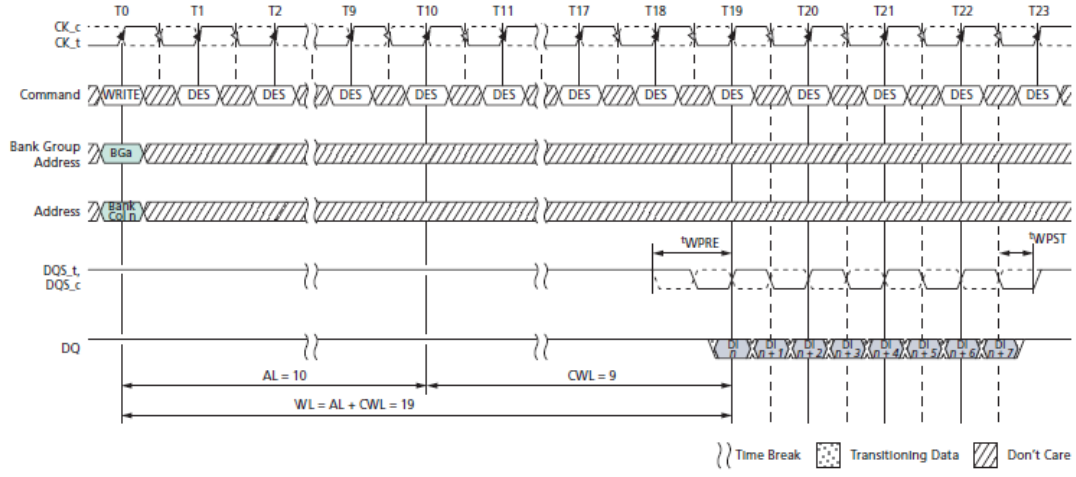
Figure 160. WRITE Burst Operation, WL = 9 (AL = 0, CWL = 9, BL8)



Note:

1. BL8, WL = 0, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* = Data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 161. WRITE Burst Operation, WL = 19 (AL = 10, CWL = 9, BL8)

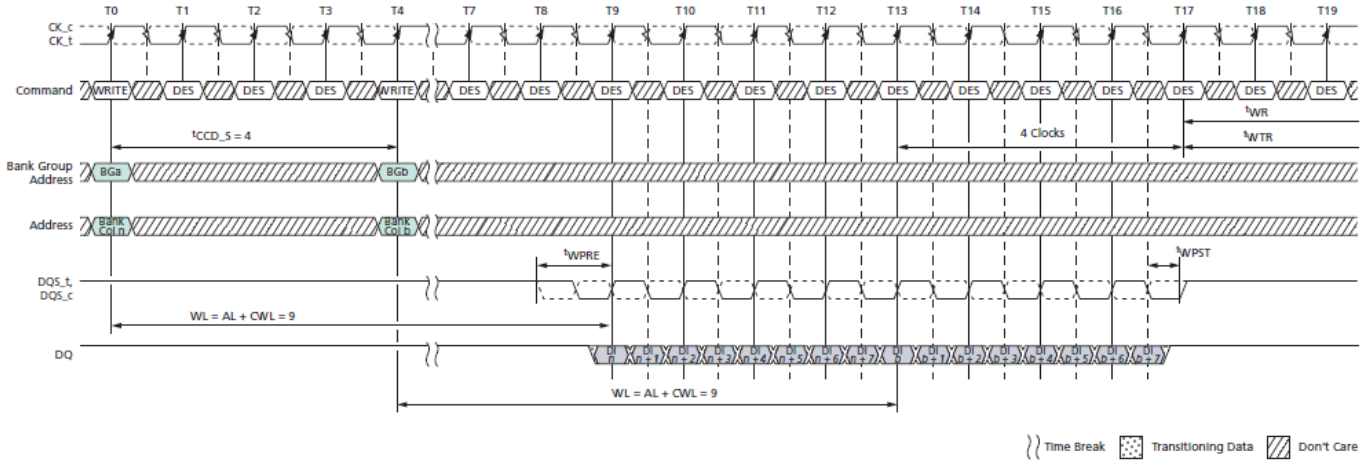


Note:

1. BL8, WL = 19, AL = 10 (CL - 1), CWL = 9, Preamble = 1tCK.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

WRITE Operation Followed by Another WRITE Operation

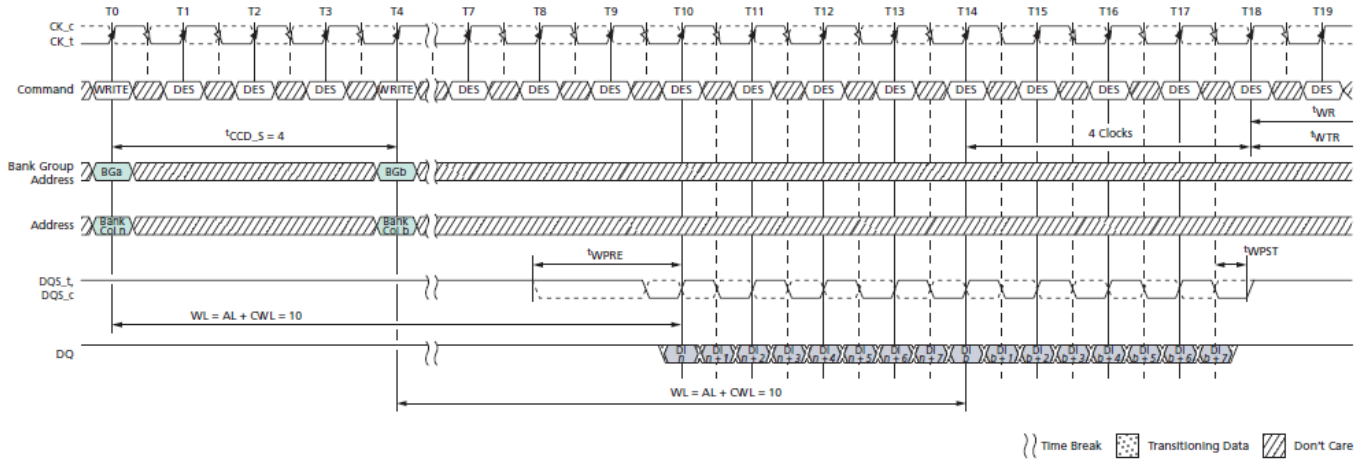
Figure 162. Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group



Note:

1. BL = 8, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T4.
5. C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

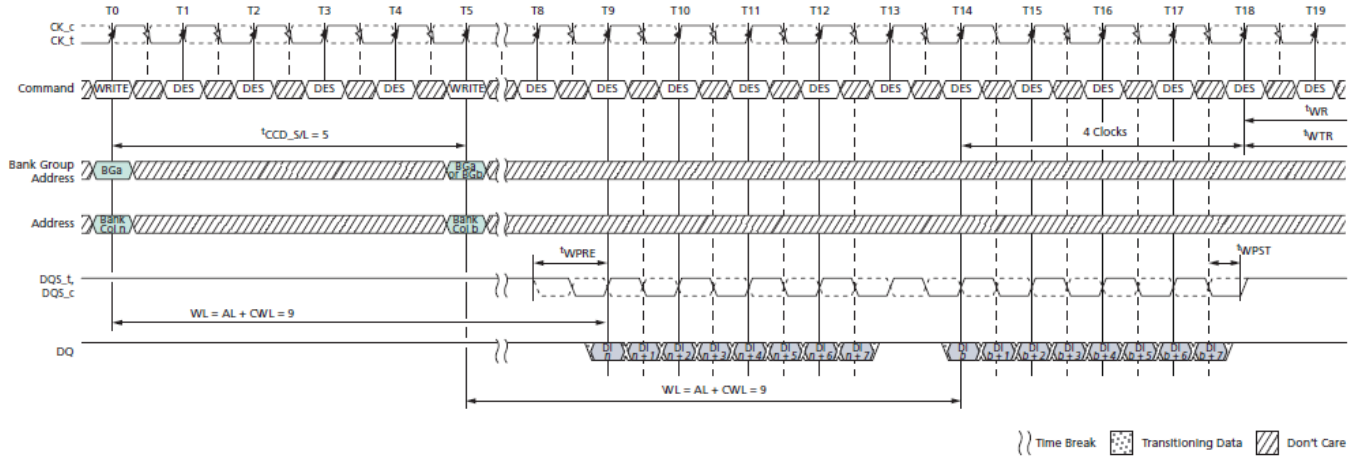
Figure 163. Consecutive WRITE (BL8) with 2tCK Preamble in Different Bank Group



Note:

1. BL = 8, AL = 0, CWL = 9 + 1 = 10 (see note 7), Preamble = 2tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time(tWR) and write timing parameter(tWTR) are referenced from the first rising clock edge after the last write data shown at T18.
7. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

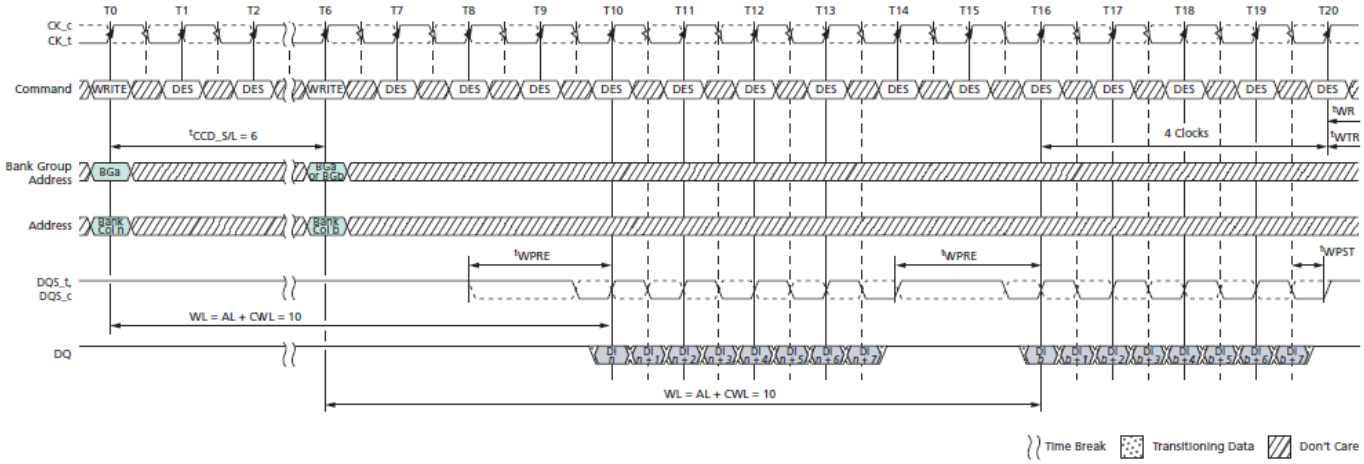
Figure 164. Nonconsecutive WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



Note:

1. BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T5.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

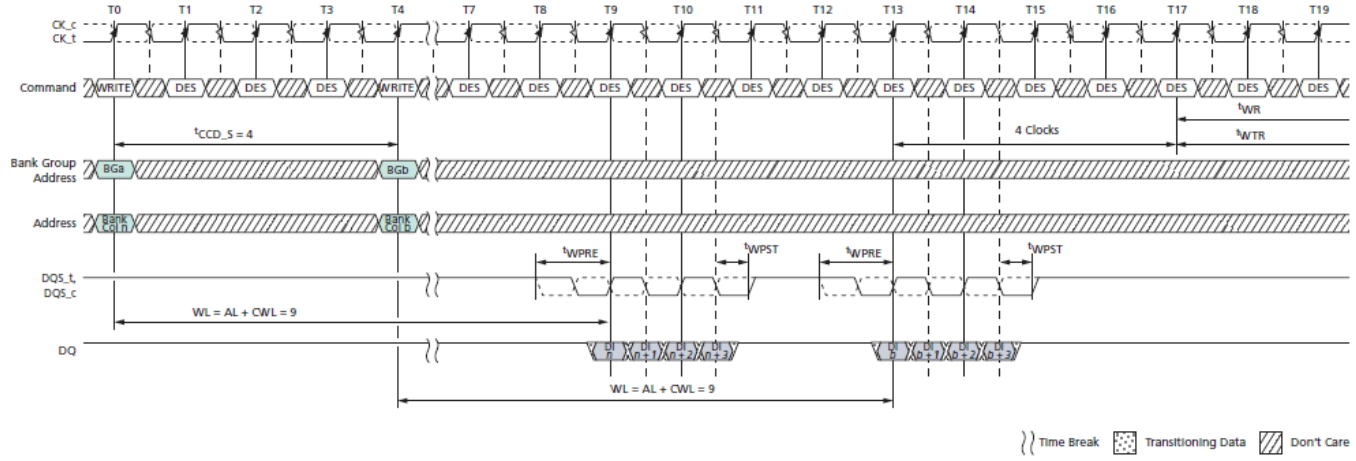
Figure 165. Nonconsecutive WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



Note:

1. BL = 8, AL = 0, CWL = 9 + 1 = 10 (see note 8), Preamble = 2tCK, tCCD_S/L = 6
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. tCCD_S/L=5 isn't allowed in 2tCK preamble mode.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T20.
8. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

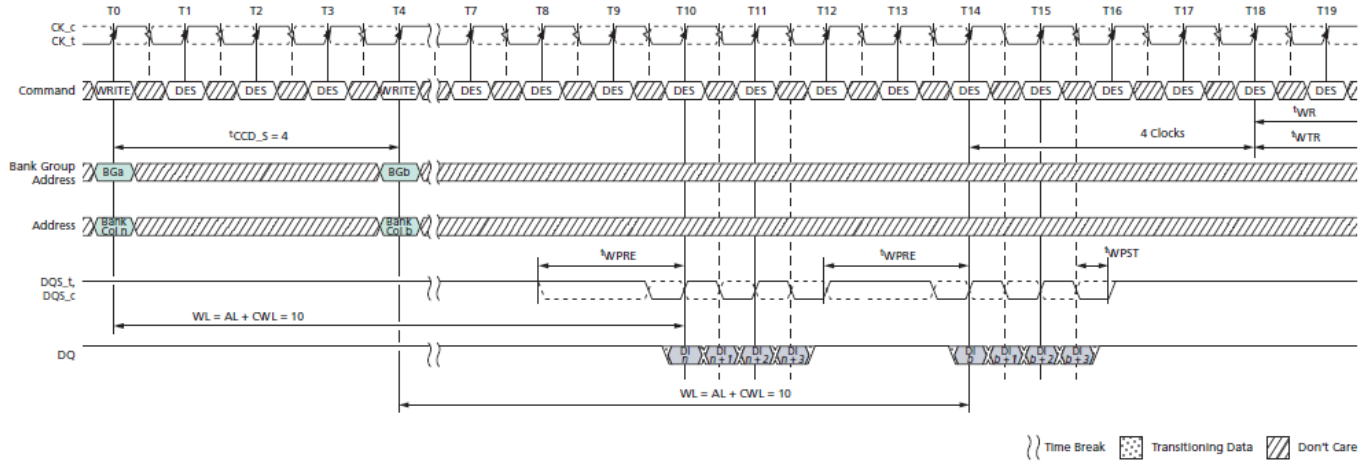
Figure 166. WRITE (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



Note:

1. BC = 4, AL = 0, CWL = 9 , Preamble = 1tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

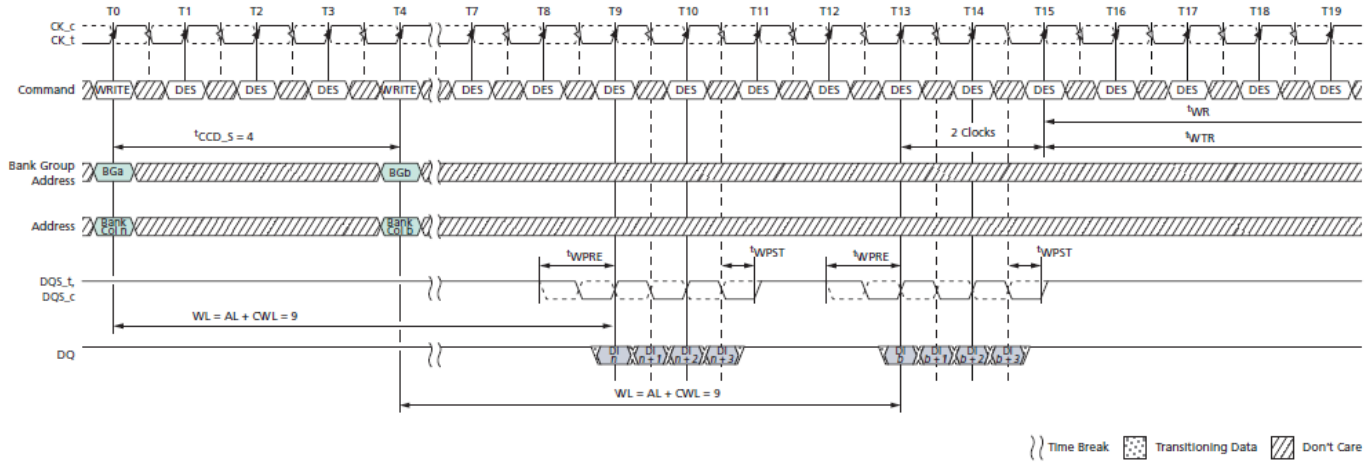
Figure 167. WRITE (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Different Bank Group



Note:

1. BC = 4, AL = 0, CWL = 9 + 1 = 10 (se note 7) , Preamble = 2tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.
7. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

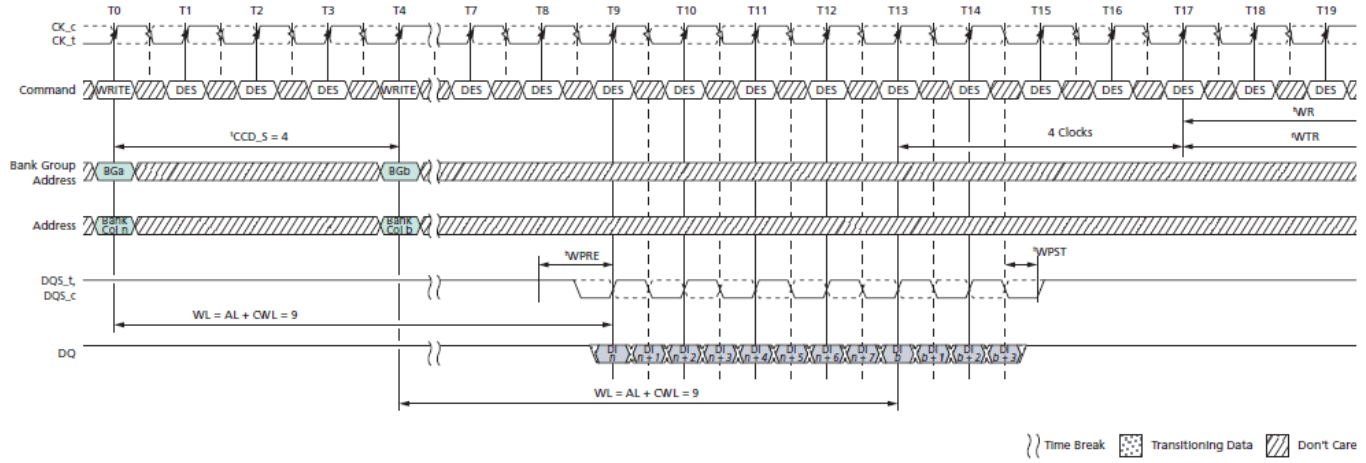
Figure 168. WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Different Bank Group



Note:

1. BC = 4, AL = 0, CWL = 9 , Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T15.

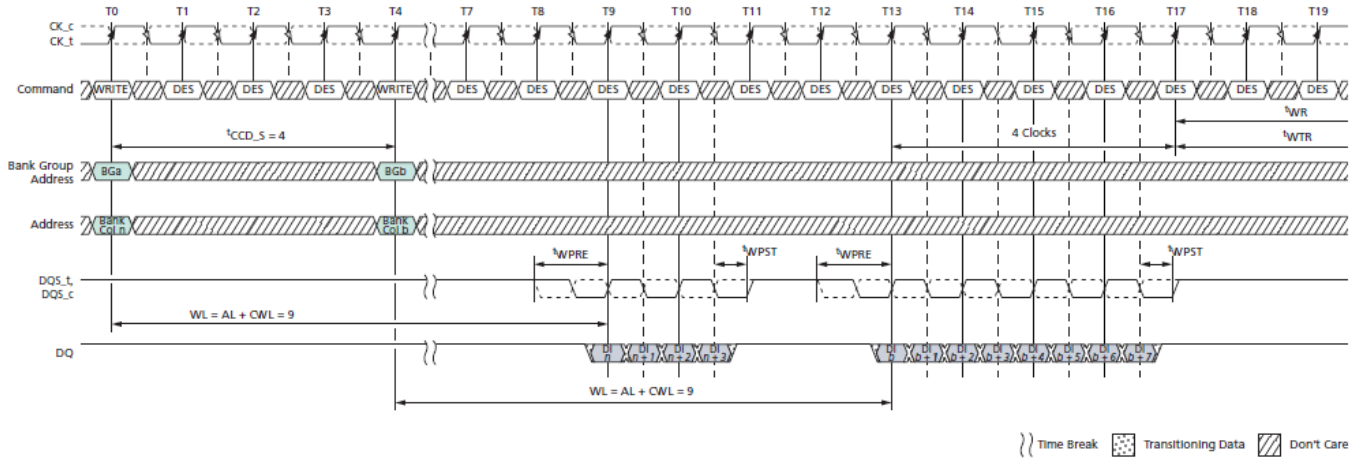
Figure 169. WRITE (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



Note:

1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17

Figure 170. WRITE (BC4) OTF to WRITE (BL8) with 1tCK Preamble in Different Bank Group

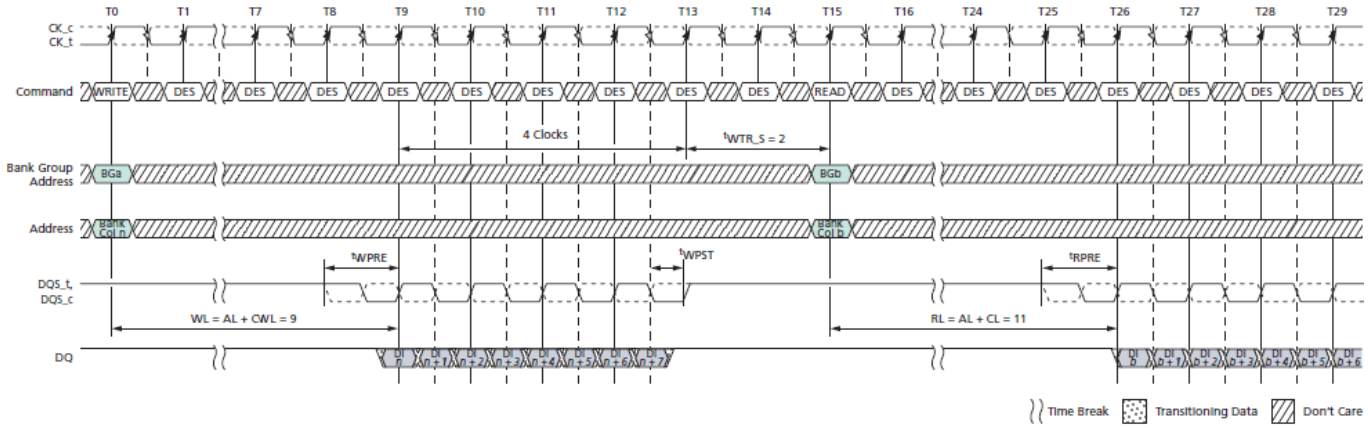


Note:

1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17

WRITE Operation Followed by READ Operation

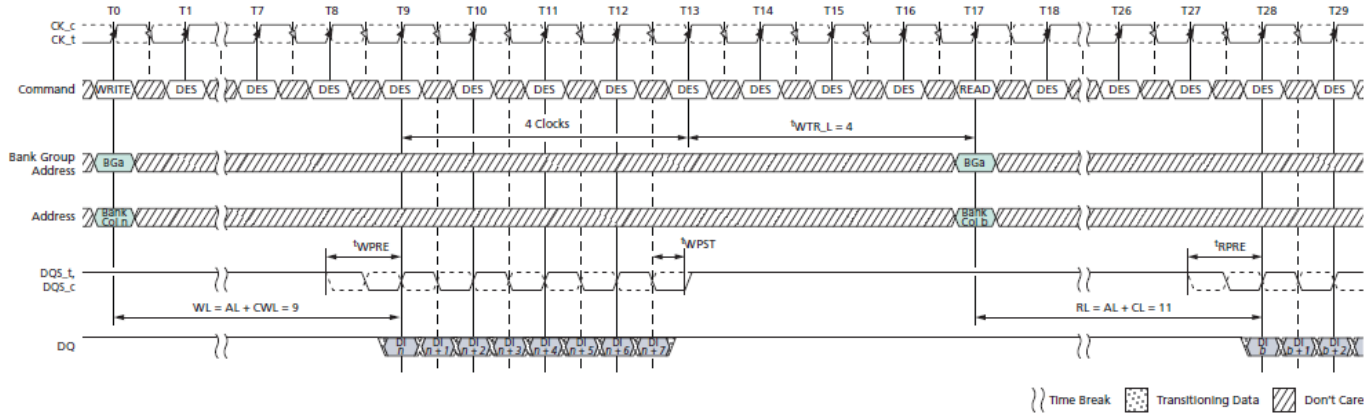
Figure 171. WRITE (BL8) to READ (BL8) with 1tCK Preamble in Different Bank Group



Note:

1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n(or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and READ command at T15.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13. When AL is non-zero, the external read command at T15 can be pulled in by AL.

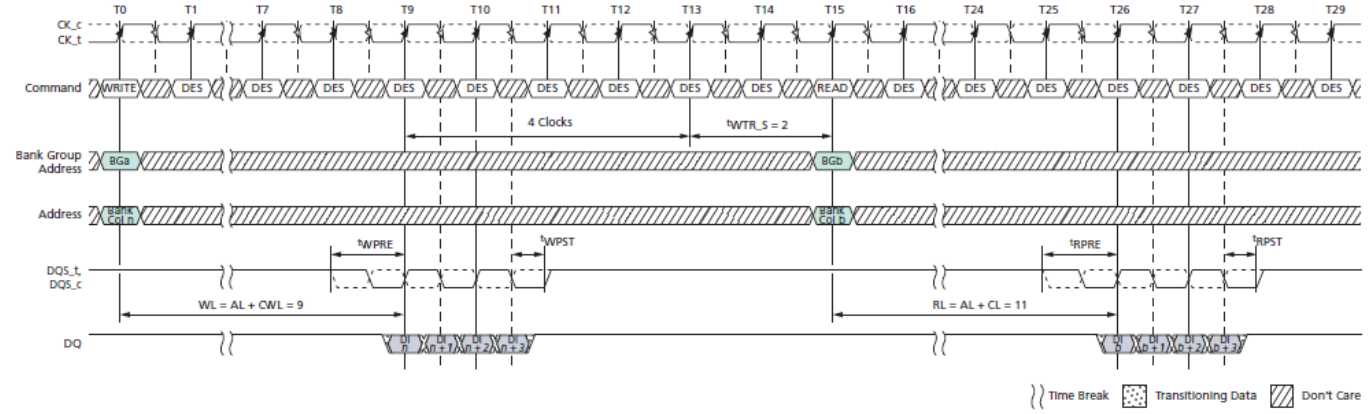
Figure 172. WRITE (BL8) to READ (BL8) with 1tCK Preamble in Same Bank Group



Note:

1. BL = 8, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and READ command at T17.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13.

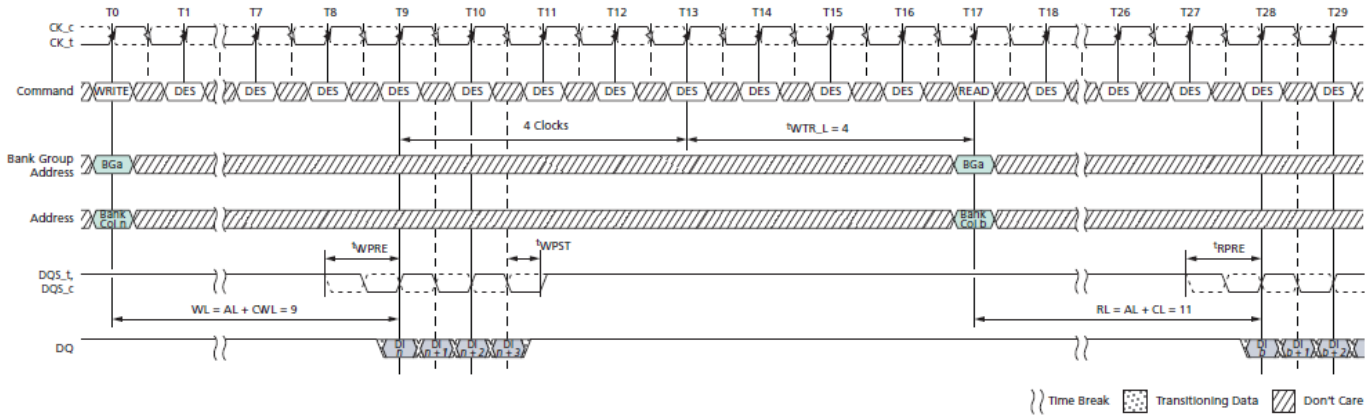
Figure 173. WRITE (BC4) OTF to READ (BC4) OTF with 1tCK Preamble in Different Bank Group



Note:

1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and READ command at T15.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13.

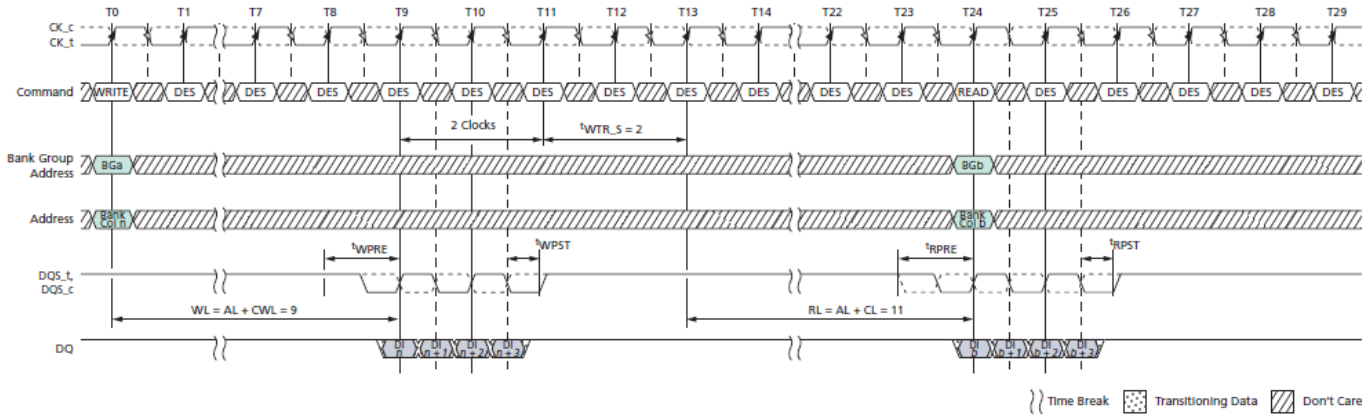
Figure 174. WRITE (BC4) OTF to READ (BC4) OTF with 1tCK Preamble in Same Bank Group



Note:

1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and READ command at T17.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13.

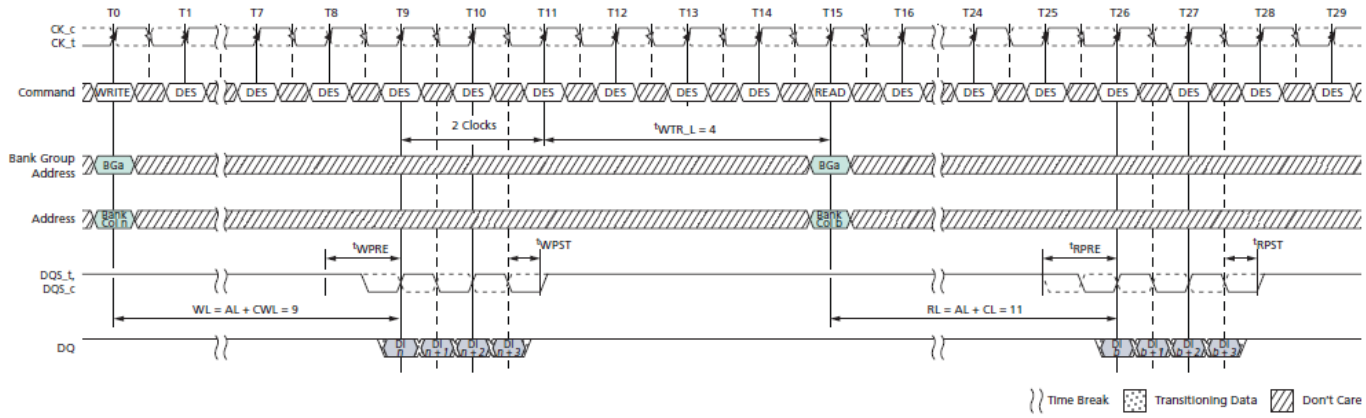
Figure 175. WRITE (BC4) Fixed to READ (BC4) Fixed with 1tCK Preamble in Different Bank Group



Note:

1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T11.

Figure 176. WRITE (BC4) Fixed to READ (BC4) Fixed with 1tCK Preamble in Same Bank Group



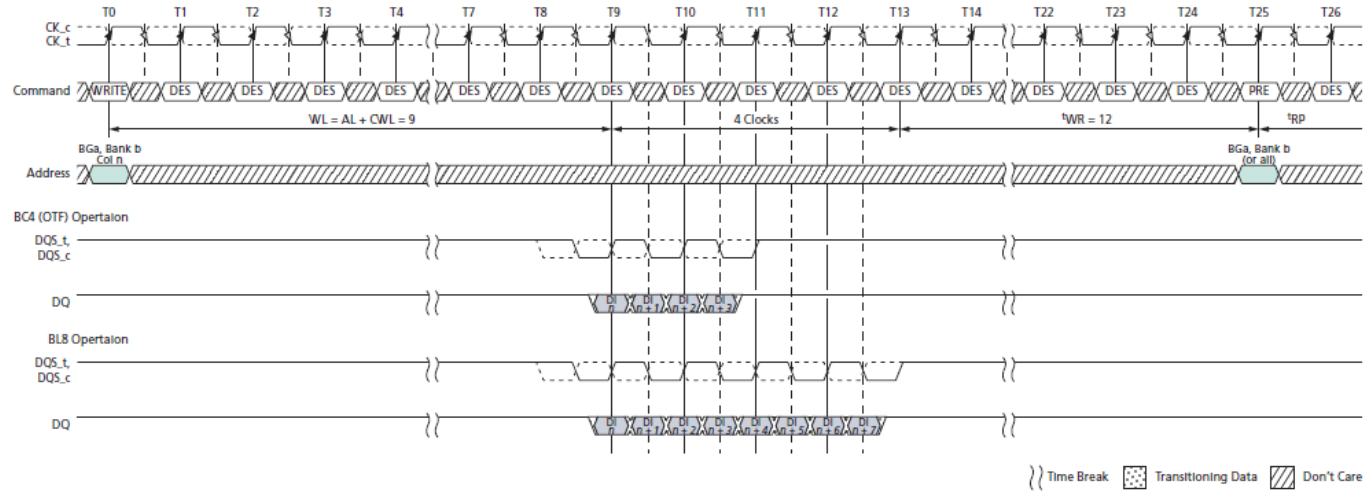
Note:

1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T11.

WRITE Operation Followed by PRECHARGE Operation

The minimum external WRITE command to PRECHARGE command spacing is equal to WL (AL + CWL) plus either 4^{t}CK (BL8/BC4-OTF) or 2tCK (BC4-fixed) plus tWR. The minimum ACT to PRE timing, ^{t}RAS, must be satisfied as well.

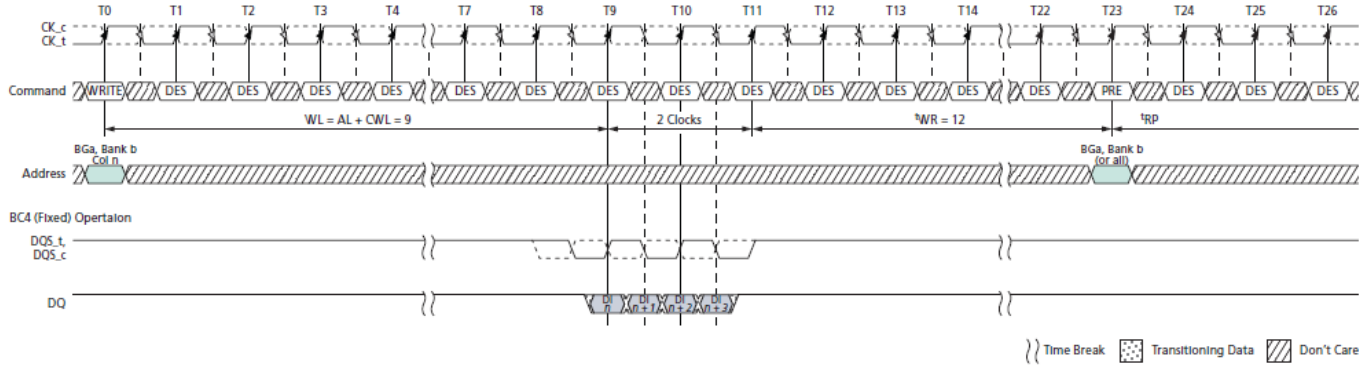
Figure 177. WRITE (BL8/BC4-OTF) to PRECHARGE with 1^{t}CK Preamble



Note:

1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK, tWR = 12.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0. BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

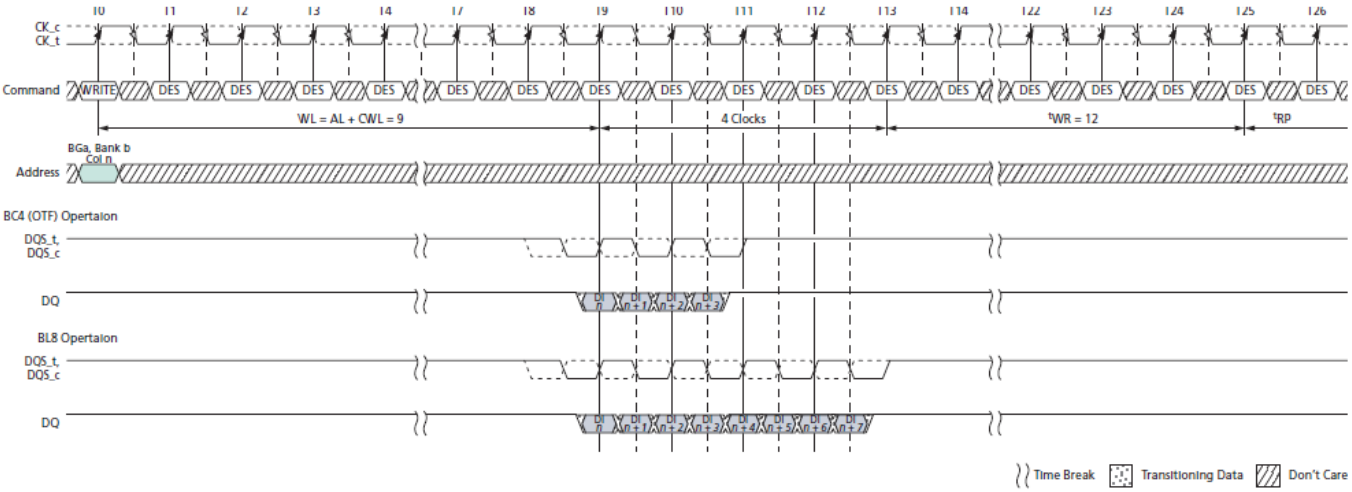
Figure 178. WRITE (BC4-Fixed) to PRECHARGE with 1tCK Preamble



Note:

1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK, tWR = 12.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

Figure 179. WRITE (BL8/BC4-OTF) to Auto PRECHARGE with 1tCK Preamble

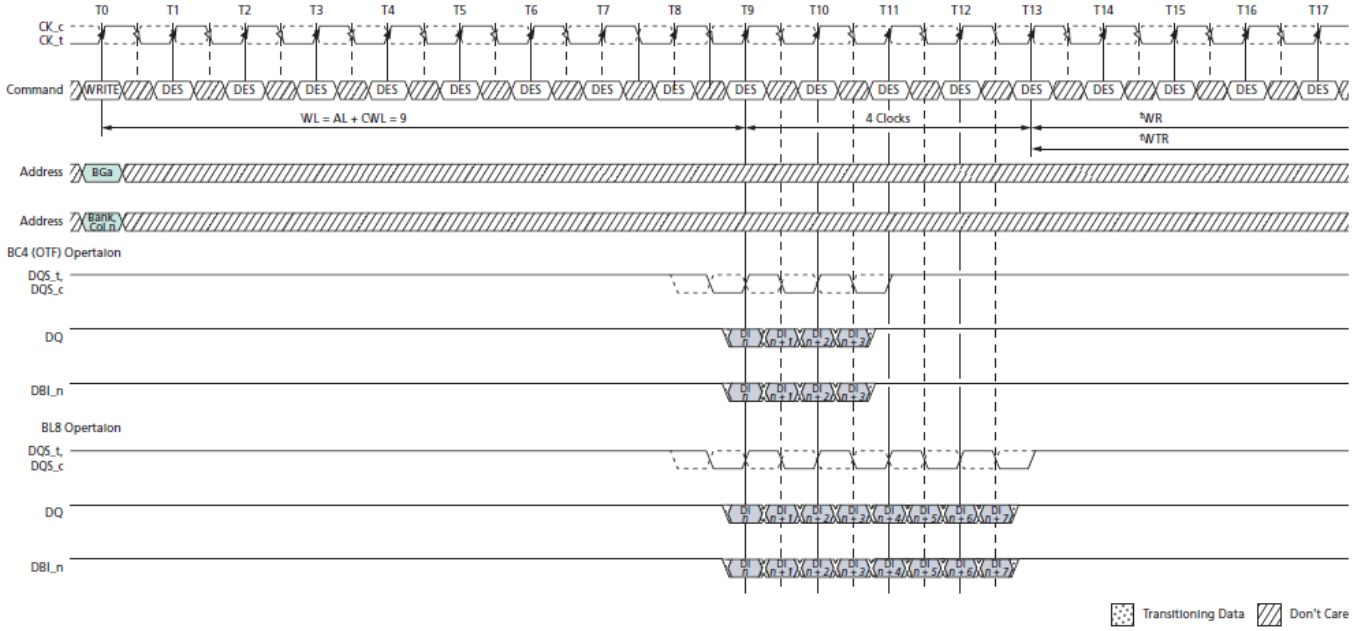


Note:

1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK, tWR = 12.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0.
   BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

WRITE Operation with WRITE DBI Enabled

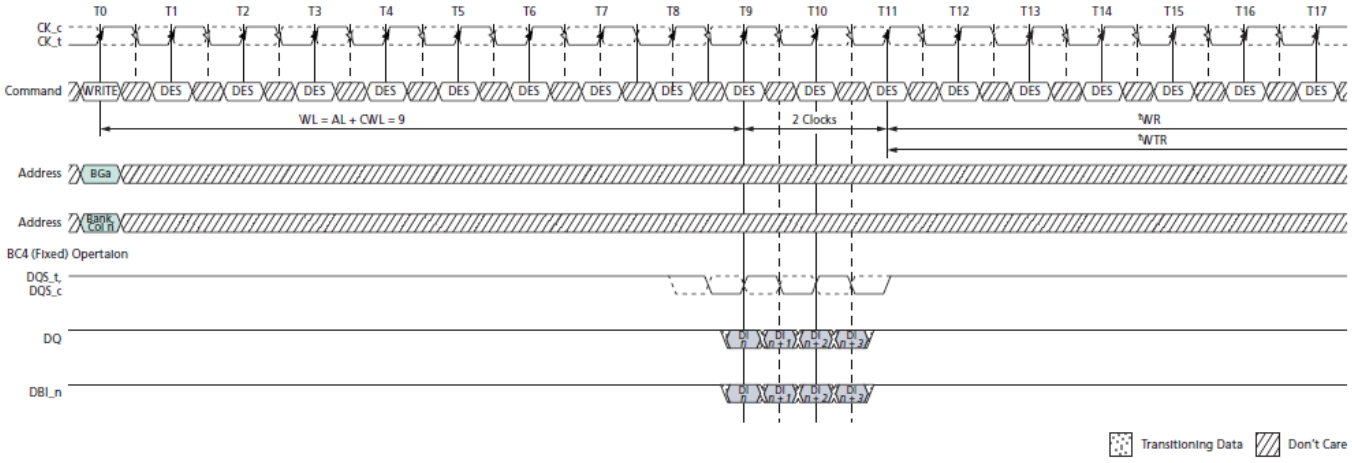
Figure 180. WRITE (BL8/BC4-OTF) with 1tCK Preamble and DBI



Note:

1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0.
   BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Enabled, Write CRC = Disabled.
6. The write recovery time (tWR_DBI) is referenced from the first rising clock edge after the last write data shown at T13.

Figure 181. WRITE (BC4-Fixed) with 1tCK Preamble and DBI

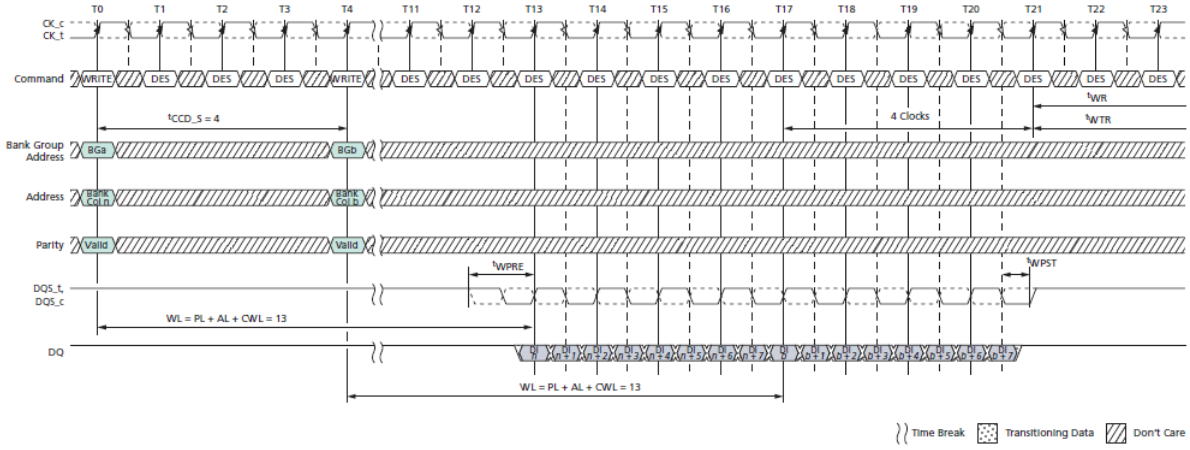


Note:

1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Enabled, Write CRC = Disabled.

WRITE Operation with CA Parity Enabled

Figure 182. Consecutive WRITE (BL8) with 1tCK Preamble and CA Parity in Different Bank Group

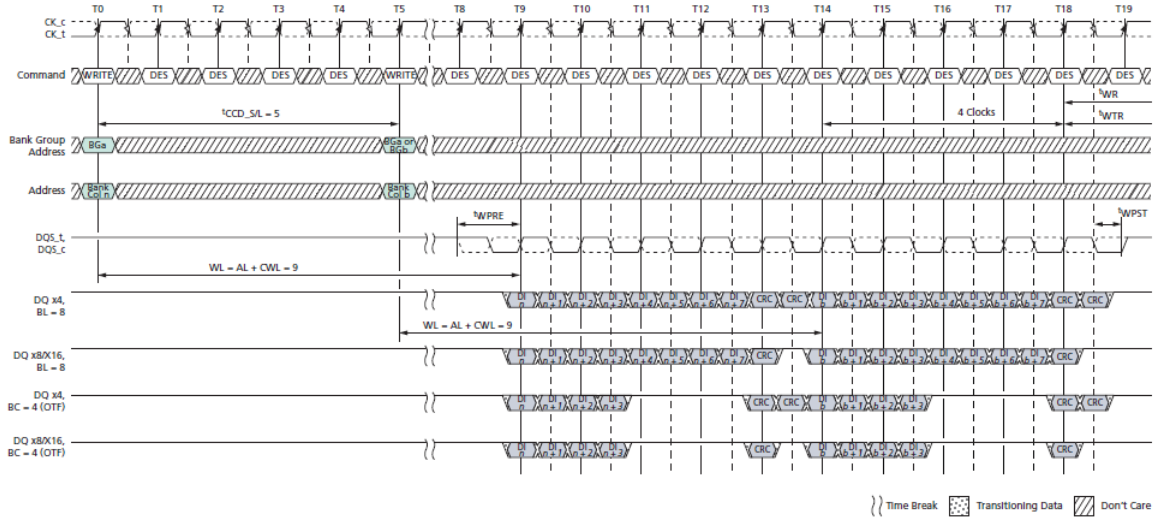


Note:

1. BL = 8, AL = 0, CWL = 9, PL = 4, Preamble = 1tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0 and T4.
5. CA Parity = Enable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.

WRITE Operation with Write CRC Enabled

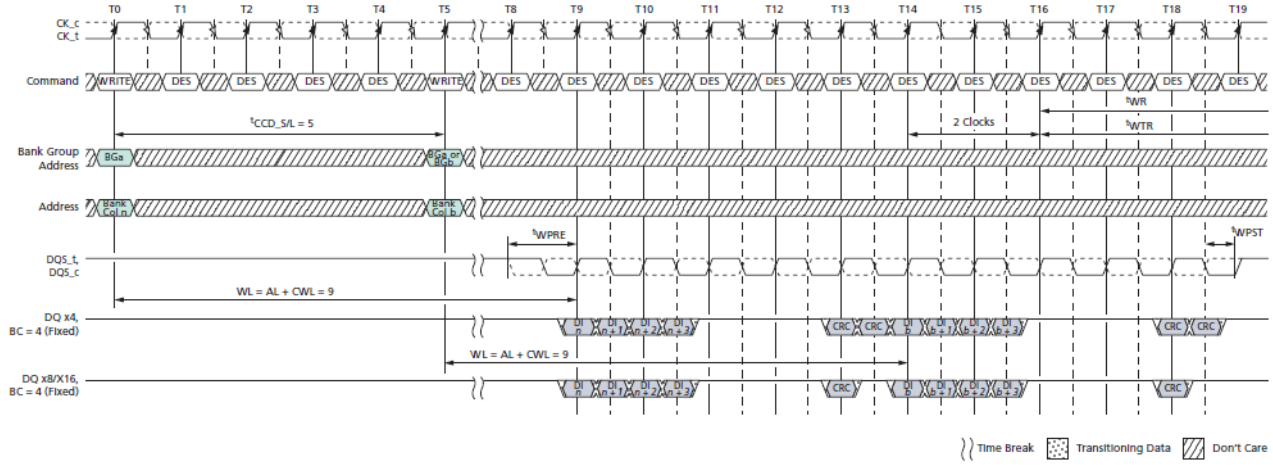
Figure 183. Consecutive WRITE (BL8/BC4) OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



Note:

1. BL = 8/BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0 and T5.
5. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T5.
6. C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable, Write CRC = Enable.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

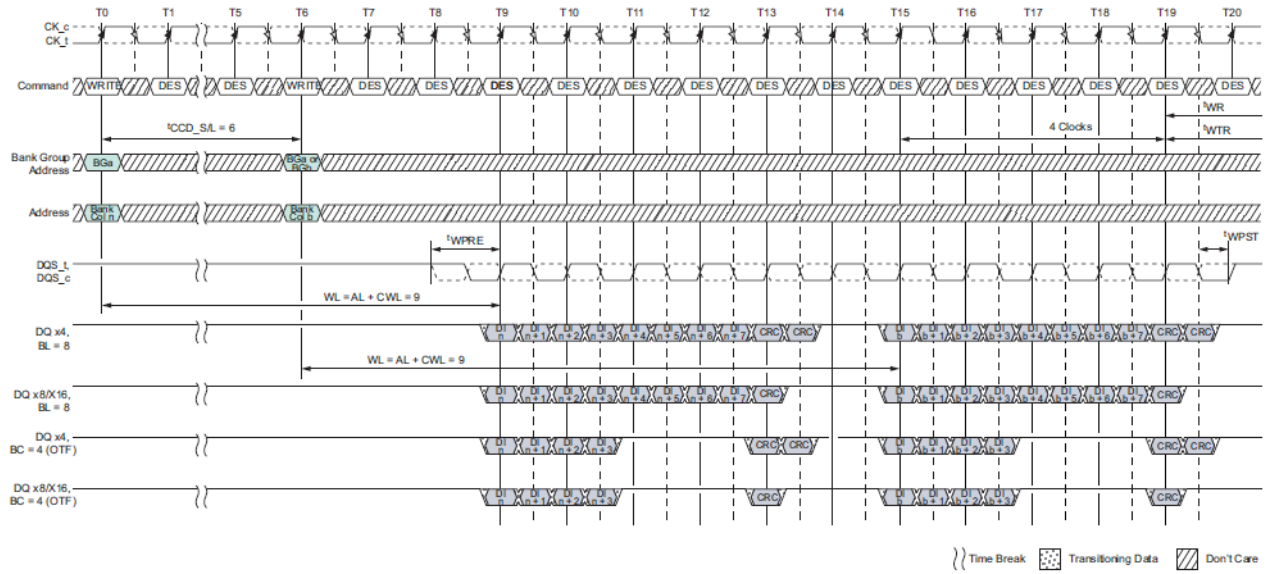
Figure 184. Consecutive WRITE (BC4-Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



Note:

1. BC4-fixed, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10 during WRITE commands at T0 and T5.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T16.

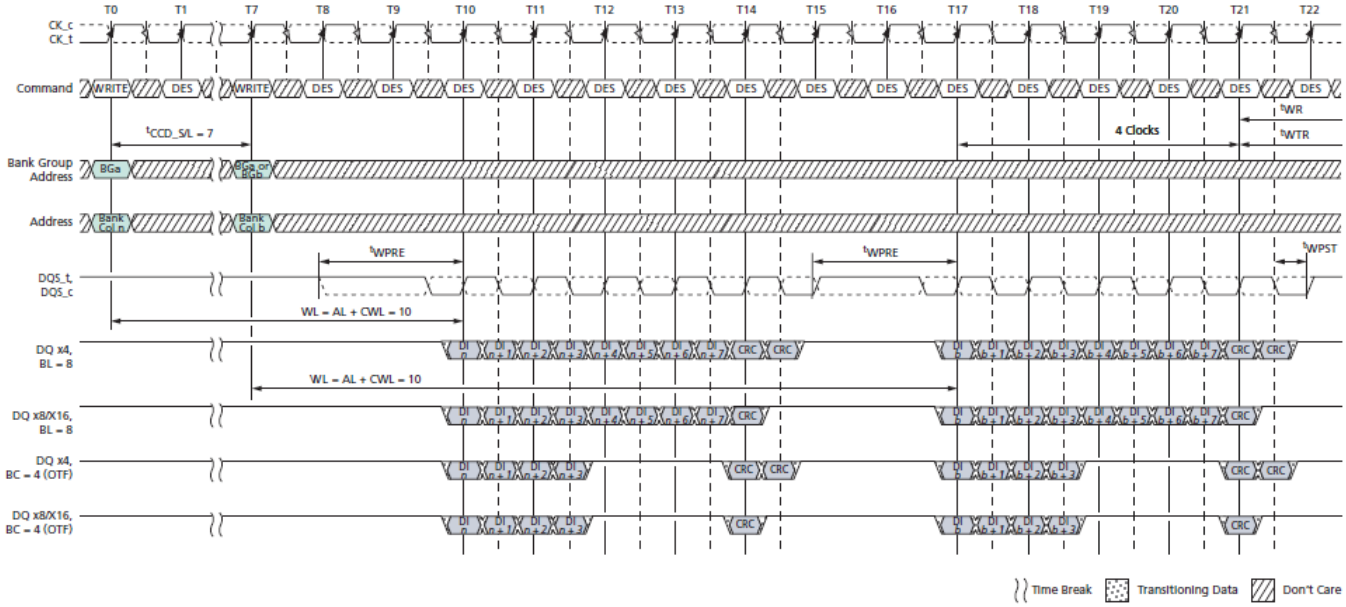
Figure 185. Nonconsecutive WRITE (BL8/BC4-OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



Note:

1. BL8/BC4-OTF, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 6tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T6.
5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T6.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Disable.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T19.

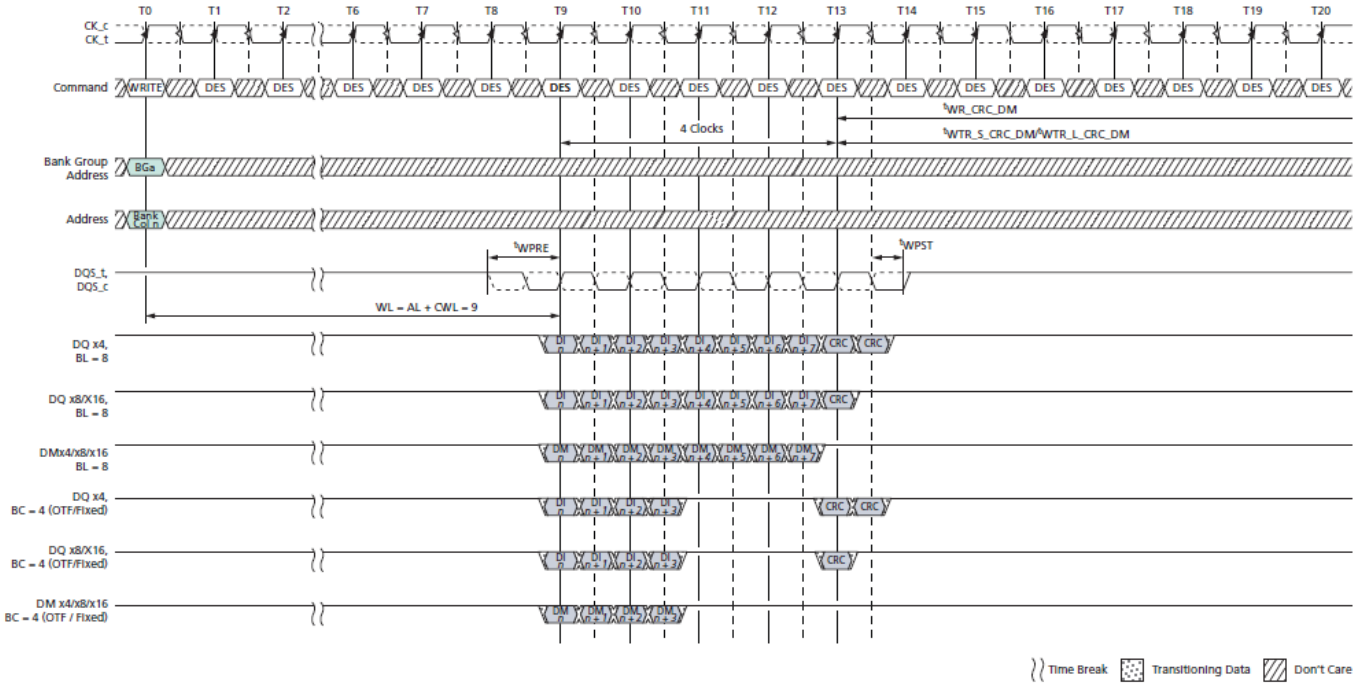
Figure 186. Nonconsecutive WRITE (BL8/BC4-OTF) with 2tCK Preamble and Write CRC in Same or Different Bank Group



Note:

1. BL8/BC4-OTF, AL = 0, CWL = 9 + 1 = 10 (see Note 9), Preamble = 2tCK, tCCD_S/L = 7tCK (see Note 7).
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T7.
5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T7.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Disable.
7. tCCD_S/L = 6tCK is not allowed in 2tCK preamble mode if minimum tCCD_S/L allowed in 1tCK preamble mode would have been 6 clocks.
8. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.
9. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK WRITE preamble mode.

Figure 187. WRITE (BL8/BC4-OTF/Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



Note:

1. BL8/BC4, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during WRITE command at T0.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Enable.
7. The write recovery time (tWR_CRC_DM) and write timing parameter (tWTR_S_CRC_DM/tWTR_L_CRC_DM) are referenced from the first rising clock edge after the last write data shown at T13.

Write Timing Violations

Motivation

Generally, if Write timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the DRAM works properly. However, it is desirable, for certain violations as specified below, the DRAM is guaranteed to not "hang up," and that errors are limited to that particular operation.

For the following, it will be assumed that there are no timing violations with regards to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

Data Setup and Hold Offset Violations

Should the data to strobe timing requirements (Tdqs_off, Tdqh_off, Tdqs_dd_off, Tdqh_dd_off) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory locations addressed with this WRITE command. In the example (Figure), the relevant strobe edges for write burst A are associated with the clock edges: T5, T5.5, T6, T6.5, T7, T7.5, T8, and T8.5.

Subsequent reads from that location might results in unpredictable read data, however the DRAM will work properly otherwise.

Strobe and Strobe to Clock Timing Violations

Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise with the following constraints:

- Both Write CRC and data burst OTF are disabled; timing specifications other than tDQSH, tDQSL, tWPRE, tWPST, tDSS, tDSH, tDQSS are not violated.
- The offending write strobe (and preamble) arrive no earlier or later than six DQS transition edges from the Write-Latency position.
- A Read command following an offending Write command from any open bank is allowed.
- One or more subsequent WR or a subsequent WRA {to same bank as offending WR} may be issued tCCD_L later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending Writes. Reads from these Writes may provide incorrect data.
- One or more subsequent WR or a subsequent WRA {to a different bank group} may be issued tCCD_S later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending Writes. Reads from these Writes may provide incorrect data.
- Once one or more precharge commands (PRE or PREA) are issued to DDR4 after offending WRITE command and all banks become precharged state (idle state), a subsequent, non-offending WR or WRA to any open bank shall be able to write correct data.

ZQ Calibration Commands

ZQ Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron & ODT values. DDR4 SDRAM needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and, once calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM IO, which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET are allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 128 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other applicationspecific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

Where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdriftrate = 1 °C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

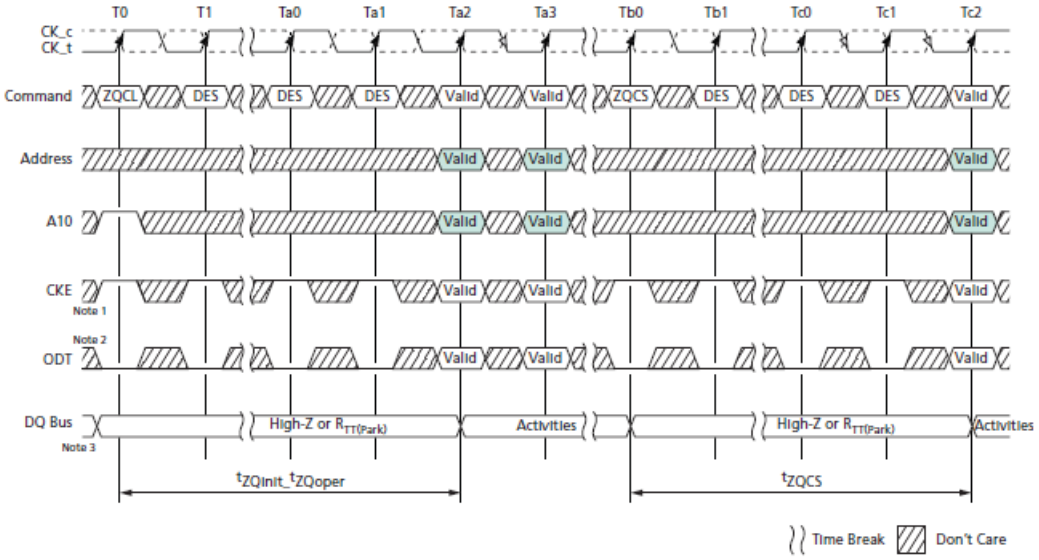
No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller. See"Command Truth Table"for a description of the ZQCL and ZQCS commands.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon Self-Refresh exit, DDR4 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is tXS, tXS_Abort/ tXS_FAST depending on operation mode.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between the devices.

Figure 188. ZQ Calibration Timing



Note:

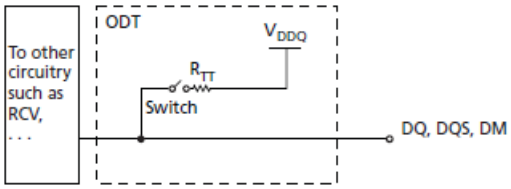
1. CKE must be continuously registered high during the calibration procedure.
2. During ZQ Calibration, ODT signal must be held LOW and DRAM continues to provide RTT_PARK.
3. All devices connected to the DQ bus should be high impedance or RTT_PARK during the calibration procedure.

On-Die Termination

ODT (On-Die Termination) is a feature of the DDR4 SDRAM that allows the DRAM to change termination resistance for each DQ, DQS_t, DQS_c and DM_n for x4 and x8 configuration (and TDQS_t, TDQS_c for X8 configuration, when enabled via A11=1 in MR1) via the ODT control pin or Write Command or Default Parking value with MR setting. For x16 configuration, ODT is applied to each DQU, DQL, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n and DML_n signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document.

The ODT feature is turned off and not supported in Self-Refresh mode. A simple functional representation of the DRAM ODT feature is shown in Functional Representation of ODT Figure.

Figure 189. Functional Representation of ODT



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and Mode Register Setting and other control information, see below. The value of RTT is determined by the settings of Mode Register bits (see Section Mode Register). The ODT pin will be ignored if the Mode Registers MR1 is programmed to disable RTT_NOM (MR1{A10,A9,A8}={0,0,0}) and in self-refresh mode.

ODT Mode Register and ODT State Table

The ODT Mode of DDR4 SDRAM has 4 states, Data Termination Disable, RTT_WR, RTT_NOM and RTT_PARK. And the ODT Mode is enabled if any of MR1 {A10,A9,A8} or MR2 {A10:A9} or MR5 {A8:A6} are non zero. In this case, the value of RTT is determined by the settings of those bits.

RTT control of each RTT condition is possible with a WR or RD command and ODT pin.

- RTT(WR): The DRAM (rank) that is being written to provide termination regardless of ODT pin status (either HIGH or LOW).
- RTT(NOM): DRAM turns ON RTT(NOM) if it sees ODT asserted HIGH (except when ODT is disabled by MR1).
- RTT(Park): Default parked value set via MR5 to be enabled and RTT(NOM) is not turned on.
- The Termination State Table that follows shows various interactions.

The RTT values have the following priority:

- Data termination disable
- RTT(WR)
- RTT(NOM)
- RTT(Park)

Table 63. Termination State Table

Case	RTT(Park)	RTT(NOM) *1	RTT(WR) *2	ODT Pin	ODT READS *3	ODT Standby *7	ODT WRITES
A[4]	Disabled	Disabled	Disabled	Don't Care	Off (High-Z)	Off (High-Z)	Off (High-Z)
			Enabled	Don't Care	Off (High-Z)	Off (High-Z)	RTT(WR)
B[5]	Enabled	Enabled	Disabled	Don't Care	Off (High-Z)	RTT(Park)	RTT(Park)
			Enabled	Don't Care	Off (High-Z)	RTT(Park)	RTT(WR)
C[6]	Disabled	Disabled	Disabled	Low	Off (High-Z)	Off (High-Z)	Off (High-Z)
				High	Off (High-Z)	RTT(NOM)	RTT(NOM)
			Enabled	Low	Off (High-Z)	Off (High-Z)	RTT(WR)
				High	Off (High-Z)	RTT(NOM)	RTT(WR)
C[6]	Enabled	Enabled	Disabled	Low	Off (High-Z)	RTT(Park)	RTT(Park)
				High	Off (High-Z)	RTT(NOM)	RTT(NOM)
			Enabled	Low	Off (High-Z)	RTT(Park)	RTT(WR)
				High	Off (High-Z)	RTT(NOM)	RTT(WR)

Note:

1. If RTT(NOM) MR is disabled, power to the ODT receiver will be turned off to save power.
2. If RTT(WR) is enabled, RTT(WR) will be activated by a WRITE command for a defined period time independent of the ODT pin and MR setting of RTT(Park)/RTT(NOM). This is described in the Dynamic ODT section.
3. When a READ command is executed, the DRAM termination state will be High-Z for a defined period independent of the ODT pin and MR setting of RTT(Park)/RTT(NOM). This is described in the ODT During Read section.
4. Case A is generally best for single-rank memories.
5. Case B is generally best for dual-rank, single-slotted memories.
6. Case C and Case D are generally best for multi-slotted memories.
7. The ODT feature is turned off and not supported in self refresh mode.

ODT Read Disable State Table

Upon receiving a READ command, the DRAM driving data disables ODT after RL - (2 or 3) clock cycles, where 2 = 1tCK preamble mode and 3 = 2tCK preamble mode. ODT stays off for a duration of BL/2 + (2 or 3) + (0 or 1) clock cycles, where 2 = 1tCK preamble mode, 3 = 2tCK preamble mode, 0 = CRC disabled, and 1 = CRC enabled.

Table 64. Read Termination Disable Window

Preamble	CRC	Start ODT Disable After Read	Duration of ODT Disable
1tCK	Disabled	RL - 2	BL/2 + 2
	Enabled	RL - 2	BL/2 + 3
2tCK	Disabled	RL - 3	BL/2 + 3
	Enabled	RL - 3	BL/2 + 4

Synchronous ODT Mode

Synchronous ODT Mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode
- Precharge power down mode

In synchronous ODT mode, RTT(NOM) will be turned on DODTLon clock cycles after ODT is sampled HIGH by a rising clock edge and turned off DODTLoff clock cycles after ODT is registered LOW by a rising clock edge. The ODT latency is determined by the programmed values for: CAS WRITE latency (CWL), additive latency (AL), and parity latency (PL), as well as the programmed state of the preamble.

ODT Latency and Posted ODT

The ODT latencies for synchronous ODT mode are summarized in the table below. For details, refer to the latency definitions.

Table 65. ODT Latency at DDR4-1600/-1866/-2133/-2400/-2666/-3200

Applicable when write CRC is disabled

Symbol	Parameter	1tck Preamble	2tck Preamble	Unit
DODTLon	Direct ODT turn on Latency	CWL + AL + PL - 2	CWL + AL + PL – 3	tCK
DODTLoff	Direct ODT turn off Latency	CWL + AL + PL - 2	CWL + AL + PL - 3	
RODTLoff	Read command to internal ODT turn off Latency	CL+AL+PL-2	CL+AL+PL-3	
RODTLon4	Read command to RTT_PARK turn on Latency in BC4	RODTLoff +4	RODTLoff +5	
RODTLon8	Read command to RTT_PARK turn on Latency in BC8/BL8	RODTLoff +6	RODTLoff +7	
ODTH4	ODT Assertion time, BC4 mode	4	5	
ODTH8	ODT Assertion time, BL8 mode	6	7	

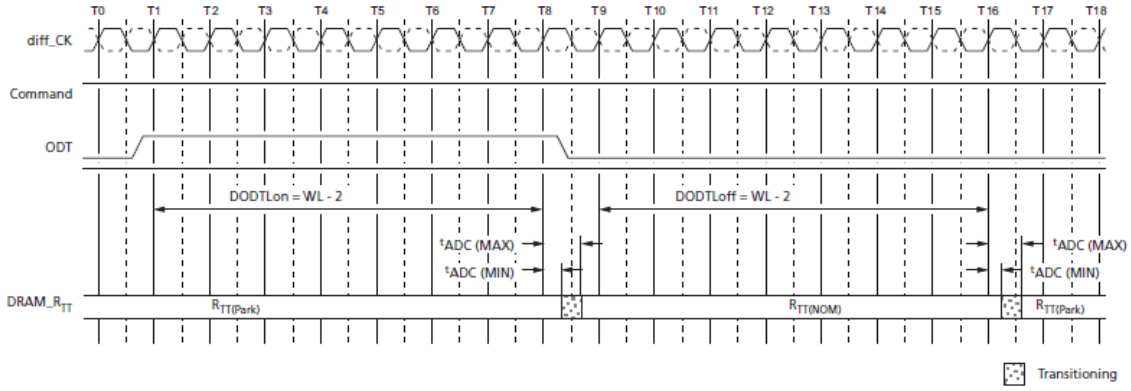
Timing Parameters

In synchronous ODT mode, the following timing parameters apply:

- DODTLon, DODTLoff, RODTLoff, RODTLon4, RODTLon8, tADC,min,max.
- tADC,min and tADC,max are minimum and maximum RTT change timing skew between different termination values. Those timing parameters apply to both the Synchronous ODT mode and the Data Termination Disable mode.

When ODT is asserted, it must remain HIGH until minimum ODTH4 (BC = 4) or ODTH8 (BL = 8) is satisfied. If write CRC mode or 2tCK preamble mode is enabled, ODTH should be adjusted to account for it. ODTH*x* is measured from ODT first registered HIGH to ODT first registered LOW or from the registration of a WRITE command.

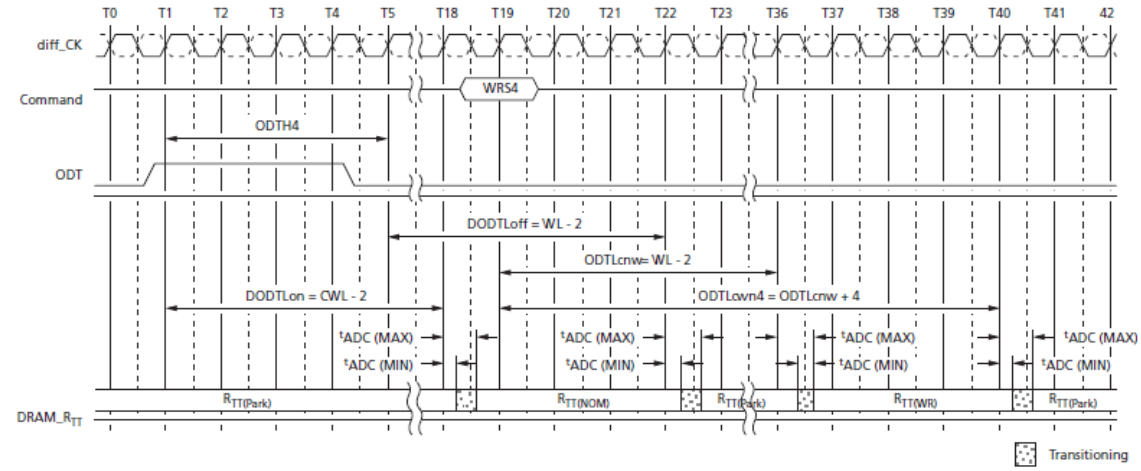
Figure 190. Synchronous ODT Timing with BL8



Note:

1. Example for CWL = 9, AL = 0, PL = 0; DODTLon = AL + PL + CWL - 2 = 7; DODTLoff = AL + PL + CWL - 2 = 7.
2. ODT must be held HIGH for at least ODTH8 after assertion (T1).

Figure 191. Synchronous ODT Timing with BC4



Note:

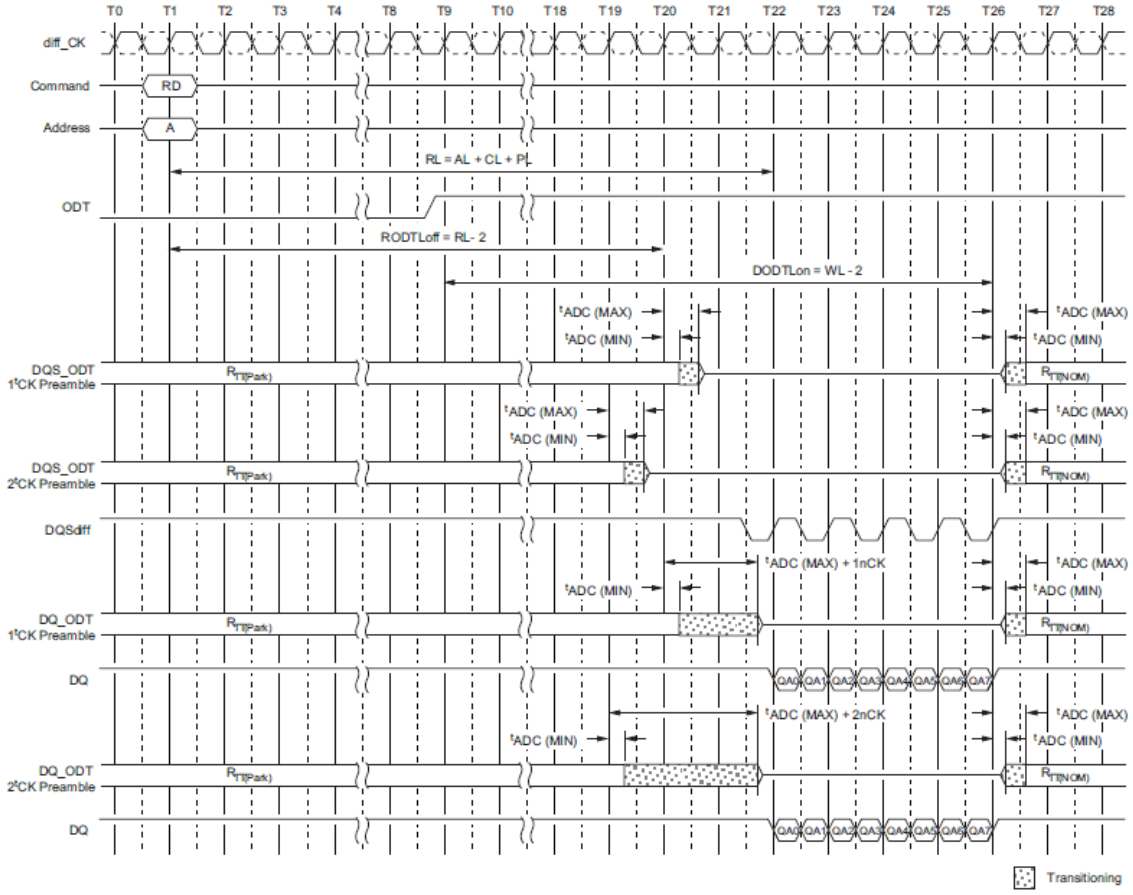
1. Example for CWL = 9, AL = 10, PL = 0; DODTLon/off = AL + PL+ CWL - 2 = 17; ODTcnw = AL + PL+ CWL - 2 = 17.
2. ODT must be held HIGH for at least ODTH4 after assertion (T1).

ODT During Reads

Because the DRAM cannot terminate with RTT and drive with RON at the same time, RTT may nominally not be enabled until the end of the postamble as shown in the example below. At cycle T26 the device turns on the termination when it stops driving, which is determined by tHZ. If the DRAM stops driving early (that is, tHZ is early), thentADC (MIN) timing may apply. If the DRAM stops driving late (that is, tHZ is late), then the DRAM complies with tADC (MAX) timing.

Using CL = 11 as an example for the figure below: PL = 0, AL = CL - 1 = 10, RL = PL + AL + CL = 21, CWL= 9; RODTLoff = RL - 2 = 19, DODTLon = PL + AL + CWL - 2 = 17, 1tCK preamble.

Figure 192. ODT During Reads



Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR4 SDRAM can be changed without issuing an MRS command. This requirement is supported by the "Dynamic ODT" feature as described as follows:

Functional Description

The Dynamic ODT Mode is enabled if bit A[9] or A[10] of MR2 is set to '1'. The function is described as follows:

- Three RTT values are available: RTT_NOM, RTT_PARK and RTT_WR.
  - The value for RTT_NOM is preselected via bits A[10:8] in MR1
  - The value for RTT_PARK is preselected via bits A[8:6] in MR5
  - The value for RTT_WR is preselected via bits A[11:9] in MR2
- During operation without commands, the termination is controlled as follows;
  - Nominal termination strength RTT_NOM or RTT_PARK is selected.
  - RTT_NOM on/off timing is controlled via ODT pin and latencies DODTLon and DODTLoff and RTT_PARK is on when ODT is LOW.
- When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
  - latency ODTLcnw after the write command, termination strength RTT_WR is selected.
  - latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_WR is de-selected.

One or two clocks will be added into or subtracted from ODTLcwn8 and ODTLcwn4, depending on write CRC mode and/or 2tCK preamble enablement.

The following table shows latencies and timing parameters relevant to the on-die termination control in dynamic ODT mode. The dynamic ODT feature is not supported in DLL-off mode. An MRS command must be used to set RTT(WR) to disable dynamic ODT externally (MR2[11:9] = 000).

Table 66. Dynamic ODT Latencies and Timing (1tCK Preamble Mode and CRC Disabled)

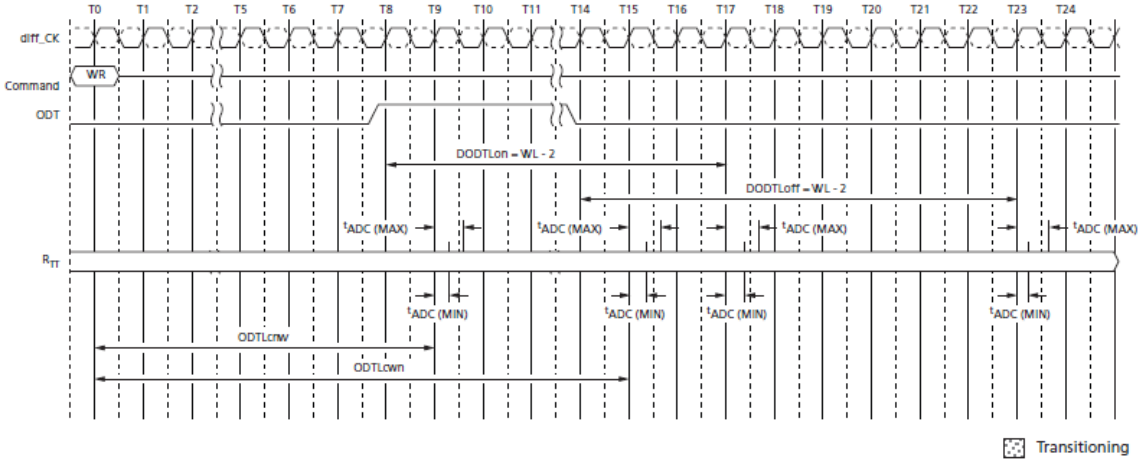
Name and Description	Abbr.	Defined from	Defined to	1600/1866/ 2133/2400	2666	2933/3200	Unit
ODT latency for change from $R_{TT(Park)}$/$R_{TT(NOM)}$ to $R_{TT(WR)}$	ODTLcnw	Registering external WRITE command	Change R_{TT} strength from $R_{TT(Park)}$/$R_{TT(NOM)}$ to $R_{TT(WR)}$	ODTLcnw = WL - 2			^{t}CK
ODT latency for change from $R_{TT(WR)}$ to $R_{TT(Park)}$/$R_{TT(NOM)}$ (BC = 4)	ODTLcwn4	Registering external WRITE command	Change R_{TT} strength from $R_{TT(WR)}$ to $R_{TT(Park)}$/$R_{TT(NOM)}$	ODTLcwn4 = 4 + ODTLcnw			^{t}CK
ODT latency for change from $R_{TT(WR)}$ to $R_{TT(Park)}$/$R_{TT(NOM)}$) (BL = 8)	ODTLcwn8	Registering external WRITE command	Change R_{TT} strength from $R_{TT(NOM)}$ to $R_{TT(WR)}$	ODTLcwn8 = 6 + ODTLcnw			^{t}CK (AVG)
R_{TT} change skew	^{t}ADC	ODTLcnw ODTLcwn	R_{TT} valid	^{t}ADC (MIN) = 0.30 ^{t}ADC (MAX) = 0.70	^{t}ADC (MIN) = 0.28 ^{t}ADC (MAX) = 0.72	^{t}ADC (MIN) = 0.26 ^{t}ADC (MAX) = 0.74	^{t}CK (AVG)

Table 67. Dynamic ODT Latencies and Timing with Preamble Mode and CRC Mode Matrix

Symbol	1tck Preamble		2tck Preamble		Unit
	CRC Off	CRC On	CRC Off	CRC On	
ODTLcnw *1	WL - 2	WL - 2	WL - 3	WL - 3	tCK
ODTLcwn4	ODTLcnw + 4	O DTLcnw + 7	ODTLcnw + 5	O DTLcnw + 8	
ODTLcwn8	ODTLcnw + 6	O DTLcnw + 7	ODTLcnw + 7	O DTLcnw + 8	

Notes: 1. ODTLcnw = WL - 2 (1tCK preamble) or WL - 3 (2tCK preamble).

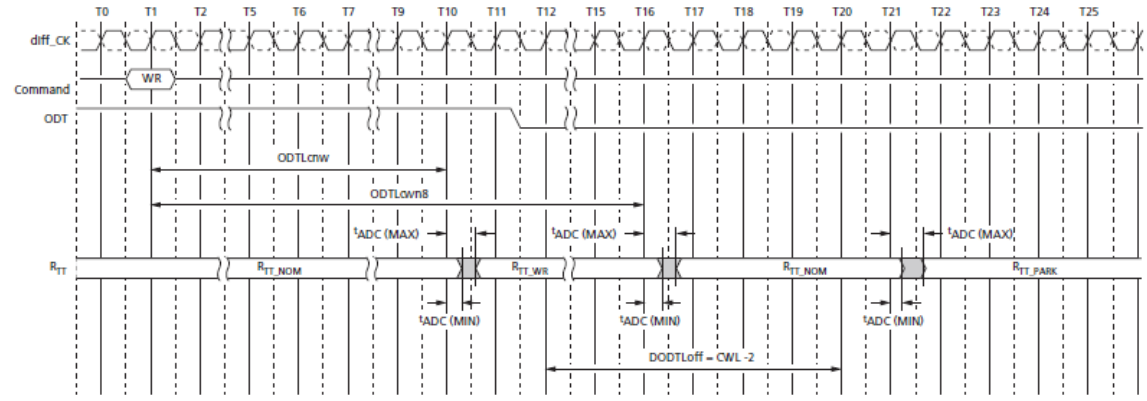
Figure 193. Dynamic ODT (1tCK Preamble; CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled)



Note:

1. ODTLcnw = WL - 2 (1tCK preamble) or WL - 3 (2tCK preamble).
2. If BC4, then ODTLcwn = WL + 4 if CRC disabled or WL + 5 if CRC enabled; If BL8, then ODTLcwn = WL + 6 if CRC disabled or WL + 7 if CRC enabled.

Figure 194. Dynamic ODT Overlapped with $R_{TT(NOM)}$ (CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled)



Note: 1. Behavior with WR command issued while ODT is registered HIGH.

Asynchronous ODT mode

Asynchronous ODT mode is selected when DLL is disabled by MR1 bit A0='0'b.

In asynchronous ODT timing mode, internal ODT command is not delayed by either the Additive latency (AL) or relative to the external ODT signal (RTT_NOM). In asynchronous ODT mode, the following timing parameters apply tAONAS,min, max, tAOFAS,min,max.

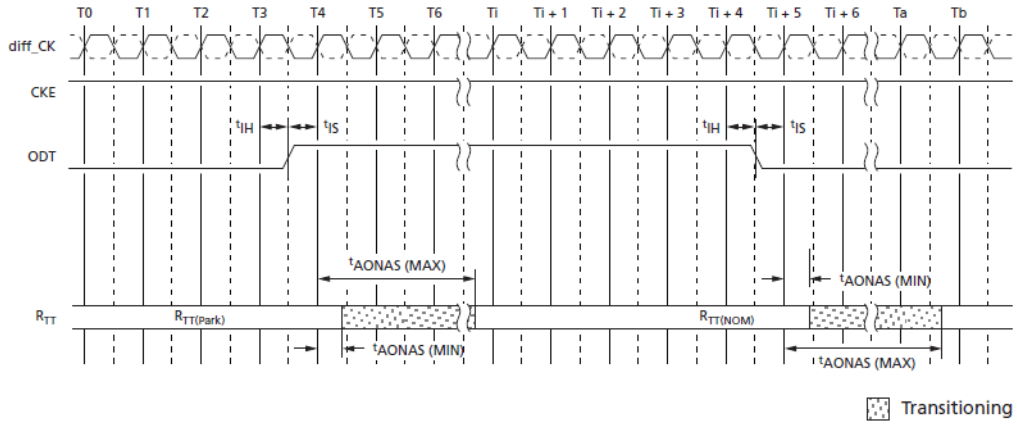
RTT(NOM) Turn-on Time

- Minimum RTT_NOM turn-on time (tAONASmin) is the point in time when the device termination circuit leaves RTT_PARK and ODT resistance begins to change.
- Maximum RTT_NOM turn on time(tAONASmax) is the point in time when the ODT resistance is reached RTT_NOM.
- tAONASmin and tAONASmax are measured from ODT being sampled high.

RTT(NOM) Turn-off Time

- Minimum RTT_NOM turn-off time (tAOFASmin) is the point in time when the devices termination circuit starts to leave
- RTT_NOM. Maximum RTT_NOM turn-off time (tAOFASmax) is the point in time when the on-die termination has reachedRTT_PARK.
- tAOFASmin and tAOFASmax are measured from ODT being sampled low.

Figure 195. Asynchronous ODT Timing with DLL-off



Electrical Specifications

Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability. Although "unlimited" row accesses to the same row is allowed within the refresh period; excessive row accesses to the same row over a long term can result in degraded operation.

Table 68. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Note
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4 ~ 1.5	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4 ~ 1.5	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	-0.4 ~ 3.0	V	3
V_{IN}, V_{OUT}	Voltage on any pin except V_{REFCA} relative to V_{SS}	-0.4 ~ 1.5	V	
T_{STG}	Storage Temperature	-55 to +150	°C	2

Note:

1. V_{DD} and V_{DDQ} must be within 300 mV of each other at all times; and V_{REFCA} must be not greater than 0.6 x V_{DDQ}, When V_{DD} and V_{DDQ} are less than 500 mV; V_{REFCA} may be equal to or less than 300 mV.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{PP} must be equal or greater than V_{DD}/V_{DDQ} at all times when powered.

DRAM Component Operating Temperature Range

Operating temperature, T_{OPER}, is the case surface temperature on the center/top side of the DRAM. For measurement conditions, refer to the JEDEC document JESD51-2.

Table 69. Temperature Ranges

Symbol	Parameter	Min	Max	Unit	Notes
T_{OPER}	Normal operating temperature range	0	85	°C	1
	Extended temperature range (optional)	>85	95	°C	2

Note:

1. The normal temperature range specifies the temperatures at which all DRAM specifications will be supported.
   During operation, the DRAM case temperature must be maintained between 0°C to 85°C under all operating conditions for the commercial offering.
2. Some applications require operation of the commercial, industrial, and automotive temperature DRAMs in the extended temperature range (between 85°C and 95°C case temperature). Full specifications are supported in this range, but the following additional conditions apply:
   - Refer to tREFI and tRFC parameters table for tREFI requirements when operating above 85°C
   - If SELF REFRESH operation is required in the extended temperature range, it is mandatory to use either the manual self refresh mode with extended temperature range capability (MR2[6] = 0 and MR2 [7] = 1) or enable the optional auto self refresh mode (MR2 [6] = 1 and MR2 [7] = 1).

AC and DC Operating Conditions

Table 70. Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	Note
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1,2,3,4,5
V_{DDQ}	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,6
V_{PP}	Wordline supply voltage	2.375	2.5	2.75	V	7

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. VDD slew rate between 300mV and 80% of VDD,min shall be between 0.004 V/ms and 600 V/ms, 20 MHz band-limited measurement.
4. VDD ramp time from 300mV to VDD,min shall be no longer than 200ms.
5. A stable valid VDD level is a set DC level (0 Hz to 250 KHz) and must be no less than VDD,min and no greater than VDD,max. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is final. AC noise of ±60mV (greater than 250 KHz) is allowed on VDD provided the noise doesn't alter VDD to less than VDD,min or greater than VDD,max.
6. A stable valid VDDQ level is a set DC level (0 Hz to 250 KHz) and must be no less than VDDQ,min and no greater than VDDQ,max. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is final. AC noise of 60mV (greater than 250 KHz) is allowed on VDDQ provided the noise doesn't alter VDDQ to less than VDDQ,min or greater than VDDQ,max.
7. A stable valid VPP level is a set DC level (0 Hz to 250 KHz) and must be no less than VPP,min and no greater than VPP,max. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is final. AC noise of ±120mV (greater than 250 KHz) is allowed on VPP provided the noise doesn't alter VPP to less than VPP,min or greater than VPP,max.

Table 71. V_{DD} Slew Rate

Symbol	Min.	Max.	Unit	Note
V_{DD}	0.004	600	V/ms	1,2
V_{PP}	-	200	ms	3

Note:

1. Measurement made between 300mV and 80% V_{DD} (minimum level).
2. The DC bandwidth is limited to 20 MHz.
3. Maximum time to ramp VDD from 300 mV to V_{DD} minimum.

Leakages

Table 72. Leakages

Condition	Symbol	Min.	Max.	Unit	Note
Input leakage (excluding ZQ and TEN)	I_{IN}	-2	2	µA	1
ZQ leakage	I_{ZQ}	-50	10	µA	1
TEN leakage	I_{TEN}	-6	10	µA	1,2
VREFCA leakage	I_{VREFCA}	-2	2	µA	3
Output leakage: $V_{OUT} = V_{DDQ}$	I_{OZpd}	-	10	µA	4
Output leakage: $V_{OUT} = V_{SSQ}$	I_{OZpu}	-50	-	µA	4,5

Note:

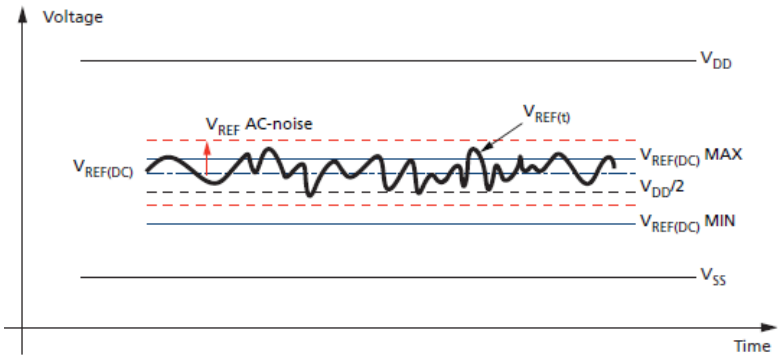
1. Input under test $0V < V_{IN} < 1.1V$.
2. Additional leakage due to weak pull-down.
3. $V_{REFCA} = V_{DD}/2$, V_{DD} at valid level after initialization.
4. DQs are disabled.
5. ODT is disabled with the ODT input HIGH.

V_{REFCA} Supply

V_{REFCA} is to be supplied to the DRAM and equal to $V_{DD}/2$. The V_{REFCA} is a reference supply input and therefore does not draw biasing current.

The DC-tolerance limits and AC-noise limits for the reference voltages V_{REFCA} are illustrated in the figure below. The figure shows a valid reference voltage $V_{REF(t)}$ as a function of time (V_{REF} stands for V_{REFCA}). $V_{REF(DC)}$ is the linear average of $V_{REF(t)}$ over a very long period of time (1 second). This average has to meet the MIN/MAX requirements. Furthermore, $V_{REF(t)}$ may temporarily deviate from $V_{REF(DC)}$ by no more than ±1% V_{DD} for the AC-noise limit.

Figure 196. V_{REFDQ} Voltage Range



The voltage levels for setup and hold time measurements are dependent on VREF. VREF is understood as VREF(DC), as defined in the above figure. This clarifies that DC-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid HIGH or LOW level, and therefore, the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals. This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VREF AC-noise. Timing and voltage effects due to AC-noise on VREF up to the specified limit (±1% of VDD) are included in DRAM timings and their associated deratings.

V_{REFDQ} Supply and Calibration Ranges

The device internally generates its own VREFDQ. DRAM internal VREFDQ specification parameters: voltage range, step size, VREF step time, VREF full step time, and VREF valid level are used to help provide estimated values for the internal VREFDQ and are not pass/fail limits. The voltage operating range specifies the minimum required range for DDR4 SDRAM devices. The minimum range is defined by VREFDQ,min and VREFDQ,max. A calibration sequence should be performed by the DRAM controller to adjust VREFDQ and optimize the timing and voltage margin of the DRAM data input receivers.

Table 73. V_{REFDQ} Specification

Parameter	Symbol	Min.	Max.	Typ.	Unit	Notes
Range 1 V_{REFDQ} operating points	V_{REFDQ} R1	60%	-	92%	V_{DDQ}	1, 2
Range 2 V_{REFDQ} operating points	V_{REFDQ} R2	45%	-	77%	V_{DDQ}	1, 2
V_{REF} step size	$V_{REF,step}$	0.5%	0.65%	0.8%	V_{DDQ}	3
V_{REF} set tolerance	V_{REF,set_tol}	-1.625%	0%	1.625%	V_{DDQ}	4, 5, 6
		-0.15%	0%	0.15%	V_{DDQ}	4, 7, 8
V_{REF} step time	$V_{REF,time}$	-	-	150	ns	9, 10, 11
V_{REF} valid tolerance	$V_{REF\_val\_tol}$	-0.15%	0%	0.15%	V_{DDQ}	12

Note:

1. VREF(DC) voltage is referenced to VDDQ(DC). VDDQ(DC) is 1.2V.
2. DRAM range 1 or range 2 is set by the MRS6[6]6.
3. VREF step size increment/decrement range. VREF at DC level.
4. VREF,new = VREF,old ±n x VREF,step. If increment, use "+," if decrement, use "-."
5. For n >4, the minimum value of VREF setting tolerance = VREF,new - 1.625% x VDDQ. The maximum value of VREF setting tolerance = VREF,new + 1.625% x VDDQ.
6. Measured by recording the MIN and MAX values of the VREF output over the range, drawing a straight line between those points, and comparing all other VREF output settings to that line.
7. For n ≤4, the minimum value of VREF setting tolerance = VREF,new - 0.15% VDDQ. The maximum value of VREF setting tolerance = VREF,new + 0.15% x VDDQ.
8. Measured by recording the MIN and MAX values of the VREF output across four consecutive steps (n = 4), drawing a straight line between those points, and comparing all VREF output settings to that line.
9. Time from MRS command to increment or decrement one step size for VREF.
10. Time from MRS command to increment or decrement more than one step size up to the full range of VREF.
11. If the VREF monitor is enabled, VREF must be derated by +10ns if DQ bus load is 0pF and an additional +15 ns/pF of DQ bus loading.
12. Only applicable for DRAM component-level test/characterization purposes. Not applicable for normal mode of operation. VREF valid qualifies the step times, which will be characterized at the component level.

V_{REFDQ} Ranges

MR6[6] selects range 1 (60% to 92.5% of VDDQ) or range 2 (45% to 77.5% of VDDQ), and MR6[5:0] sets the VREFDQ level, as listed in the following table. The values in MR6[6:0] will update the VDDQ range and level independent of MR6[7] setting. It is recommended MR6[7] be enabled when changing the settings in MR6[6:0], and it is highly recommended MR6[7] be enabled when changing the settings in MR6[6:0] multiple times during a calibration routine.

Table 74. V_{REFDQ} Ranges and Levels

MR6[5:0]	Range 1 MR6[6] 0 = Range 1	Range 2 MR6[6] 1 = Range 2	MR6[5:0]	Range 1 MR6[6] 0 = Range 1	Range 2 MR6[6] 1 = Range 2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111 = Reserved		

RESET_n Input Levels

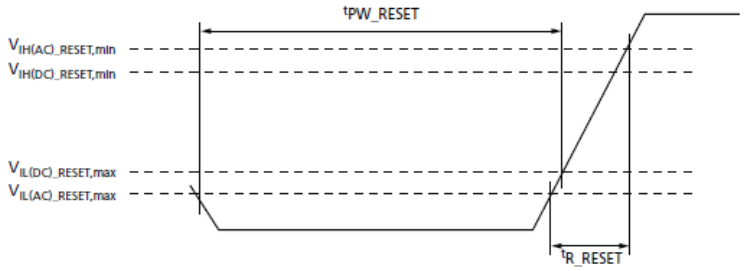
Table 75. RESET_n Input Levels (CMOS)

Parameter	Symbol	Min	Max	Unit	Note
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	1
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	3
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	4
Rising time	tR_RESET	-	1	us	5
RESET pulse width after power-up	tPW_RESET_S	1	-	us	6,7
RESET pulse width during power-up	tPW_RESET_L	200	-	us	6

Note:

1. Overshoot should not exceed the VIN shown in the Absolute Maximum Ratings table.
2. After RESET_n is registered HIGH, the RESET_n level must be maintained above VIH(DC)_RESET, otherwise operation will be uncertain until it is reset by asserting RESET_n signal LOW.
3. After RESET_n is registered LOW, the RESET_n level must be maintained below VIL(DC)_RESET during tPW_RESET, otherwise the DRAM may not be reset.
4. Undershoot should not exceed the VIN shown in the Absolute Maximum Ratings table.
5. Slope reversal (ring-back) during this level transition from LOW to HIGH should be mitigated as much as possible.
6. RESET is destructive to data contents.
7. See RESET Procedure at Power Stable Condition figure.

Figure 197. RESET_n Input Slew Rate Definition



Command/Address Input Levels

Table 76. Command and Address Input Levels: DDR4-2666 Through DDR4-3200

Parameter	Symbol	Min	Max	Unit	Note
AC Input High Voltage	VIH(AC)	VREF + 90	VDD [*5]	mV	1,2,3
DC Input High Voltage	VIH(DC)	VREF + 65	VDD	mV	1,2
DC Input Low Voltage	VIL(DC)	VSS	VREF - 65	mV	1,2
AC Input Low Voltage	VIL(AC)	VSS [*5]	VREF - 90	mV	1,2,3
Reference voltage for CMD/ADDR inputs	VREFFCA(DC)	0.49 x VDD	0.52 x VDD	V	4

Note:

1. For input except RESET_n. VREF = VREFCA(DC).
2. VREF = VREFCA(DC).
3. Input signal must meet VIL/VIH(AC) to meet tIS timings and VIL/VIH(DC) to meet tIH timings.
4. The AC peak noise on VREF may not allow VREF to deviate from VREFCA(DC) by more than ±1% VDD (for reference: approximately ±12mV).
5. Refer to “Overshoot and Undershoot Specifications.”

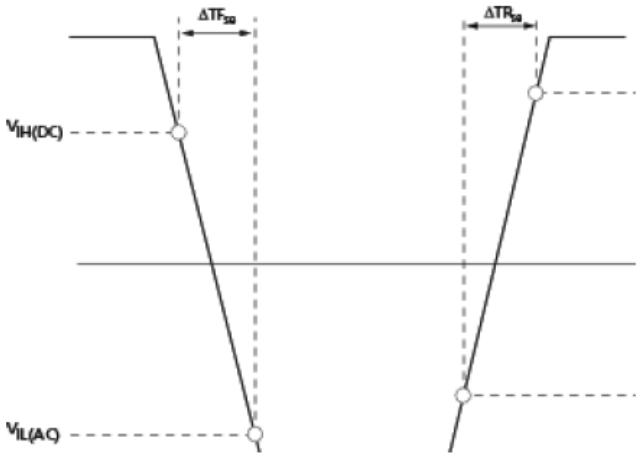
Table 77. Single-Ended Input Slew Rates

Parameter	Symbol	Min	Max	Unit	Note
Single-Ended Input Slew Rates-CA	SR_{CA}	1.0	7.0	V/ns	1,2,3,4

Note:

1. For input except RESET_n.
2. VREF = VREFCA(DC).
3. tIS/tIH timings assume SRCA = 1V/ns.
4. Measured between VIH(AC) and VIL(AC) for falling edges and between VIL(AC) and VIH(AC) for rising edges.

Figure 198. Single-Ended Input Slew Rate Definition



Command, Control, and Address Setup, Hold, and Derating

The total tIS (setup time) and tIH (hold time) required is calculated to account for slew rate variation by adding the data sheet tIS (base) values, the VIL(AC)/VIH(AC) points, and tIH (base) values, the VIL(DC)/VIH(DC) points; to the ΔtIS and ΔtIH derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2V/ns. Example: tIS (total setup time) = tIS (base) + ΔtIS. For a valid transition, the input signal has to remain above/below VIH(AC)/VIL(AC) for the time defined by tVAC.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH(AC)/ VIL(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH(AC)/ VIL(AC). For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)max that does not ring back above VIL(DC)max.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)min that does not ring back above VIL(DC)max.

Table 78. Command, Address, Control Setup and Hold Values – AC/DC-Based

Symbol	2666	3200	Unit	Reference
tIS(base, AC100)	-	-	ps	VIH/L(ac)
tIH(base, DC75)	-	-	ps	VIH/L(dc)
tIS(base, AC90)	55	40	ps	VIH/L(ac)
tIH(base, DC65)	80	65	ps	VIH/L(dc)
tIS/tIH @ VREF	145	130	ps	VIH/L(dc)

Table 79. Derating values for tIS/tIH – AC100/DC75-based

△tIS, △tIH derating in [ps] AC/DC based[1]																	
		CK_t, CK_c Differential Slew Rate															
		10.0V/ns		8.0V/ns		6.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1.0V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CMD, ADDR, CNTL Input Slew rate V/ns	7.0	76	54	76	55	77	56	79	58	82	60	86	64	94	73	111	89
	6.0	73	53	74	53	75	54	77	56	79	58	83	63	92	71	108	88
	5.0	70	50	71	51	72	52	74	54	76	56	80	60	88	68	105	85
	4.0	65	46	66	47	67	48	69	50	71	52	75	56	83	65	100	81
	3.0	57	40	57	41	58	42	60	44	63	46	67	50	75	58	92	75
	2.0	40	28	41	28	42	29	44	31	46	33	50	38	58	46	75	63
	1.5	23	15	24	16	25	17	27	19	29	21	33	25	42	33	58	50
	1.0	-10	-10	-9	-9	-8	-8	-6	-6	-4	-4	0	0	8	8	25	25
	0.9	-17	-14	-16	-14	-15	-13	-13	-10	-11	-8	-7	-4	1	4	18	21
	0.8	-26	-19	-25	-19	-24	-18	-22	-16	-20	-14	-16	-9	-7	-1	9	16
	0.7	-37	-26	-36	-25	-35	-24	-33	-22	-31	-20	-27	-16	-18	-8	-2	9
	0.6	-52	-35	-51	-34	-50	-33	-48	-31	-46	-29	-42	-25	-33	-17	-17	0
	0.5	-73	-48	-72	-47	-71	-46	-69	-44	-67	-42	-63	-38	-54	-29	-38	-13
	0.4	-104	-66	-103	-66	-102	-65	-100	-63	-98	-60	-94	-56	-85	-48	-69	-31
Note: 1. VIH/L(ac) = +/-tbd mV, VIH/L(dc) = +/- tbd mV; relative to VREFCA																	

Table 80. Derating values for tIS/tIH – AC90/DC65-based

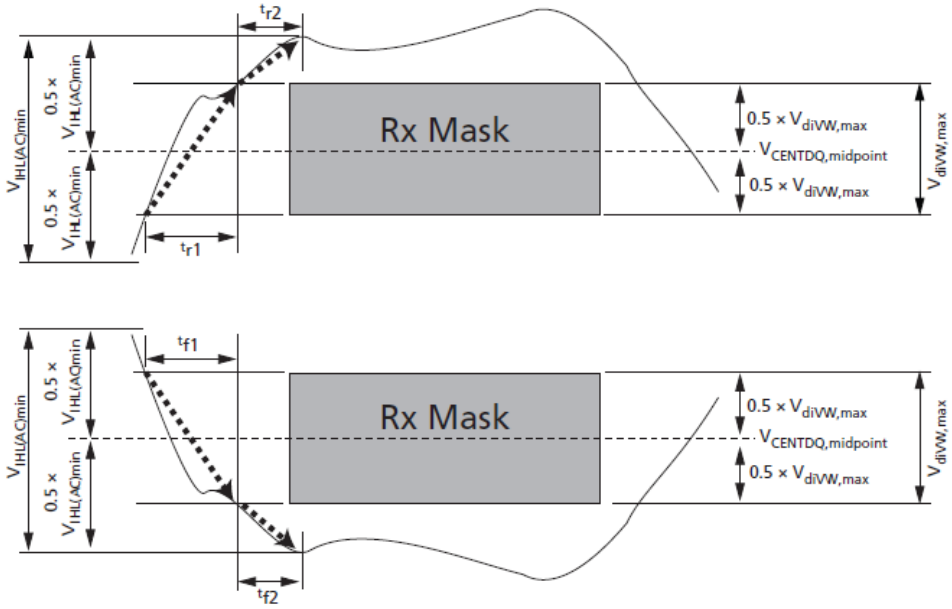
△tIS, △tIH derating in [ps] AC/DC based[1]																	
		CK_t, CK_c Differential Slew Rate															
		10.0V/ns		8.0V/ns		6.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1.0V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CMD, ADDR, CNTL Input Slew rate V/ns	7.0	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
	6.0	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
	5.0	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
	4.0	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
	3.0	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
	2.0	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
	1.5	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
	1.0	-9	-9	-8	-8	-8	-8	-6	-6	-4	-4	0	0	8	8	23	23
	0.9	-15	-13	-15	-12	-14	-11	-12	-9	-10	-7	-6	-4	1	4	16	19
	0.8	-23	-17	-23	-17	-22	-16	-20	-14	-18	-12	-14	-8	-7	-1	8	14
	0.7	-34	-23	-33	-22	-32	-21	-30	-20	-28	-18	-25	-14	-17	-6	-2	9
	0.6	-47	-31	-47	-30	-46	-29	-44	-27	-42	-25	-38	-22	-31	-14	-16	1
	0.5	-67	-42	-66	-41	-65	-40	-63	-38	-61	-36	-58	-33	-50	-25	-35	-10
	0.4	-95	-58	-95	-57	-94	-56	-92	-54	-90	-53	-86	-49	-79	-41	-64	-26
Note: 1. VIH/L(ac) = +/-tbd mV, VIH/L(dc) = +/- tbd mV; relative to VREFCA																	

Data Receiver Input Requirements

The following parameters apply to the data receiver Rx MASK operation detailed in the Write Timing section, Data Strobe-to-Data Relationship. The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in the figure below. A LOW-to-HIGH transition time, tr1, is measured from 0.5 x VdiVW,max below VCENTDQ,midpoint to the last transition through 0.5 VdiVW,max above VCENTDQ,midpoint; tr2 is measured from the last transition through 0.5 VdiVW,max above VCENTDQ,midpoint to the first transition through the 0.5 x VIHL(AC)min above VCENTDQ,midpoint.

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in the figure below. A HIGH-to-LOW transition time, tf1, is measured from 0.5 x VdiVW,max above VCENTDQ,midpoint to the last transition through 0.5 x VdiVW,max below VCENTDQ,midpoint; tf2 is measured from the last transition through 0.5 x VdiVW,max below VCENTDQ,midpoint to the first transition through the 0.5 x VIHL(AC)min below VCENTDQ,midpoint.

Figure 199. DQ Slew Rate Definitions



Note:

1. Rising edge slew rate equation srr1 = VdiVW,max/(tr1).
2. Rising edge slew rate equation srr2 = (VIHL(AC)min - VdiVW,max)/(2 x tr2).
3. Falling edge slew rate equation srf1 = VdiVW,max/(tf1).
4. Falling edge slew rate equation srf2 = (VIHL(AC)min - VdiVW,max)/(2 x tf2).

Table 81. DQ Input Receiver Specifications

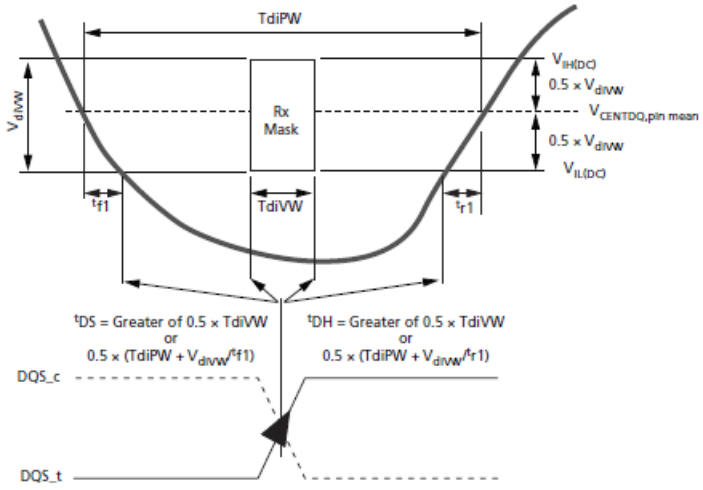
Symbol	Parameter	DDR4-2666		DDR4-3200		Unit	Note
		min	max	min	max		
VdIVW	Rx Mask voltage - pk-pk	-	120	-	110	mV	2,3
TdIVW	Rx timing window	-	0.22	-	0.23	UI	2,3
VIHL_AC	DQ AC input swing pk-pk	150	-	140	-	mV	4,5
TdIPW	DQ input pulse width	0.58	-	0.58	-	UI	6
tDQS2DQ	Rx Mask DQS to DQ offset	-0.19	0.19	-0.22	0.22	UI	7
tDQ2DQ	Rx Mask DQ to DQ offset	-	0.105	-	0.125	UI	8
srr1, srf1	Input Slew Rate over VdIVW if tCK >= 0.937ns	1	9	1	9	V/ns	9
	Input Slew Rate over VdIVW if 0.937ns > tCK >= 0.625ns	1.25	9	1.25	9	V/ns	9
srr2	Rising Input Slew Rate over 1/2 VIHL_AC	0.2*srr1	9	0.2* srr1	9	V/ns	10
srf2	Falling Input Slew Rate over 1/2 VIHL_AC	0.2*srf1	9	0.2* srr1	9	V/ns	10

Note:

1. All Rx mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiVW (MIN), VdiVW,max, and minimum slew rate limits, then either TdiVW (MIN) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.
2. Data Rx mask voltage and timing total input valid window where VdiVW is centered around VCENTDQ,midpoint after VREFDQ training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER =1e- 16 when the Rx mask is not violated.
3. Defined over the DQ internal VREF range 1.
4. Overshoot and undershoot specifications apply.
5. DQ input pulse signal swing into the receiver must meet or exceed VIHL(AC)min. VIHL(AC)min is to be achieved on an UI basis when a rising and falling edge occur in the same UI (a valid TdiPW).
6. DQ minimum input pulse width defined at the VCENTDQ,midpoint.
7. DQS-to-DQ Rx mask offset is skew between DQS and DQ within a nibble (x4) or word (x8, x16 [for x16, the upper and lower bytes are treated as separate x8s]) at the SDRAM balls over process, voltage, and temperature.
8. DQ-to-DQ Rx mask offset is skew between DQs within a nibble (x4) or word (x8, x16) at the SDRAM balls for a given component over process, voltage, and temperature.
9. Input slew rate over VdiVW mask centered at VCENTDQ,midpoint. Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7V/ns of each other.
10. Input slew rate between VdiVW mask edge and VIHL(AC)min points.
11. Note 1 applies to the entire table.

The following figure shows the Rx mask relationship to the input timing specifications relative to system tDS and tDH. The classical definition for tDS/tDH required a DQ rising and falling edges to not violate tDS and tDH relative to the DQS strobe at any time; however, with the Rx mask tDS and tDH can shift relative to the DQS strobe provided the input pulse width specification is satisfied and the Rx mask is not violated.

Figure 200. Rx Mask Relative to ^{t}DS/^{t}DH



The following figure and table show an example of the worst case Rx mask required if the DQS and DQ pins do not have DRAM controller to DRAM write DQ training. The figure and table show that without DRAM write DQ training, the Rx mask would increase from 0.2UI to essentially 0.54UI. This would also be the minimum tDS and tDH required as well.

Figure 201. Rx Mask Without Write Training

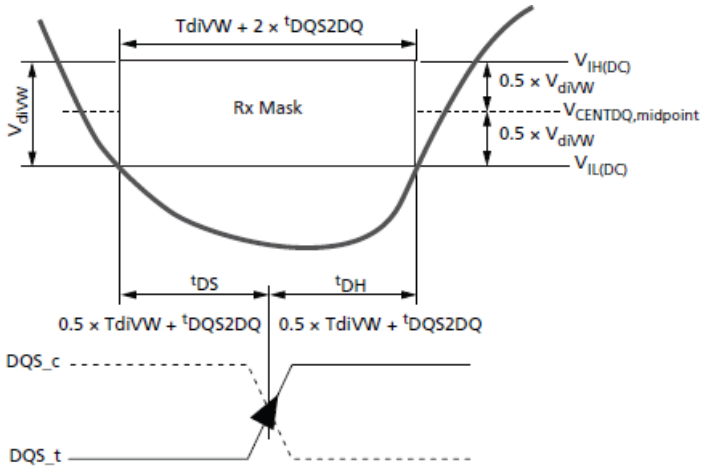


Table 82. Rx Mask and ^{t}DS/^{t}DH without Write Training

DDR4	VIHL(AC) (mV)	TdiPW (UI)	VdiVW (mV)	TdiVW (UI)	tDQS2DQ (UI)	tDQ2DQ (UI)	Rx Mask with Write Train (ps)	tDS + tDH (ps)
2666	150	0.58	120	0.22	±0.19	0.105	82.5	225
3200	140	0.58	110	0.23	±0.22	0.125	71.8	209

Notes: 1. VIHL(AC), VdiVW, and VILH(DC) referenced to VCENTDQ,midpoint.

Connectivity Test (CT) Mode Input Levels

Table 83. TEN Input Levels (CMOS)

Parameter	Symbol	Min	Max	Unit	Note
TEN AC Input High Voltage	VIH(AC)_TEN	0.8 * VDD	VDD	V	1
TEN DC Input High Voltage	VIH(DC)_TEN	0.7 * VDD	VDD	V	
TEN DC Input Low Voltage	VIL(DC)_TEN	VSS	0.3 * VDD	V	
TEN AC Input Low Voltage	VIL(AC)_TEN	VSS	0.2 * VDD	V	2
TEN falling time	tF_input_TEN	-	10	ns	
TEN rising time	tR_input_TEN	-	10	ns	

Note:

1. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
2. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

Figure 202. TEN Input Slew Rate Definition

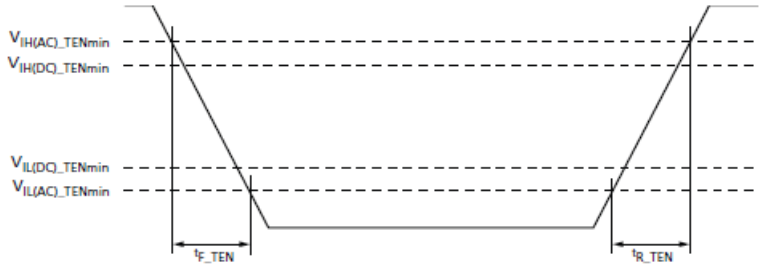


Table 84. CT Type-A Input Levels

Parameter	Symbol	Min	Max	Unit	Note
CTipA AC Input High Voltage	VIH(AC)_CTipA	VREF + 200	VDD *1	V	2,3
CTipA DC Input High Voltage	VIH(DC)_CTipA	VREF + 150	VDD	V	2,3
CTipA DC Input Low Voltage	VIL(DC)_CTipA	VSS	VREF - 150	V	2,3
CTipA AC Input Low Voltage	VIL(AC)_CTipA	VSS *1	VREF - 200	V	2,3
CTipA falling time	tF_CTipA	-	5	ns	2
CTipA rising time	tR_CTipA	-	5	ns	2

Note:

1. Refer to Overshoot and Undershoot Specifications.
2. CT Type-A inputs: CS_n, BG[1:0], BA[1:0], A[9:0], A10/AP, A11, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, A17, CKE, ACT_n, ODT, CLK_t, CLK_C, PAR.
3. VREFCA = 0.5 x VDD.

Figure 203. CT Type-A Input Slew Rate Definition

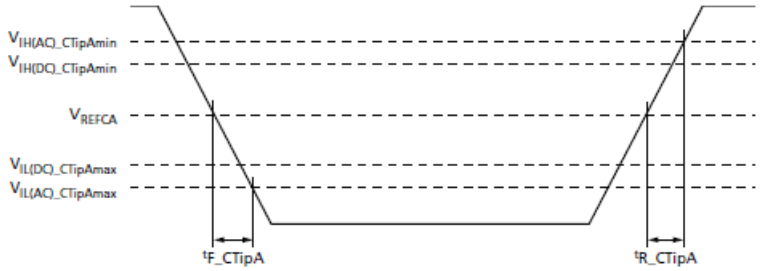


Table 85. CT Type-B Input Levels

Parameter	Symbol	Min	Max	Unit	Note
CTipB AC Input High Voltage	VIH(AC)_CTipB	VREF + 300	VDD *1	V	2,3
CTipB DC Input High Voltage	VIH(DC)_CTipB	VREF + 200	VDD	V	2,3
CTipB DC Input Low Voltage	VIL(DC)_CTipB	VSS	VREF - 200	V	2,3
CTipB AC Input Low Voltage	VIL(AC)_CTipB	VSS *1	VREF - 300	V	2,3
CTipB falling time	tF_ CTipB	-	5	ns	2
CTipB rising time	tR_ CTipB	-	5	ns	2

Note:

1. Refer to Overshoot and Undershoot Specifications.
2. CT Type-B inputs: DML_n/DBIL_n, DMU_n/DBIU_n and DM_n/DBI_n.
3. VREFDQ should be 0.5 x VDD.

Figure 204. CT Type-B Input Slew Rate Definition

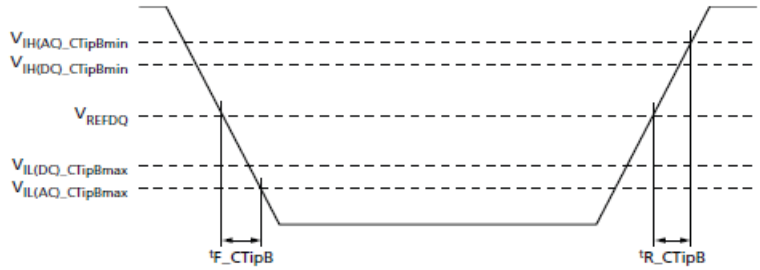


Table 86. CT Type-C Input Levels

Parameter	Symbol	Min	Max	Unit	Note
CTipC AC Input High Voltage	VIH(AC)_CTipC	0.8 * VDD	VDD *1	V	2
CTipC DC Input High Voltage	VIH(DC)_CTipC	0.7 * VDD	VDD	V	2
CTipC DC Input Low Voltage	VIL(DC)_CTipC	VSS	0.3 * VDD	V	2
CTipC AC Input Low Voltage	VIL(AC)_CTipC	VSS *1	0.2 * VDD	V	2
CTipC falling time	tF_ CTipC	-	10	ns	2
CTipC rising time	tR_ CTipC	-	10	ns	2

Note:

1. Refer to Overshoot and Undershoot Specifications.
2. CT Type-C inputs: Alert_n.

Figure 205. CT Type-C Input Slew Rate Definition

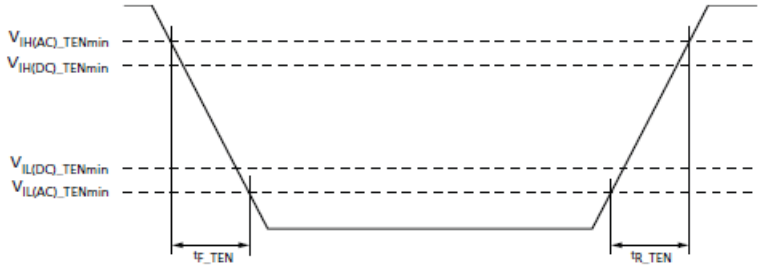


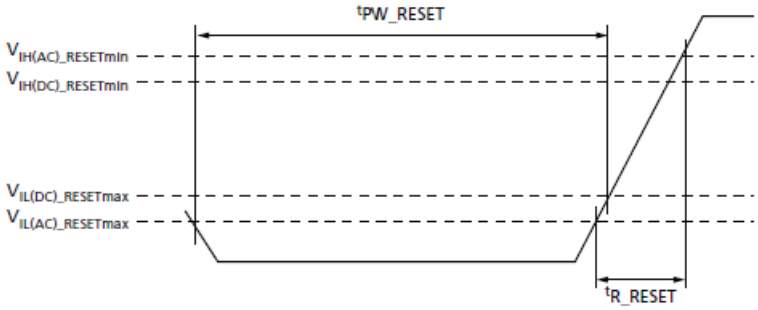
Table 87. CT Type-D Input Levels

Parameter	Symbol	Min	Max	Unit	Note
CTipC AC Input High Voltage	VIH(AC)_CTipC	0.8 * VDD	VDD	V	4
CTipC DC Input High Voltage	VIH(DC)_CTipC	0.7 * VDD	VDD	V	2
CTipC DC Input Low Voltage	VIL(DC)_CTipC	VSS	0.3 * VDD	V	1
CTipC AC Input Low Voltage	VIL(AC)_CTipC	VSS	0.2 * VDD	V	5
Rising time	tR_RESET	-	1	µs	3
RESET pulse width - after power-up	tPW_RESET_S	1	-	µs	
RESET pulse width - during power-up	tPW_RESET_L	200	-	ns	

Note:

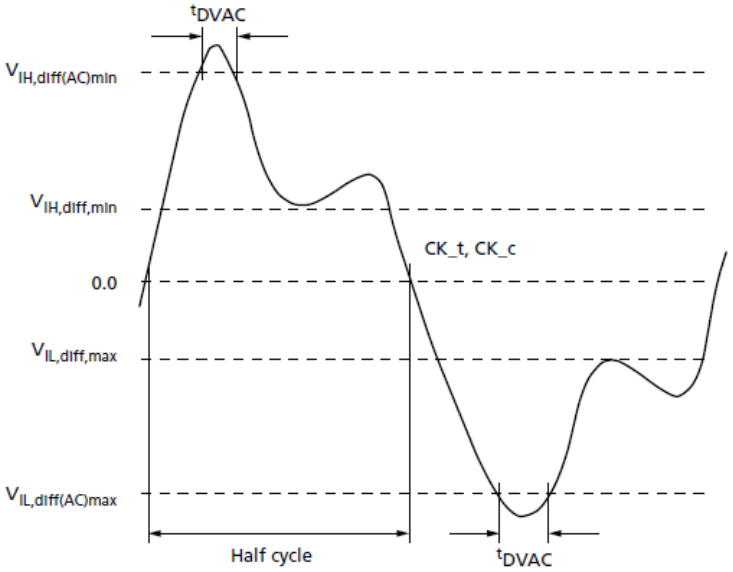
1. After RESET_n is registered LOW, the RESET_n level must be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, the DRAM may not be reset.
2. After RESET_n is registered HIGH, the RESET_n level must be maintained above VIH(DC)_RESET, otherwise, operation will be uncertain until it is reset by asserting RESET_n signal LOW.
3. Slope reversal (ring-back) during this level transition from LOW to HIGH should be mitigated as much as possible.
4. Overshoot should not exceed the VIN values in the Absolute Maximum Ratings table.
5. Undershoot should not exceed the VIN values in the Absolute Maximum Ratings table.
6. CT Type-D inputs: RESET_n; same requirements as in normal mode.

Figure 206. CT Type-D Input Slew Rate Definition



Differential Inputs

Figure 207. Differential AC Swing and "Time Exceeding AC-Level" ^{t}DVAC



Notes:
1. Differential signal rising edge from VIL,diff,max to VIH,diff(AC)min must be monotonic slope.
2. Differential signal falling edge from IH,diff,min to VIL,diff(AC)max must be monotonic slope.

Table 88. Differential Input Swing Requirements for CK_t, CK_c

Parameter	Symbol	DDR4-2666		DDR4-3200		Unit	Note
		Min	Max	Min	Max		
Differential input high	VIHdiff	135	Note 3	110	Note 3	mV	1
Differential input low	VILdiff	Note 3	-135	Note 3	-110	mV	1
Differential input high (AC)	VIHdiff(AC)	2 x (VIH(AC) - VREF)	Note 3	2 x (VIH(AC) - VREF)	Note 3	V	2
Differential input low (AC)	VILdiff(AC)	Note 3	2 x (VIL(AC) - VREF)	Note 3	2 x (VIL(AC) - VREF)	V	2

Notes:
1. Used to define a differential signal slew-rate.
2. For CK_t, CK_c use VIH(AC) and VIL(AC) of ADD/CMD and VREFCA.
3. These values are not defined; however, the differential signals (CK_t, CK_c) need to be within the respective limits, VIH(DC)max and VIL(DC)min for single-ended signals as well as the limitations for overshoot and undershoot.

Table 89. Minimum Time AC Time ^{t}DVAC for CK

Parameter	tDVAC (ps) at |VIH,diff(AC) to VIL,diff(AC)|
	200mV
>4.0	120
4.0	115
3.0	110
2.0	105
1.9	100
1.6	95
1.4	90
1.2	85
1.0	80
<1.0	80

Notes: 1. Below VIL(AC).

Single-Ended Requirements for CK Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has to comply with certain requirements for single-ended signals. CK_t and CK_c have to reach approximately VSEHmin/VSEL,max, which are approximately equal to the AC levels VIH(AC) and VIL(AC) for ADD/CMD signals in every half-cycle.

The applicable AC levels for ADD/CMD might differ per speed-bin, and so on. For example, if a value other than 100mV is used for ADD/CMD VIH(AC) and VIL(AC) signals, then these AC levels also apply for the single-ended signals CK_t and CK_c.

While ADD/CMD signal requirements are with respect to VREFCA, the single-ended components of differential signals have a requirement with respect to VDD/2; this is nominally the same. The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL,max/VSEH,min has no bearing ontiming, but adds a restriction on the common mode characteristics of these signals.

Figure 208. Single-Ended Requirements for CK

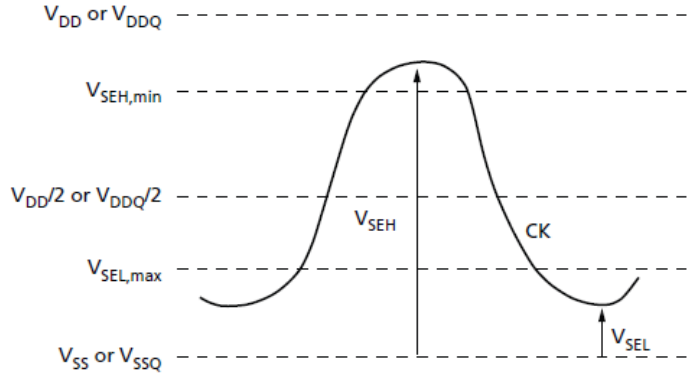


Table 90. Single-Ended Requirements for CK

Symbol	Parameter	DDR4-2666		DDR4-3200		Unit	Note
		Min.	Max.	Min.	Max.		
V_{SEH}	Single-ended high-level for CK_t , CK_c	(VDD/2) +0.095	Note3	(VDD/2) +0.085	Note3	V	1, 2
V_{SEL}	Single-ended low-level for CK_t , CK_c	Note3	(VDD/2) -0.095	Note3	(VDD/2) - 0.085	V	1, 2

Note:

1. For CK_t - CK_c use $V_{IH.CA}/V_{IL.CA}$(AC) of ADD/CMD;
2. V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA};
3. These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

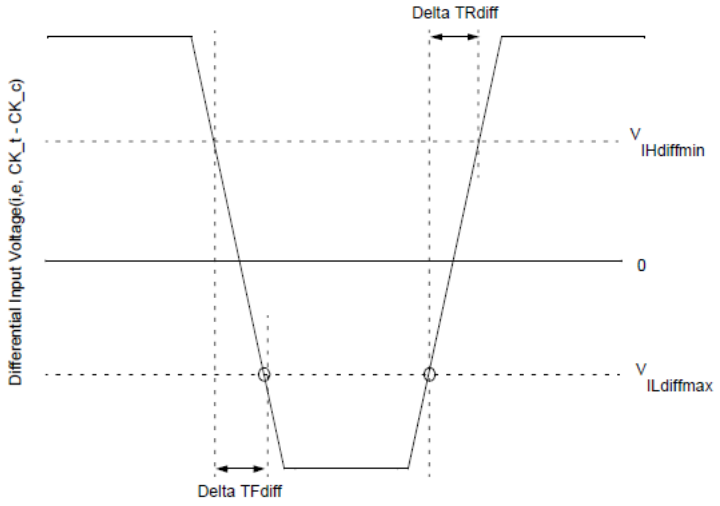
Slew Rate Definitions for CK Differential Input Signals

Table 91. CK Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge(CK_t - CK_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTRdiff
Differential input slew rate for falling edge(CK_t - CK_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTFdiff

Note: The differential signal (i,e.,CK_t - CK_c) must be linear between these thresholds.

Figure 209. Differential Input Slew Rate Definition for CK_t, CK_c



CK Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signal CK_t, CK_c must meet the requirements shown below. The differential input cross point voltage VIX(CK) is measured from the actual cross point of true and complement signals to the midlevel between VDD and VSS.

Figure 210. $V_{IX(CK)}$ Definition

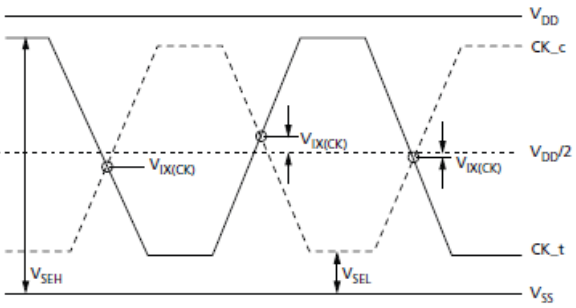


Table 92. Cross Point Voltage For CK Differential Input Signals at DDR4-2666 through DDR4-3200

Parameter	Symbol	Input Level	DDR4-2666/3200	
			Min.	Max.
Differential input cross point voltage relative to VDD/2 for CK_t, CK_c	$V_{IX(CK)}$	VSEH > VDD/2 + 145mV	N/A	110mV
		VDD/2 + 90mV≦VSEH ≦VDD/2 + 145mV	N/A	(VSEH - VDD/2) - 30mV
		VDD/2 - 145mV≦VSEL≦VDD/2 - 90mV	-(VDD/2 - VSEL) + 30mV	N/A
		VSEL < VDD/2 - 145mV	-110mV	N/A

DQS Differential Input Signal Definition and Swing Requirements

Figure 211. Differential Input Signal Definition for DQS_t, DQS_c

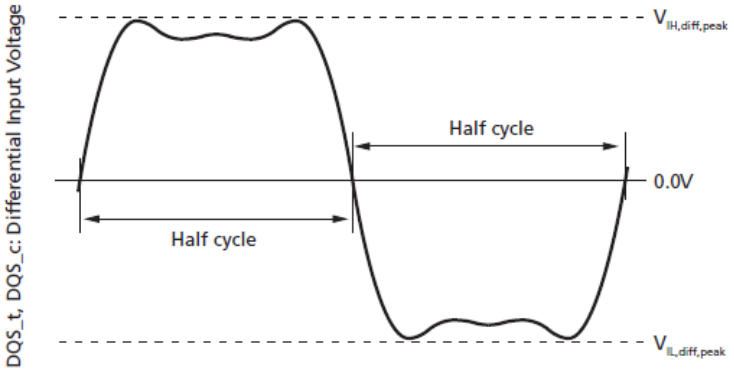


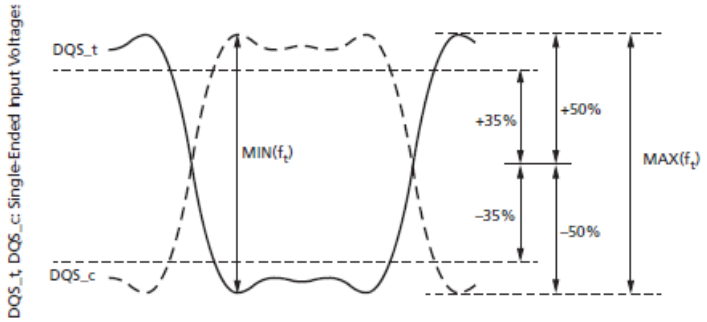
Table 93. Cross Point Voltage For CK Differential Input Signals at DDR4-2666 through DDR4-3200

Parameter	Symbol	DDR4-2666		DDR4-3200		Unit	Notes
		Min.	Max.	Min.	Max.		
Peak differential input high voltage	VIH,diff,peak	150	VDDQ	140	VDDQ	mV	1,2
Peak differential input low voltage	VIL,diff,peak	VSSQ	-150	VSSQ	-140	mV	1,2

Note:

1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
2. Minimum value point is used to determine differential signal slew-rate.

Figure 212. DQS_t, DQS_c Input Peak Voltage Calculation and Range of Exempt non-Monotonic Signaling



Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Cross point voltage for DQS differential input signals table. The differential input cross point voltage VIX_DQS (VIX_DQS_FR and VIX_DQS_RF) is measured from the actual cross point of DQS_t, DQS_c relative to the VDQSmid of the DQS_t and DQS_c signals.

VDQSmid is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.

A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within +/- 35% of the midpoint of either VIH.DIFF.Peak Voltage (DQS_t rising) or VIL.DIFF.Peak Voltage (DQS_c rising), refer to Definition of differential DQS Peak Voltage and rage of exempt non-monotonic signaling figure. A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Vix Definition (DQS) figure) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Vix Definition (DQS) figure) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Vix Definition (DQS) figure) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Vix Definition (DQS) figure) is not a valid horizontal tangent.

Figure 213. Vix Definition (DQS)

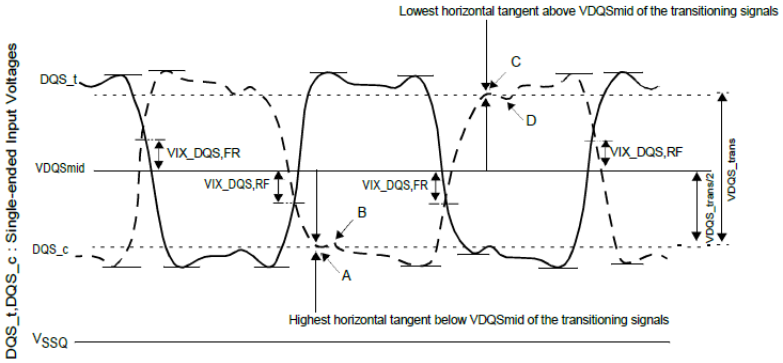


Table 94. Cross point voltage for DQS differential input signals

Symbol	Parameter	DDR4-2666/3200		Unit	Note
		Min	Max		
Vix_DQS_ratio	DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings	-	25	%	1, 2
VDQSmid_to_Vcent	VDQSmid offset relative to Vcent_DQ(midpoint)	-	Note 3	mV	2

Note:

1. VIX_DQS,ratio is DQS VIX crossing (VIX_DQS,FR or VIX_DQS,RF) divided by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQS,midd of the transitioning DQS signals and the highest horizontal tangent below VDQS,mid of the transitioning DQS signals.
2. VDQS,mid will be similar to the VREFDQ internal setting value (Vcent(midpoint) offset) obtained during VREF Training if the DQS and DQs drivers and paths are matched.
3. The maximum limit shall not exceed the smaller of VIH,diff,DQS minimum limit or 50mV.

Table 95. Slew Rate Definitions for DQS Differential

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (DQS_t - DQS_c)	VILDiff_DQS	VIHDiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTRdiff
Differential input slew rate for falling edge (DQS_t - DQS_c)	VIHDiff_DQS	VILDiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTFdiff

Table 96. Differential Input Level for DQS_t, DQS_c

Symbol	Parameter	DDR4-2666		DDR4-3200		Unit	Note
		Min.	Max.	Min.	Max.		
VIH,diff,peak	Peak differential input high voltage	150	VDDQ	140	VDDQ	mV	1
VIHDiff_DQS	Differential Input High	130	-	110	-	mV	2,3
2VILDiff_DQS	Differential Input Low	-	-130	-	-110	mV	2,3
VIL,diff,peak	Peak differential input low voltage	VSSQ	-150	VSSQ	-140	mV	1
SRIdiff	DQS differential input slew rate	2.5	18	2.5	18	V/ns	4,5

Note:

1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
2. Differential signal rising edge from VIL,diff,DQS to VIH,diff,DQS must be monotonic slope.
3. Differential signal falling edge from VIH,diff,DQS to VIL,diff,DQS must be monotonic slope.
4. Differential input slew rate for rising edge from VIL,diff,DQS to VIH,diff,DQS is defined by |VIL,diff,min -VIH,diff,max|/△TRdiff.
5. Differential input slew rate for falling edge from VIH,diff,DQS to VIL,diff,DQS is defined by |VIL,diff,min - VIH,diff,max|/△TFdiff.

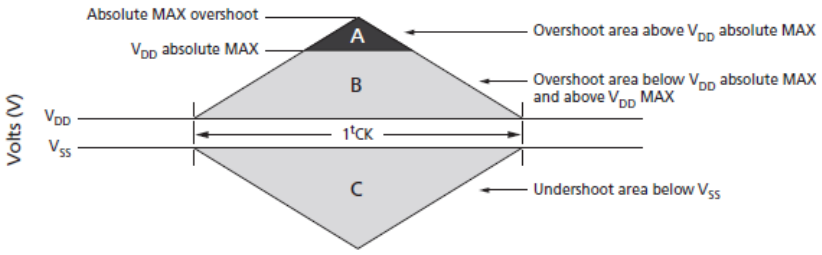
Address, Command and Control Overshoot and Undershoot specifications

Table 97. AC overshoot/undershoot specification for Address, Command and Control pins

Parameter	Symbol	DDR4- 2666/3200	Unit
Maximum peak amplitude above V_{AOS}	V_{AOSP}	0.06	V
Upper boundary of overshoot area A_{AOS1}	V_{AOS}	VDD + 0.24	V
Maximum peak amplitude allowed for undershoot	V_{AUS}	0.30	V
Maximum overshoot area per 1 tCK above V_{AOS}	A_{AOS2}	0.0055	V/ns
Maximum overshoot area per 1 tCK between VDD and V_{AOS}	A_{AOS1}	0.1699	V/ns
Maximum undershoot area per 1 tCK below VSS	A_{AUS}	0.1762	V/ns
(A0-A13,A17,BG0-BG1,BA0-BA1,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT,C2-C0)			

Note: The value of V_{AOS} matches VDD absolute max as defined in Absolute Maximum DC Ratings table if VDD equals VDD max as defined in Recommended DC Operating Conditions table. If VDD is above the recommended operating conditions, V_{AOS} remains at VDD absolute max as defined in Absolute Maximum DC Ratings table.

Figure 214. Address, Command and Control Overshoot and Undershoot Definition

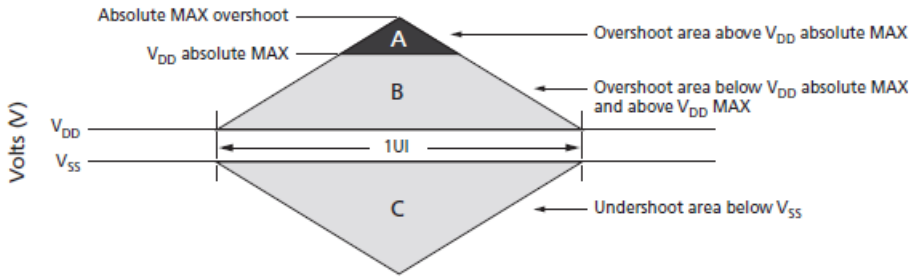


Clock Overshoot and Undershoot Specifications

Table 98. AC overshoot/undershoot specification for Clock

Parameter	Symbol	DDR4- 2666/3200	Unit
Maximum peak amplitude above V_{COS}	V_{COSP}	0.06	V
Upper boundary of overshoot area A_{DOS1}	V_{COS}	VDD + 0.24	V
Maximum peak amplitude allowed for undershoot	V_{CUS}	0.30	V
Maximum overshoot area per 1 UI above V_{COS}	A_{COS2}	0.0025	V/ns
Maximum overshoot area per 1 UI between VDD and V_{DOS}	A_{COS1}	0.0750	V/ns
Maximum undershoot area per 1 UI below VSS	A_{CUS}	0.0762	V/ns

Figure 215. Clock Overshoot and Undershoot Definition

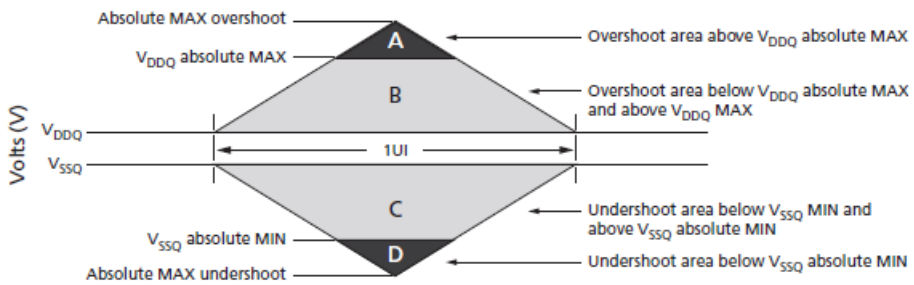


Data, trobe, and Mask Overshoot and Undershoot Specifications

Table 99. Data, Strobe, and Mask Overshoot and Undershoot/ Specifications

Parameter	DDR4- 2666/3200	Unit
Area A: Maximum peak amplitude above VDDQ absolute MAX	0.16	V
Area B: Amplitude allowed between VDDQ and VDDQ absolute MAX	0.24	V
Area C: Maximum peak amplitude allowed for undershoot below VSSQ	0.30	V
Area D: Maximum peak amplitude below VSSQ absolute MIN	0.10	V
Area A maximum overshoot area per 1UI	0.0100	V/ns
Area B maximum overshoot area per 1UI	0.0700	V/ns
Area C maximum undershoot area per 1UI	0.0700	V/ns
Area D maximum undershoot area per 1UI	0.0100	V/ns

Figure 216. Data, Strobe, and Mask Overshoot and Undershoot Definition



Single-ended AC & DC Output Levels

Table 100. Single-ended AC & DC output levels

Symbol	Parameter	DDR4-2666/3200	Unit
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V
$V_{OH(AC)}$	AC output high measurement level (for output SR)	(0.7 + 0.15) x V_{DDQ}	V
$V_{OL(AC)}$	AC output low measurement level (for output SR)	(0.7 - 0.15) x V_{DDQ}	V

Note:

1. The swing of ± 0.15 × V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ}.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals.

Table 101. Single-ended output slew rate definition

Description	Measured		Defined by
	from	to	
Single ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TRse
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TFse

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.

Figure 217. Single-ended Output Slew Rate Definition

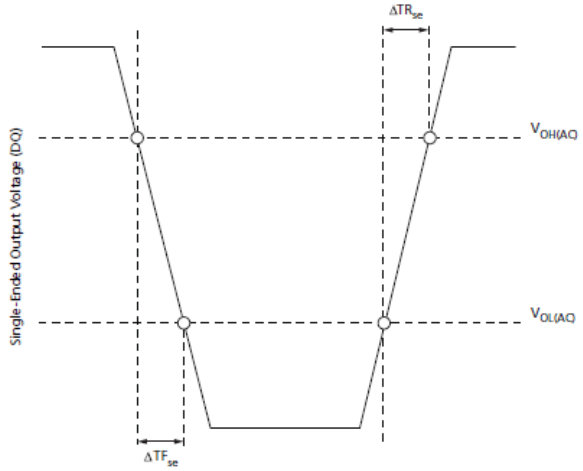


Table 102. Single-ended output slew rate

Parameter	Symbol	DDR4-2666/3200		Unit
		Min	Max	
Single ended output slew rate	SRQse	4	9	V/ns

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals
For Ron = RZQ/7 setting

Note: 1 In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e., they stay at either high or low).
-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e., from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

Differential Output Slew Rate

Table 103. Differential Output Levels

Symbol	Parameter	DDR4-2666/3200	Unit
$V_{OH,diff(AC)}$	AC differential output high measurement level (for output slew rate)	0.3 x V_{DDQ}	V
$V_{OL,diff(AC)}$	AC differential output low measurement level (for output slew rate)	-0.3 x V_{DDQ}	V

Notes: 1. The swing of ±0.3 x VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $R_{ZQ}/7$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$ at each differential output.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL,diff(AC)}$ and $V_{OH,diff(AC)}$ for differential signals.

Table 104. Differential output slew rate definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	V_{OLdiff}(AC)	V_{OHdiff}(AC)	[V_{OHdiff}(AC)-V_{OLdiff}(AC)] / Delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}(AC)	V_{OLdiff}(AC)	[V_{OHdiff}(AC)-V_{OLdiff}(AC)] / Delta TFdiff

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.

Figure 218. Differential Output Slew Rate Definition

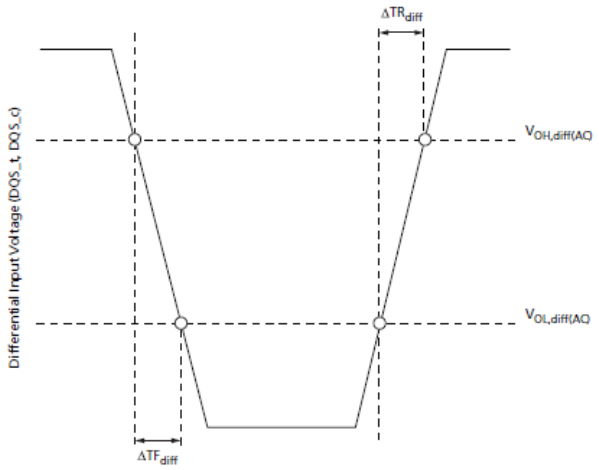


Table 105. Differential output slew rate

Parameter	Symbol	DDR4-2666/3200		Unit
		Min	Max	
Differential output slew rate	SRQdiff	8	18	V/ns

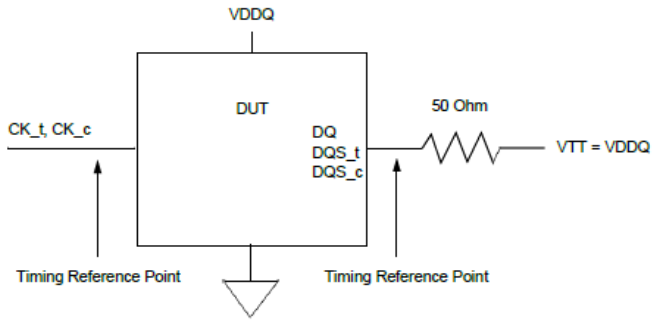
Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

Reference Load for AC Timing and Output Slew Rate

The effective reference load of 50 to VTT = VDDQ and driver impedance of RZQ/7 for each output was used in defining the relevant AC timing parameters of the device as well as output slew rate measurements. RON nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device. The maximum DC high level of output signal = 1.0 x VDDQ, the minimum DC low level of output signal = { 34 /(34 + 50) } x VDDQ = 0.4 x VDDQ.

The nominal reference level of an output signal can be approximated by the following: The center of maximum DC high and minimum DC low = { (1 + 0.4) / 2 } x VDDQ = 0.7 x VDDQ. The actual reference level of output signal might vary with driver RON and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye.

Figure 219. Reference Load for AC Timing and Output Slew Rate



Connectivity Test Mode Output Levels

Table 106. Connectivity Test Mode output levels

Symbol	Parameter	DDR4-2666/3200	Unit
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ	V
$V_{OH(AC)}$	AC output high measurement level (for output SR)	VTT + (0.1 x VDDQ)	V
$V_{OL(AC)}$	AC output below measurement level (for output SR)	VTT - (0.1 x VDDQ)	V

Note:

1. The effective test load is 50Ω terminated by VTT = 0.5 * VDDQ.

Figure 220. Connectivity Test Mode Timing Reference Load

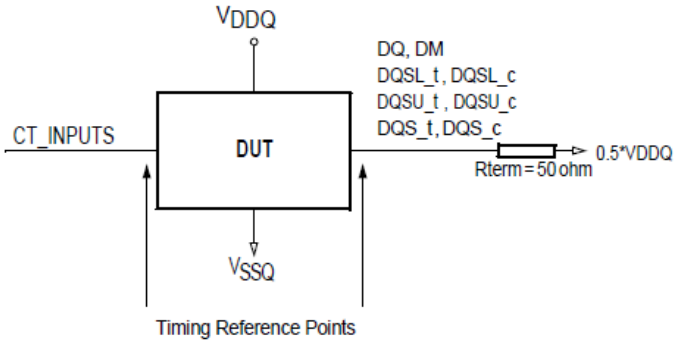


Figure 221. Output Slew Rate Definition of Connectivity Test Mode

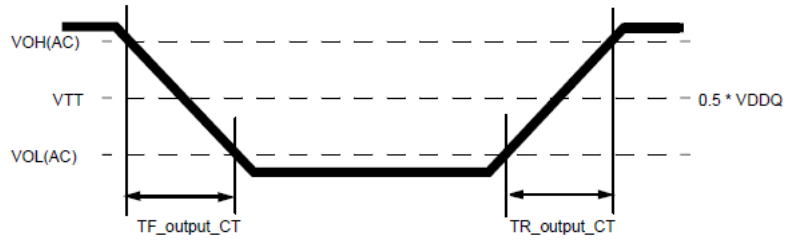


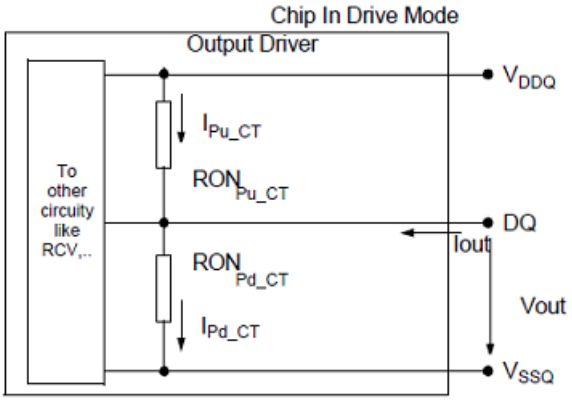
Table 107. Single-ended output slew rate of Connectivity Test Mode

Parameter	Symbol	DDR4-2666/3200		Unit
		Min	Max	
Output signal Falling time	TF_output_CT	-	10	ns/V
Output signal Rising time	TR_output_CT	-	10	ns/V

Connectivity Test Mode Output Driver Electrical Characteristic

The DDR4 driver supports special values during connectivity test mode. These RON values are referenced in this section. A functional representation of the output buffer is shown in the figure below.

Figure 222. Output Driver



The output driver impedance, *RON,* is determined by the value of the external reference resistor RZQ as follows: RON = RZQ/7. This targets 34Ω with nominal RZQ = 240Ω; however, connectivity test mode uses uncalibrated drivers and only a maximum target is defined. Mismatch between pull up and pull down is undefined.

The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ}-V_{OUT}}{|Iout|}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{|Iout|}$$

Table 108. RONPu_CT and RONPd_CT

RON_{NOM_CT}	Resistor	Vout	Max	Unit	Note
34Ω	RON_{Pd_CT}	VOB_{dc} = 0.2 x V_{DDQ}	1.9	34Ω	1
		VOL_{dc} = 0.5 x V_{DDQ}	2.0	34Ω	1
		VOM_{dc} = 0.8 x V_{DDQ}	2.2	34Ω	1
		VOH_{dc} = 1.1 x V_{DDQ}	2.5	34Ω	1
	RON_{Pu_CT}	VOB_{dc} = 0.2 x V_{DDQ}	2.5	34Ω	1
		VOL_{dc} = 0.5 x V_{DDQ}	2.2	34Ω	1
		VOM_{dc} = 0.8 x V_{DDQ}	2.0	34Ω	1
		VOH_{dc} = 1.1 x V_{DDQ}	1.9	34Ω	1

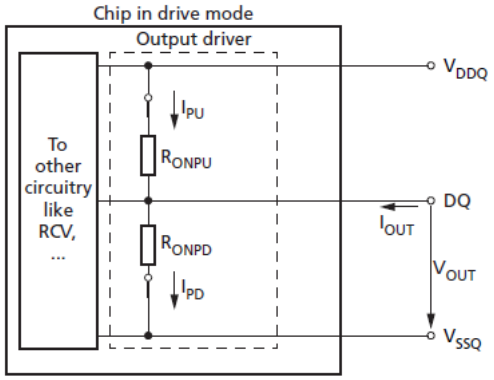
Note:

Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

Output Driver Electrical Characteristics

The DDR4 driver supports two RON values. These RON values are referred to as strong mode (low RON: 34Ω) and weak mode (high RON: 48Ω). A functional representation of the output buffer is shown in the figure below.

Figure 223. Output Driver: Definition of Voltages and Currents



The output driver impedance, *RON,* is determined by the value of the external reference resistor RZQ as follows: RON(34) = RZQ/7, or RON(48) = RZQ/5. This provides either a nominal 34.3Ω ±10% or 48Ω±10% with nominal RZQ = 240Ω.
The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:
RONPu when RONPd is off:

$$RON_{Pu} = \frac{V_{DDQ}-V_{OUT}}{|Iout|}$$

$$RON_{Pd} = \frac{V_{OUT}}{|Iout|}$$

Table 109. Output Driver Electrical Characteristics

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Note
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/7	1,2,3
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/7	1,2,3
		VOHdc= 1.1* VDDQ	0.83	1	1.25	RZQ/7	1,2,3
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2,3
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2,3
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2,3
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/5	1,2,3
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/5	1,2,3
		VOHdc= 1.1* VDDQ	0.83	1	1.25	RZQ/5	1,2,3
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2,3
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2,3
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2,3
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	10	-	23	%	1,2,3,4, 6,7
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,3,4, 5
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,3,4, 6,7

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
3. Recommends calibrating pull-down and pull-up output driver impedances at 0.8 VDDQ. Other calibration schemes may be used to achieve the linearity specification shown above; for example, calibration at 0.5 x VDDQ and 1.1 VDDQ.
4. DQ-to-DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized).
5. Measurement definition for mismatch between pull-up and pull-down, MMPUPD:
   Measure both RONPU and RONPD at 0.8 VDDQ separately; RON,nom is the nominal RON value:

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

6. RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

7. The lower and upper bytes of a x16 are each treated on a per byte basis.
8. Assumes RZQ = 240Ω; entire operating temperature range after proper ZQ calibration.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the equations and tables below. △T = T - T(@calibration); △V = VDDQ - VDDQ(@ calibration); VDD = VDDQ

Table 110. Output Driver Sensitivity Definitions

Symbol	Min	Max	Unit
R_{ONPU}@ $V_{OH(DC)}$	0.6 - $dR_{ON}dTH$ x |△T| - $dR_{ON}dVH$ x |△V|	1.1 - $dR_{ON}dTH$ x |△T| + $dR_{ON}dVH$ x |△V|	$R_{ZQ}/6$
R_{ON}@ $V_{OM(DC)}$	0.9 - $dR_{ON}dTM$ x |△T| - $dR_{ON}dVM$ x |△V|	1.1 + $dR_{ON}dTM$ x |△T| + $dR_{ON}dVM$ x |△V|	$R_{ZQ}/6$
R_{ONPD}@ $V_{OL(DC)}$	0.6 - $dR_{ON}dTL$ x |△T| - $dR_{ON}dVL$ x |△V|	1.1 + $dR_{ON}dTL$ x |△T| + $dR_{ON}dVL$ x |△V|	$R_{ZQ}/6$

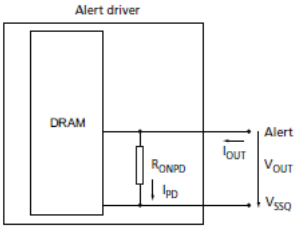
Table 111. Output Driver Voltage and Temperature Sensitivity

Parameter	Voltage and Temperature Range		Unit
	Min	Max	
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	0.15	%/mV
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV

Alert Driver

A functional representation of the alert output buffer is shown in the figure below. Output driver impedance, RON, is defined as follows.

Figure 224. Alert Driver



R_{ONPD} when R_{ONPU} is off:

$$R_{ONPD} = \frac{V_{OUT}}{|I_{OUT}|}$$

Table 112. Alert Driver Voltage

$R_{ON,NOM}$	Resistor	Vout	Min	Nom	Max	Unit
N/A	R_{ONPD}	$V_{OL(DC)}$ = 0.1 x V_{DDQ}	0.3	N/A	1.2	$R_{ZQ}/7$
		$V_{OM(DC)}$ = 0.8 x V_{DDQ}	0.4	N/A	1.2	$R_{ZQ}/7$
		$V_{OH(DC)}$ = 1.1 x V_{DDQ}	0.4	N/A	1.4	$R_{ZQ}/7$

Notes: 1. V_{DDQ} voltage is at $V_{DDQ(DC)}$.

On Die Termination Characteristics

ODT Levels and I-V Characteristics

On-die termination (ODT) effective resistance settings are defined and can be selected by any or all of the following options:

- MR1[10:8] (RTT(NOM)): Disable, 240 ohms, 120 ohms, 80 ohms, 60 ohms, 48 ohms, 40 ohms, and 34 ohms.
- MR2[11:9] (RTT(WR)): Disable, 240 ohms,120 ohms, and 80 ohms.
- MR5[8:6] (RTT(Park)): Disable, 240 ohms, 120 ohms, 80 ohms, 60 ohms, 48 ohms, 40 ohms, and 34 ohms.

ODT is applied to the following inputs:

- x16: DQ, DML_n, DMU_n, DQSL_t, DQSL_c, DQUS_t, and DQSU_c inputs.

A functional representation of ODT is shown in the figure below.

Figure 225. ODT Definition of Voltages and Currents

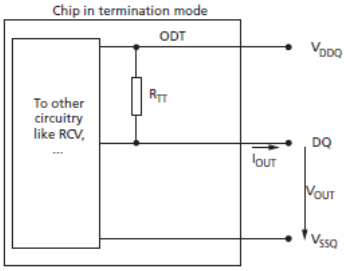


Table 113. ODT DC Characteristics

RTT	Vout	Min	Nom	Max	Unit	Note
240Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ	1,2,3
120Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/2	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/2	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/2	1,2,3
80Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/3	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/3	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/3	1,2,3
60Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/4	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/4	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/4	1,2,3
48Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2,3
40Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/6	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/6	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/6	1,2,3
34Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2,3
DQ-DQ Mismatch Within byte	VOMdc = 0.8* VDDQ	0	-	10	%	1,2,4,5,6

Note:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve

the linearity spec shown above, e.g., calibration at 0.5*VDDQ and 1.1*VDDQ.

3. The tolerance limits are specified under the condition that VDDQ=VDD and VSSQ=VSS
4. DQ to DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized)
5. RTT variance range ratio to RTT Nominal value in a given component, including DQS_t and DQS_c.

$$\text{DQ-DQ Mismatch in a Device} = \frac{\text{RTTMax -RTTMin}}{\text{RTTNOM}} *100$$

6. This parameter of x16 device is specified for Upper byte and Lower byte.

ODT Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the following equations and tables.
△T = T - T(@ calibration); △V = VDDQ - VDDQ(@ calibration); VDD = VDDQ

Table 114. ODT Sensitivity Definitions

Symbol	Min	Max	Unit
R_{TT}@	0.9 - $dR_{TT}dT$ x |△T| - $dR_{TT}dV$ x |△V|	1.6 + $dR_{TT}dTH$ x |△T| + $dR_{TT}dVH$ x |△V|	R_{ZQ}/n

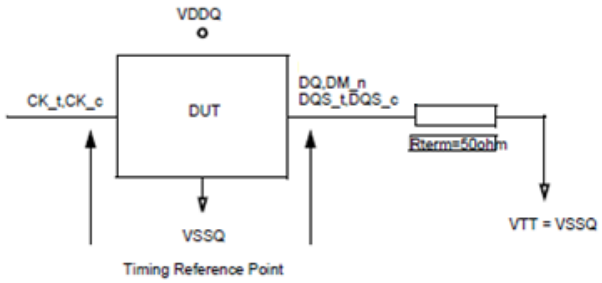
Table 115. Output Driver Voltage and Temperature Sensitivity

Parameter	Voltage and Temperature Range		Unit
	Min	Max	
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

ODT Timing Definitions

The reference load for ODT timings is different than the reference load used for timing measurements.

Figure 226. ODT Timing Reference Load



ODT Timing Definitions and Waveforms

Definitions for tADC, tAONAS, and tAOFAS are provided in the 4 and shown in 3 and 5. Measurement reference settings are provided in the subsequent 5.

The tADC for the dynamic ODT case and read disable ODT cases are represented by tADC of Direct ODT Control case.

Table 116. ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
tADC	Rising edge of CK_t,CK_c defined by the end point of DODTLoff	Extrapolated point at VRTT_NOM	Definition of tADC at Direct ODT Control
	Rising edge of CK_t,CK_c defined by the end point of DODTLon	Extrapolated point at VSSQ	
	Rising edge of CK_t - CK_c defined by the end point of ODTLcnw	Extrapolated point at VRTT_NOM	Definition of tADC at Dynamic ODT Control
	Rising edge of CK_t - CK_c defined by the end point of ODTLcwn4 or ODTLcwn8	Extrapolated point at VSSQ	
tAONAS	Rising edge of CK_t,CK_c with ODT being first registered high	Extrapolated point at VSSQ	Definition of tAOFAS and tAONAS
tAOFAS	Rising edge of CK_t,CK_c with ODT being first registered low	Extrapolated point at VRTT_NOM	

Table 117. Reference Settings for ODT Timing Measurements

Symbol	RTT(Park)	RTT(NOM)	RTT(WR)	VSW1	VSW2	Note
tADC	Disable	RZQ/7 (34Ω)	-	0.20V	0.40V	1, 2
	-	RZQ/7 (34Ω)	High-Z	0.20V	0.40V	1, 3
tAONAS	Disable	RZQ/7 (34Ω)	-	0.20V	0.40V	1, 2,
tAOFAS	Disable	RZQ/7 (34Ω)	-	0.20V	0.40V	1, 2

Note:

1. MR settings are as follows: MR1 has A10 = 1, A9 = 1, A8 = 1 for RTT(NOM) setting; MR5 has A8 = 0, A7 = 0, A6 = 0 for RTT(Park) setting; and MR2 has A11 = 0, A10 = 1, A9 = 1 for RTT(WR) setting.
2. ODT state change is controlled by ODT pin.
3. ODT state change is controlled by a WRITE command.

Figure 227. tADC at Direct ODT Control

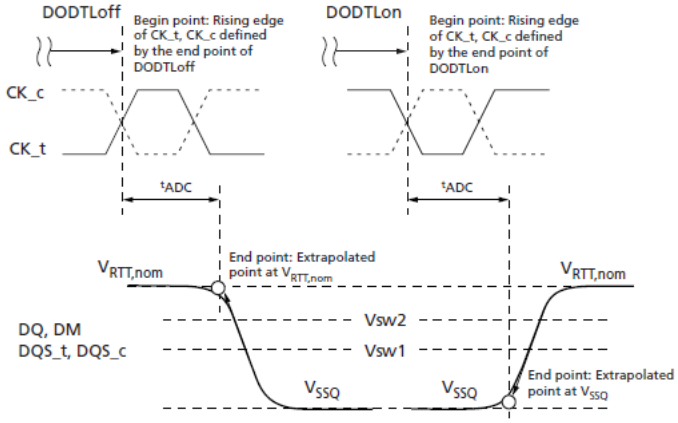


Figure 228. tADC Definition with Dynamic ODT Control

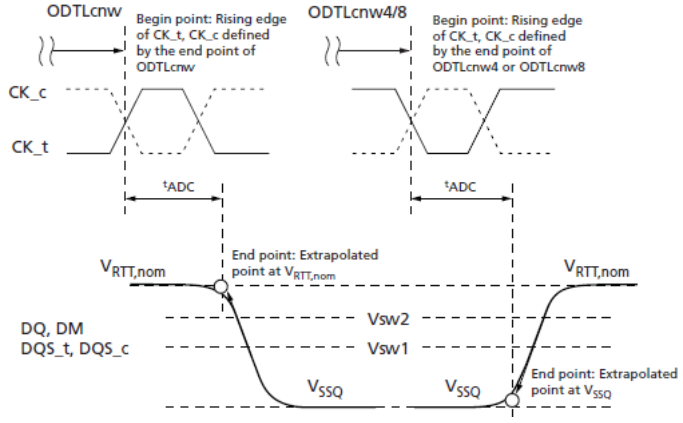
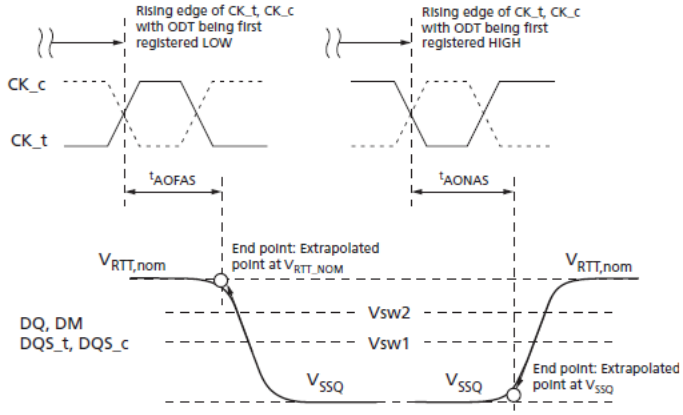


Figure 229. tAOFAS and tAONAS Definitions



DRAM Package Electrical Specifications

Table 118. DRAM package electrical specifications

Symbol	Parameter	DDR4-2666/3200		Unit	Note
		Min.	Max.		
Z_{IO}	Input/output Zpkg	45	85	Ω	1
T_{dIO}	Input/output Pkg Delay	14	45	ps	1
L_{io}	Input/Output Lpkg	-	3.4	nH	1, 2
C_{io}	Input/Output Cpkg	-	0.82	pF	1, 3
$Z_{IO\ DQS}$	DQS_t, DQS_c Zpkg	45	85	Ω	1
$Td_{IO\ DQS}$	DQS_t, DQS_c Pkg Delay	14	45	ps	1
$L_{io\ DQS}$	DQS Lpkg	-	3.4	nH	1, 2
$C_{io\ DQS}$	DQS Cpkg	-	0.82	pF	1, 3
$DZ_{DIO\ DQS}$	Delta Zpkg DQSU_t, DQSU_c	-	10.5	Ω	-
	Delta Zpkg DQSL_t, DQSL_c	-	10.5	Ω	-
$D_{TdDIO\ DQS}$	Delta Delay DQSU_t, DQSU_c	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	ps	-
$Z_{I\ CTRL}$	Input CTRL pins Zpkg	50	90	Ω	1
$T_{dI\_\ CTRL}$	Input CTRL pins Pkg Delay	14	42	ps	1
$L_{i\ CTRL}$	Input CTRL Lpkg	-	3.4	nH	1, 2
$C_{i\ CTRL}$	Input CTRL Cpkg	-	0.7	pF	1, 3
$Z_{IADD\ CMD}$	Input- CMD ADD pins Zpkg	50	90	Ω	1
$Td_{IADD\_\ CMD}$	Input- CMD ADD pins Pkg Delay	14	52	ps	1
$L_{i\ ADD\ CMD}$	Input CMD ADD Lpkg	-	3.9	nH	1, 2
$C_{i\ ADD\ CMD}$	Input CMD ADD Cpkg	-	0.86	pF	1, 3
Z_{CK}	CK_c Zpkg	50	90	Ω	1
Td_{CK}	CK_c Pkg Delay	14	42	ps	1
DZ_{DCK}	Delta Zpkg CK_c	-	10.5	Ω	-
D_{TdCK}	Delta Delay CK_c	-	5	ps	-
$L_{i\ CLK}$	Input CK Lpkg	-	3.4	nH	1, 2
$C_{i\ CLK}$	Input CK Cpkg	-	0.7	pF	1, 3
Z_{OZQ}	ZQ Zpkg	-	100	Ω	-
$Td_{O\ ZQ}$	ZQ Delay	20	90	ps	-
$Z_{O\ ALERT}$	ALERT Zpkg	40	100	Ω	-
$Td_{O\ ALERT}$	ALERT Delay	20	55	ps	-

Note:

1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown
2. It is assumed that Lpkg can be approximated as Lpkg = Zo*Td
3. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo

Input/Output Capacitance

Table 119. Silicon pad I/O Capacitance

Symbol	Parameter	DDR4-2666		DDR4-3200		Unit	Note
		Min.	Max.	Min.	Max.		
C_{IO}	Input/output capacitance	0.55	1.15	0.55	1.00	pF	1,2,3
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.7	0.15	0.7	pF	2,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	pF	2,3,6
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	pF	2,3,5
C_{I}	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.7	0.15	0.55	pF	2,3,4
C_{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	pF	2,3,8,9
$C_{DI\_ADD\_CMD}$	Input capacitance delta(All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,10,11
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	pF	1,2,3,4
C_{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	pF	2,3
C_{ZQ}	Input/output capacitance of ZQ	-	2.3	-	2.3	pF	2,3,12
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.15	2.3	pF	2,3,13

Note:

1. Although the DM pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to a production test; it is verified by design and characterization and are provided for reference; system signal simulations should not use these values but use the package model. The capacitance is measured with VDD, VDDQ, VSS, and VSSQ applied and all other pins floating (except the pin under test, CKE, RESET_n and ODT, as necessary). VDD = VDDQ = 1.2V, VBIAS = VDD/2 and on-die termination off. Measured data is rounded using industry standard half-rounded up methodology to the nearest hundredth of the MSB.
3. This parameter applies to monolithic die, obtained by de-embedding the package L and C parasitics.
4. CDIO = CIO(DQ, DM) - 0.5 (CIO(DQS_t) + CIO(DQS_c)).
5. Absolute value of CIO (DQS_t), CIO (DQS_c)
6. Absolute value of CCK_t, CCK_c
7. CI applies to ODT, CS_n, CKE, A[17:0], BA[1:0], BG[1:0], RAS_n, CAS_n, ACT_n, PAR and WE_n.
8. CDI_CTRL applies to ODT, CS_n, and CKE.
9. CDI_CTRL = CI(CTRL) - 0.5 x (CI(CLK_t) + CI(CLK_c)).
10. CDI_ADD_CMD applies to A[17:0], BA1:0], BG[1:0], RAS_n, CAS_n, ACT_n, PAR and WE_n.
11. CDI_ADD_CMD = CI(ADD_CMD) - 0.5 x (CI(CLK_t) + CI(CLK_c)).
12. Maximum external load capacitance on ZQ pin: 5pF.
13. Only applicable if TEN pin does not have an internal pull-up.

IDD and IDDQ Specification Parameters and Test conditions

IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements figure shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement figure. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

- For IDD, IPP and IDDQ measurements, the following definitions apply:
- "0" and "LOW" is defined as VIN <= VILAC(max).
- "1" and "HIGH" is defined as VIN >= VIHAC(min).
- "MID-LEVEL" is defined as inputs are VREF = VDD / 2.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table .
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1] table through IDD7 Measurement-Loop Pattern[1] table.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  RTT_NOM = RZQ/6 (40 Ohm in MR1);
  RTT_WR = RZQ/2 (120 Ohm in MR2);
  RTT_PARK = Disable;
  Qoff = 0B (Output Buffer enabled) in MR1;
  TDQS_t disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear down mode disabled in MR3
  Read/Write DBI disabled in MR5;
  DM disabled in MR5

- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} := {HIGH, LOW, LOW, LOW, LOW} ; apply BG/BA changes when directed.
- Define D_n = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} := {HIGH, HIGH, HIGH, HIGH, HIGH} ; apply invert of BG/BA changes when directed above.

NOTE: The measurement-loop patterns must be executed at least once before actual current measurements can be taken, with the exception of IDD9 which may be measured any time after MBIST-PPR entry.

Figure 230. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

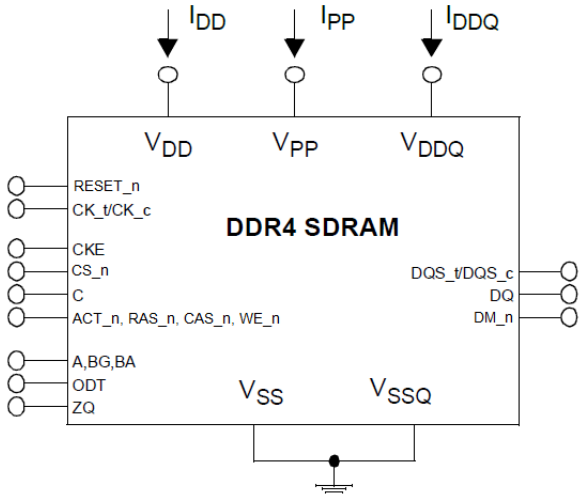
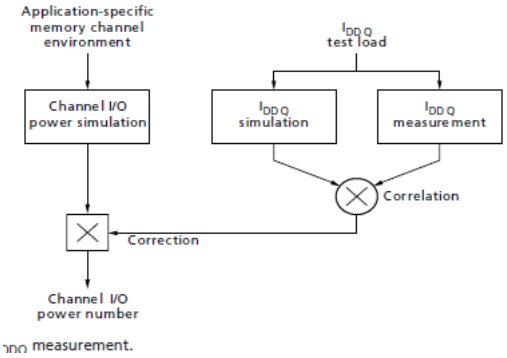


Figure 231. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement



Note: 1. Supported by IDDQ measurement.

Table 120. Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns (cont'd) table; **BL:** 8[1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to **IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1] t**able; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1] table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1] **t**able.
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0**
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns (cont'd) table; **BL:** 8[1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling according to IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1] table; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1] table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1] table
IDD2N	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns (cont'd) table; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P table; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P table
IDD2NT	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns (cont'd) table; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD2NT and IDDQ2NT Measurement-Loop Pattern[1] table; **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according to IDD2NT and IDDQ2NT Measurement-Loop Pattern[1] table; **Pattern Details:** see IDD2NT and IDDQ2NT Measurement-Loop Pattern[1] table
IDD2P	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: see **Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns (cont'd) t**able; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see **Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns (cont'd) t**able; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0

Symbol	Description
IDD3N	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P table; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P table
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N**
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[2]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1] table; **Data IO:** seamless read data burst with different data between one burst and the next one according to IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1] table; **DM_n**: stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1] table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1] table
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1] table; **Data IO:** seamless write data burst with different data between one burst and the next one according to IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1] table; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1] table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** see IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1] table
IDD5R	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD5B Measurement-Loop Pattern[1] table; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC (see IDD5B Measurement-Loop Pattern[1] table); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD5B Measurement-Loop Pattern[1] table
IPP5R	**Burst Refresh Write IPP Current (1X REF) Same condition with IDD5B**

Symbol	Description
IDD6N	**Self Refresh Current: Normal Temperature Range** ***T*CASE for devices:** 0 to 85°C; **Low Power Auto Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IDD6E	**Self-Refresh Current: Extended Temperature Range**) ***T*CASE for devices:** 0 to 95°C; **Low Power Auto Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6X	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E**
IDD6R	**Self-Refresh Current: Reduced Temperature Range** ***T*CASE for CT devices:** 0 to 45°C; **Low Power Auto Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: see Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table; **BL:** 8[1]; **AL:** CL-1; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to IDD7 Measurement-Loop Pattern1 table; **Data IO:** read data bursts with different data between one burst and the next one according to IDD7 Measurement-Loop Pattern1 table; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see IDD7 Measurement-Loop Pattern1 table; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see DD7 Measurement-Loop Pattern1 table
IPP7	**Operating Bank Interleave Read IPP** **Current Same condition with IDD7**
IDD8	**Maximum Power Down Current** **DRAM in MPSM, CKE:** HIGH; **External clock:** on; **tCK, CL:** see Recommended DC Operating Conditions table, **BL:** 8[1]; **AL:** 0; **CS_n:** stable at 1; **Command, address, bank group address, bank address inputs:** stable at 0; **Data I/O:** VDDQ; **DM_n:** stable at 1; **Bank activity:** all banks closed; **Output buffer and RTT:** Enabled in mode registers[2]; **ODT signal:** stable at 0.
IDD9 (Optional)	**MBIST-PPR Current[6]** **Device in MBIST-PPR mode, External clock:** On; **CS_n:** stable at 1 after MBIST-PPR entry; **CA Inputs:** stable at 1; **Data IO:** Don't care; B**ank activity:** MBIST-PPR operation; **Output buffer and RTT:** Enabled in mode registers[2]; **ODT signal:** stable at LOW
IPP9 (Optional)	**MBIST-PPR IPP Current[6]** **Same condition with IDD9,** however measuring IPP current instead of IDD current

Note:

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable
   - set MR1 [A12 = 0] : Qoff = Output buffer enabled
   - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7

   RTT_Nom enable
   - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6

   RTT_WR enable
   - set MR2 [A11:9 = 001] : RTT_WR = RZQ/2

   RTT_PARK disable
   - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s
   010] : 1866MT/s, 2133MT/s
   011] : 2400MT/s

   Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate
   DLL disabled : set MR1 [A0 = 0]
   CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s
   010] : 2400MT/s
   Read DBI enabled : set MR5 [A12 = 1]
   Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Auto Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
   01] : Reduced Temperature range
   10] : Extended Temperature range
   11] : Auto Self Refresh
5. IDD2NG should be measured after sync pulse (NOP) input.
6. When measuring IDD9/IPP9 after entering MBIST-PPR mode and ALERT_N driving LOW, there is a chance that DRAM may perform an hPPR if fails are found after internal self-test is completed and before ALERT_N fires HIGH.

Table 121. I_{DD0} and I_{PP0} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n / A16	CAS_n / A15	WE_n / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3, 4	D_n, D_n	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			…	repeat nRC 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 1** instead																
		2	2*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead																
		3	3*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 3** instead																
		4	4*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 1** instead																
		5	5*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 2** instead																
		6	6*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 3** instead																
		7	7*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

Table 122. I_{DD1} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n / A16	CAS_n / A15	WE_n / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3, 4	D_n, D_n	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
			…	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
			nRCD -AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	**PRE**	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	
			…	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1*nRC + 3, 4	D_n, D_n	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
			…	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																
			1*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			…	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			1*nRC + nRAS	**PRE**	0	1	0	1	0	0	0	1	1	0	0	0	0	0	0	
			…	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																
		2	2*nRC	repeat Sub-Loop 0, use **$BG[1:0]^2$ = 0, BA[1:0] = 2** instead																
		3	3*nRC	repeat Sub-Loop 1, use **$BG[1:0]^2$ = 1, BA[1:0] = 3** instead																
		4	4*nRC	repeat Sub-Loop 0, use **$BG[1:0]^2$ = 0, BA[1:0] = 1** instead																
		5	5*nRC	repeat Sub-Loop 1, use **$BG[1:0]^2$ = 1, BA[1:0] = 2** instead																
		6	6*nRC	repeat Sub-Loop 0, use **$BG[1:0]^2$ = 0, BA[1:0] = 3** instead																
		7	7*nRC	repeat Sub-Loop 1, use **$BG[1:0]^2$ = 1, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

Table 123. I_{DD2N}, I_{DD3N} and I_{PP3P} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n / A16	CAS_n / A15	WE_n / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	0
			1	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	0
			2	D_n, D_n	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	0
			3	D_n, D_n	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	0
		1	4-7	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

Table 124. I_{DD2NT} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n / A16	CAS_n / A15	WE_n / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	0
			1	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	0
			2	D_n, D_n	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	0
			3	D_n, D_n	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	0
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ.

Table 125. I_{DD4R} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n / A16	CAS_n / A15	WE_n / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2,3	D_n, D_n	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
		1	4	RD	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6,7	D_n, D_n	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use **BG[1:0]^2 = 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 1, use **BG[1:0]^2 = 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0]^2 = 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 1, use **BG[1:0]^2 = 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0]^2 = 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 1, use **BG[1:0]^2 = 1, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command.

Table 126. I_{DD4W} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n / A16	CAS_n / A15	WE_n / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			2,3	D_n, D_n	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			6,7	D_n, D_n	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead															
		3	12-15	repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 3** instead															
		4	16-19	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 1** instead															
		5	20-23	repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 2** instead															
		6	24-27	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 3** instead															
		7	28-31	repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 0** instead															

Note:

1. DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command.

Table 127. I_{DD4WC} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n / A16	CAS_n / A15	WE_n / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC
			1,2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			3,4	D_n, D_n	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		1	5	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC
			6,7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			8,9	D_n, D_n	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		2	10-14	repeat Sub-Loop 0, use **BG[1:0]**2 **= 0, BA[1:0] = 2** instead																
		3	15-19	repeat Sub-Loop 1, use **BG[1:0]**2 **= 1, BA[1:0] = 3** instead																
		4	20-24	repeat Sub-Loop 0, use **BG[1:0]**2 **= 0, BA[1:0] = 1** instead																
		5	25-29	repeat Sub-Loop 1, use **BG[1:0]**2 **= 1, BA[1:0] = 2** instead																
		6	30-34	repeat Sub-Loop 0, use **BG[1:0]**2 **= 0, BA[1:0] = 3** instead																
		7	35-39	repeat Sub-Loop 1, use **BG[1:0]**2 **= 1, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Write Command.

Table 128. I_{DD5R} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n / A16	CAS_n / A15	WE_n / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D_n, D_n	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
			4	D_n, D_n	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
			5-8	repeat pattern 1...4, use **BG[1:0]**$_2$ **= 1, BA[1:0] = 1** instead																
			9–12	repeat pattern 1...4, use **BG[1:0]**$_2$ **= 0, BA[1:0] = 2** instead																
			13–16	repeat pattern 1...4, use **BG[1:0]**$_2$ **= 1, BA[1:0] = 3** instead																
			17–20	repeat pattern 1...4, use **BG[1:0]**$_2$ **= 0, BA[1:0] = 1** instead																
			21–24	repeat pattern 1...4, use **BG[1:0]**$_2$ **= 1, BA[1:0] = 2** instead																
			25–28	repeat pattern 1...4, use **BG[1:0]**$_2$ **= 0, BA[1:0] = 3** instead																
			29–32	repeat pattern 1...4, use **BG[1:0]**$_2$ **= 1, BA[1:0] = 0** instead																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are VDDQ.

Table 129. I_{DD7} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n / A16	CAS_n / A15	WE_n / A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/ BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	RDA	0	1	1	0	1	0		0	0	0	0	1	0	0	0	-
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D_n	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			...	repeat pattern 2...3 until nRRD - 1, if nRRD > 4. Truncate if necessary																
		1	nRRD	ACT	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	-
			nRRD + 1	RDA	0	1	1	0	1	0		1	1	0	0	1	0	0	0	-
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRRD > 4. Truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead																
		3	3*nRRD	repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 3** instead																
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRRD. Truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use **BG[1:0]**2 **= 0, BA[1:0] = 1** instead																
		6	nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0]**2 **= 1, BA[1:0] = 2** instead																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0]**2 **= 0, BA[1:0] = 3** instead																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0]**2 **= 1, BA[1:0] = 0** instead																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																

Note:

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

IDD Specifications

Table 130. Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol	DDR4-2666 (18-18-18)	DDR4-3200 (22-22-22)	Unit
tCK	0.75	0.625	ns
CL	18	22	CK
CWL	18	20	CK
nRCD	18	22	CK
nRC	61	74	CK
nRP	18	22	CK
nRAS	43	52	CK
nFAW	40	48	CK
nRRD_S	8	9	CK
nRRD_L	9	11	CK
tCCD_S	4	4	CK
tCCD_L	7	8	CK
tWTR_S	4	4	CK
tWTR_L	10	12	CK
nREFI	10,400	12,480	CK
nRFC 8Gb	467	560	CK

Current Specifications - Limits

Table 131. I_{DD}, I_{PP}, and I_{DDQ} Current Limits

Speed Grade Bin			Unit
Symbol	**DDR4-2666**	**DDR4-3200**	
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	55	59	mA
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	5	5	mA
I_{DD1}: One bank ACTIVATE-to-READ-to- PRECHARGE current	65	69	mA
I_{DD2N}: Precharge standby current	36	38	mA
I_{DD2NT}: Precharge standby ODT current	42	46	mA
I_{DD2P}: Precharge powerdown current	30	30	mA
I_{DD2Q}: Precharge quiet standby current	34	34	mA
I_{DD3N}: Active standby current	40	44	mA
I_{PP3N}: Active standby IPP current	3	3	mA
I_{DD3P}: Active power-down current	32	34	mA
I_{DD4R}: Burst read current	151	176	mA
I_{DD4W}: Burst write current	119	138	mA
I_{DD5R}: Distributed refresh current (1X REF)	45	47	mA
I_{PP5R}: Distributed refresh I_{PP} current (1X REF)	5	5	mA
I_{DD6N}: Self refresh current; 0–85°C	32	32	mA
I_{DD6E}: Self refresh current; 0–95°C	52	52	mA
I_{DD6R}: Self refresh current; 0–45°C	19	19	mA
I_{DD6A}: Auto self refresh current (25°C)	8	8	mA
I_{DD6A}: Auto self refresh current (45°C)	19	19	mA
I_{DD6A}: Auto self refresh current (75°C)	29	29	mA
I_{DD6A}: Auto self refresh current (95°C)	52	52	mA
I_{PP6x}: Auto self refresh I_{PP} current; 0–95°C	5	5	mA
I_{DD7}: Bank interleave read current	196	225	mA
I_{PP7}: Bank interleave read I_{PP} current	13	13	mA
I_{DD8}: Maximum power-down current	24	24	mA
I_{DD9}: MBIST-PPR current	170	170	mA
I_{PP9}: MBIST-PPR I_{PP} current	13	13	mA

Note:

1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. I_{DD6E}, I_{DD6R}, I_{DD6A} values are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately +1%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +5%.
7. When additive latency is enabled for I_{DD2N}, current changes by approximately +2%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately +19%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately -20%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately +2%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +10%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately -2%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +4%.
14. When read DBI is enabled for I_{DD4R}, current changes by approximately -14%.
15. When additive latency is enabled for I_{DD4W}, current changes by approximately +6%.
16. When write DBI is enabled for I_{DD4W}, current changes by approximately +1%.
17. When write CRC is enabled for I_{DD4W}, current changes by approximately -5%.
18. When CA parity is enabled for I_{DD4W}, current changes by approximately +14%.
19. When 2X REF is enabled for I_{DD5R}, current changes by approximately +0%.
20. When 4X REF is enabled for I_{DD5R}, current changes by approximately +0%.
21. When 2X REF is enabled for I_{PP5R}, current changes by approximately +0%.
22. When 4X REF is enabled for I_{PP5R}, current changes by approximately +0%.
23. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
24. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PPs} for the noted I_{DD} tests.
25. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133.
26. The I_{DD} values must be derated (increased) when operating between 85°C < $T_C \leqq$ 95°C:
    I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2P}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, and I_{DD4W} must be derated by +10%; and I_{DD5R} and I_{PP5R} must be derated by +43%; I_{PP0} must be derated by +13%. I_{PP3N} must be derated by +22%. I_{PP7} must be derated by +3%. These values are verified by design and characterization, and may not be subject to production test.
27. IPP6x is applicable to I_{DD6N}, I_{DD6E}, I_{DD6R} and I_{DD6A} conditions.

Speed Bin Tables

DDR4 DRAM timing is primarily covered by two types of tables: the Speed Bin tables in this section and the tables found in the Electrical Characteristics and AC Timing Parameters section. The timing parameter tables define the applicable timing specifications based on the speed rating. The Speed Bin tables on the following pages list the ^{t}AA, ^{t}RCD, ^{t}RP, ^{t}RAS, and ^{t}RC limits of a given speed mark and are applicable to the CL settings in the lower half of the table provided they are applied in the correct clock range, which is noted.

Speed Bin

Table 132. DDR4-2666 Speed Bins and Operations

Speed Bin				DDR4-2666		Unit
CL-nRCD-nRP				18-18-18		
Parameter			Symbol	min	max	
Internal read command to first data			tAA	13.50	19.00 *6	ns
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns
ACT to internal read or write delay time			tRCD	13.50	-	ns
PRE command period			tRP	13.50	-	ns
ACT to PRE command period			tRAS	32	9 x tREFI	ns
ACT to ACT or REF command period			tRC *5	tRAS + tRP	-	ns
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5	1.9 *6	ns
	CL = 10	CL = 12	tCK(AVG)	1.5	1.9 *6	ns
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns
CWL = 11,14	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns
CWL = 12,16	CL = 16	CL = 19	tCK(AVG)	Reserved		ns
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns
CWL = 14,18	CL = 18	CL = 21	tCK(AVG)	0.75	<0.833	ns
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns
Supported CL Settings				9-20		nCK
Supported CL Settings with read DBI				11-16,18-23		nCK
Supported CWL Settings				9-12,14,16,18		nCK

Note:

1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native tCK-CL-*n*RCD-*n*RP combinations.
5. When calculating tRC in clocks, values may not be used in a combination that violate tRAS or tRP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 133. DDR4-3200 Speed Bins and Operations

Speed Bin				DDR4-3200		Unit
CL-nRCD-nRP				22-22-22		
Parameter			Symbol	min	max	
Internal read command to first data			tAA	13.75	19.00 *6	ns
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 4nCK	tAA(max) + 4nCK	ns
ACT to internal read or write delay time			tRCD	13.75	-	ns
PRE command period			tRP	13.75	-	ns
ACT to PRE command period			tRAS	32	9 x tREFI	ns
ACT to ACT or REF command period			tRC	tRAS + tRP	-	ns
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns
	CL = 10	CL = 12	tCK(AVG)	1.5	1.9 *6	ns
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns
CWL = 11,14	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns
CWL = 12,16	CL = 16	CL = 19	tCK(AVG)	Reserved		ns
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns
CWL = 14,18	CL = 18	CL = 21	tCK(AVG)	Reserved		ns
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns
CWL = 16,20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns
	CL = 21	CL = 25	tCK(AVG)	0.682	<0.75	ns
	CL = 22	CL = 26	tCK(AVG)	0.682	<0.75	ns
	CL = 24	CL = 28	tCK(AVG)	0.682	<0.75	ns
CWL = 16,20	CL = 22	CL = 26	tCK(AVG)	0.625	<0.682	ns
	CL = 24	CL = 28	tCK(AVG)	0.625	<0.682	ns
Supported CL Settings				10–22,24		nCK
Supported CL Settings with read DBI				12–16,18–23,25-26,28		nCK
Supported CWL Settings				9–12,14,16,18,20		nCK

Note:

1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2tCK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native tCK-CL-*n*RCD-*n*RP combinations.
5. When calculating tRC in clocks, values may not be used in a combination that violate tRAS or tRP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Refresh Parameters By Device Density

Table 134. Refresh Parameters by Device Density

Parameter	Symbol		8 Gb	Unit
REF command to ACT or REF	tRFC (All bank groups)		350	ns
Average periodic refresh interval	tREFI	0℃ ≦ T_C ≦ 85℃	7.8	us
		85℃ < T_C ≦ 95℃	3.9	us

Electrical Characteristics and AC Timing Parameters: 2666 Through 3200

Table 135. Electrical Characteristics and AC Timing Parameters

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	tCK(avg, DLL_OFF)	8	20	8	20	ns	
Average Clock Period	tCK(avg DLL_ON)	0.75	1.9	0.625	1.9	ns	3,13
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	MIN = tCK(avg)min + tJIT(per)min_tot MAX = tCK(avg)max + tJIT(per)max_tot				ps	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	tCK(avg)	
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	tCK(avg)	
Clock Period Jitter-total	JIT(per)_tot	-38	38	-32	32	ps	17,18
Clock Period Jitter-deterministic	JIT(per)_dj	-19	19	-16	16	ps	17
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-30	30	-25	25	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_tot	-	75	-	62	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	60	-	62	ps	
Cumulative error across 2 cycles	tERR(2per)	-55	55	-46	46	ps	
Cumulative error across 3 cycles	tERR(3per)	-66	66	-55	55	ps	
Cumulative error across 4 cycles	tERR(4per)	-73	73	-61	61	ps	
Cumulative error across 5 cycles	tERR(5per)	-78	78	-65	65	ps	
Cumulative error across 6 cycles	tERR(6per)	-83	83	-69	69	ps	
Cumulative error across 7 cycles	tERR(7per)	-87	87	-73	73	ps	
Cumulative error across 8 cycles	tERR(8per)	-91	91	-76	76	ps	
Cumulative error across 9 cycles	tERR(9per)	-94	94	-78	78	ps	
Cumulative error across 10 cycles	tERR(10per)	-96	96	-80	80	ps	

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
Cumulative error across 11 cycles	tERR(11per)	-99	99	-83	83	ps	
Cumulative error across 12 cycles	tERR(12per)	-101	101	-84	84	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)				ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	55	-	40	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	145	-	130	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	80	-	65	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	145	-	130	-	ps	
Control and Address Input pulse width for each input	tIPW	385	-	340	-	ps	
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	CK	
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(4nCK, 5ns)	-	Max(4nCK, 5ns)	-	CK	14

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	CK	1
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	CK	1
Four activate window for 2KB page size	tFAW_2K	Max (28nCK,30ns)	-	Max (28nCK,30ns)	-	ns	
WRITE recovery time	tWR_{1CK}	MIN = 15ns				ns	1,5,9
	tWR_{2CK}	MIN = 1CK + tWR_{1ck}				CK	1,5,10
Write recovery time when CRC and DM are enabled	tWR_CRC _DM_{1CK}	MIN = tWR_{1ck} + greater of (5CK or 3.75ns)				CK	1,6,9
	tWR_CRC _DM_{2CK}	MIN = 1CK + $tWR\_CRC\_DM_{1ck}$				CK	1,6,10
Delay from start of internal write transaction to internal read command for same bank group	$tWTR\_L_{1CK}$	MIN = greater of 4CK or 7.5ns				CK	1,5,9
	$tWTR\_L_{2CK}$	MIN = 1CK + $tWTR\_L_{1ck}$				CK	1,5,10
Delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CR C_DM_{1CK}	MIN = tWTR_L1ck + greater of (5CK or 3.75ns)				CK	1,6,9
	tWTR_L_CR C_DM_{2CK}	MIN = 1CK + $tWTR\_L\_CRC\_DM_{1ck}$				CK	1,6,10
Delay from start of internal write transaction to internal read command for different bank group	$tWTR\_S_{1CK}$	MIN = greater of (2CK or 2.5ns)				CK	
	$tWTR\_S_{2CK}$	MIN = 1CK + $tWTR\_S_{1ck}$				CK	
Delay from start of internal write transaction to internal read command for different bank groups with both CRC and DM enabled	tWTR_S_CR C_DM_{1CK}	MIN = $tWTR\_S_{1ck}$ + greater of (5CK or 3.75ns)				CK	1,6-9
	tWTR_S_CR C_DM_{2CK}	MIN = 1CK + $tWTR\_S\_CRC\_DM_{1ck}$				CK	1,6-8, 10
Internal READ Command to PRECHARGE Command delay	tRTP	MIN = greater of 4CK or 7.5ns				CK	1

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
Clock Timing							
DLL locking time	tDLLK	854	-	1024	-	CK	2,4
Mode Register Set command cycle time	tMRD	8	-	8	-	CK	
MRS command cycle time in PDA mode	tMRD_PDA	MIN = greater of (16nCK, 10ns)				CK	1
MRS command cycle time in CAL mode	tMRD_CAL	MIN = tMOD + tCAL				CK	
Mode Register Set command update delay	tMOD	MIN = greater of (24nCK, 15ns)				CK	1
MRS command update delay in PDA mode	tMOD_PDA	MIN = tMOD				CK	
MRS command update delay in CAL mode	tMOD_CAL	MIN = tMOD + tCAL				CK	
MRS command to DQS drive in preamble training	tSDO	MIN = tMOD + 9ns				CK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	CK	
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	CK	
Auto precharge write recovery + precharge time	tDAL(min)	MIN = WR + ROUNDtRP/tCK (AVG); MAX = N/A				CK	8
Data setup time to DQS_t, DQS_c	tPDA_S	0.5	-	0.5	-	UI	22
Data hold time from DQS_t, DQS_c	tPDA_H	0.5	-	0.5	-	UI	22
CS_n to Command Address Latency							
CS_n to Command Address Latency	tCAL	5	-	6	-	CK	19
CS_n to command address latency in gear-down mode	tCALg	6	-	8	-	CK	

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
DRAM Data Timing							
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.18	-	0.20	UI	
DQ output hold time per group, per access from DQS_t,DQS_c	tQH	0.74	-	0.70	-	UI	
Data Valid Window per device per UI : (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.64	-	0.64	-	UI	
Data Valid Window per pin per UI : (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.72	-	0.72	-	UI	
DQ low impedance time from CK_t, CK_c	tLZDQ	-310	170	-250	160	ps	
DQ high impedance time from CK_t, CK_c	tHZDQ	-	170	-	160	ps	
Data Strobe Timing							
DQS_t, DQS_c differential READ Preamble (1 clock preamble)	$tRPRE_{1ck}$	0.9	-	0.9	-	CK	20
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	$tRPRE_{2ck}$	1.8	-	1.8	-	CK	20
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	-	0.33	-	CK	21
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	CK	
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	CK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZDQS	-310	170	-250	160	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZDQS	-	170	-	160	ps	

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	Symbol	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	CK	
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	$tWPRE_{1ck}$	0.9	-	0.9	-	CK	
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	$tWPRE_{2ck}$	1.8	-	1.8	-	CK	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	CK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	CK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	$tDQSS_{1ck}$	-0.27	0.27	-0.27	0.27	CK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	$tDQSS_{2ck}$	-0.50	0.50	-0.50	0.50	CK	
DQS_t, DQS_c differential input high pulse width for 2tCK preamble	tDQSH2PRE	1.46	-	1.46	-	CK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	$tDSS_{1ck}$	0.18	-	0.18	-	CK	
	$tDSS_{2ck}$	0	-	0	-	CK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	$tDSH_{1ck}$	0.18	-	0.18	-	CK	
	$tDSH_{2ck}$	0	-	0	-	CK	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	tDQSCK	-170	170	-160	160	ps	
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI	-	270	-	260	ps	

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
MPSM Timing							
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	CK	1
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	CK	1
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	CK	1
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	CK	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	CK	1
CS setup time to CKE	tMPX_S	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	ns	
CS_n HIGH hold time to CKE rising edge	tMPX_HH	tXP	-	tXP	-	ns	
CS_n LOW hold time to CKE rising edge	tMPX_LH	12	tXMP-10ns	12	tXMP-10ns	ns	
Calibration Timing							
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	CK	
Normal operation Full calibration time	tZQoper	512	-	512	-	CK	
Normal operation Short calibration time	tZQCS	128	-	128	-	CK	
Reset/Self Refresh Timing							
Exit Reset from CKE HIGH to a valid command	tXPR	MIN = tRFC1 + 10ns				ns	1
Begin power supply ramp to power supplies stable	tVDDPR	MIN = N/A; MAX = 200				ms	
RESET_n LOW to power supplies stable	tRPS	MIN = 0; MAX = 0				ns	
Exit Self Refresh to commands not requiring a locked DLL	tXS	MIN = tRFC1 + 10ns				ns	1

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT (min)	MIN = tRFC4 + 10ns				ns	1
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	MIN = tRFC4 + 10ns				ns	1
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	MIN = tDLLK (MIN)				CK	1
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	MIN = tCKE (MIN) + 1*n*CK				CK	1
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	MIN = tCKE (MIN) + 1*n*CK + PL				CK	1
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	MIN = greater of (5CK, 10ns)				CK	1
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	MIN = greater of (5CK, 10ns) + PL				CK	1
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	MIN = greater of (5CK, 10ns)				CK	1
Power Down Timing							
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	MIN = greater of 4CK or 6ns				CK	1

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
Exit precharge power-down with DLL frozen to commands not requiring a locked DLL when CA Parity is enabled.	tXP _PAR	MIN = (greater of 4CK or 6ns) + PL				CK	1
CKE minimum pulse width	tCKE	MIN = greater of 3CK or 5ns				CK	1
Command pass disable delay	tCPDED	4	-	4	-	CK	
Power Down Entry to Exit Timing	tPD	MIN = tCKE (MIN); MAX = 9 x tREFI				CK	
Begin power-down period prior to CKE registered HIGH	tANPD	WL - 1CK				CK	
Power-down entry period: ODT either synchronous or asynchronous	PDE	Greater of tANPD or tRFC - REFRESH command to CKE LOW time				CK	
Power-down exit period: ODT either synchronous or asynchronous	PDX	tANPD + tXSDLL				CK	
Timing of ACT command to Power Down entry	tACTPDEN	2	-	2	-	CK	
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	2	-	CK	
Timing of REF command to Power Down entry	tREFPDEN	2	-	2	-	CK	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	CK	1
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	CK	1
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	CK	1
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	CK	1

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	MIN = WL + 2 + tWR/tCK (AVG)				CK	1
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	MIN = WL + 2 + WR + 1				CK	1
ODT Timing							
Direct ODT turn-on latency	DODTLon	WL - 2 = CWL + AL + PL - 2				CK	
Direct ODT turn-off latency	DODTLoff	WL - 2 = CWL + AL + PL - 2				CK	
RTT dynamic change skew	tADC	0.28	0.72	0.26	0.74	CK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1	9	1	9	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1	9	1	9	ns	
ODT HIGH time with WRITE command and BL8	ODTH8 1^{t}CK	6	-	6	-	CK	
	ODTH8 2^{t}CK	7	-	7	-		
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4 1^{t}CK	4	-	4	-	CK	
	ODTH4 2^{t}CK	5	-	5	-		
Write Leveling Timing							
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	CK	
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	CK	
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/ DQS_n crossing	tWLS	0.13	-	0.13	-	CK	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	CK	

Speed		DDR4-2666		DDR4-3200		Unit	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**		
Write leveling output delay	tWLO	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	
CA Parity Timing							
Commands not guaranteed to be executed during this time	tPAR _UNKNOWN	-	PL	-	PL	CK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT _ON	-	PL+6ns	-	PL+6ns	CK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT _PW	80	160	96	192	CK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT _RSP	-	71	-	85	CK	
Parity Latency	PL	5	-	6	-	CK	
CRC Error Reporting							
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT _PW	6	10	6	10	CK	
Geardown timing							
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	tXPR	-	tXPR	-	CK	
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	tXS	-	tXS	-	CK	
MRS command to Sync pulse time(T3)	tSYNC_GEA R	tMOD+4nCK	-	tMOD+4nCK	-	CK	
Sync pulse to First valid command(T4)	tCMD_GEAR	tMOD	-	tMOD	-	CK	
Geardown setup time	tGEAR_setup	2	-	2	-	CK	
Geardown hold time	tGEAR_hold	2	-	2	-	CK	
tREFI							
tRFC1 (min)	8Gb	350	-	350	-	ns	1,11
tRFC2 (min)	8Gb	260	-	260	-	ns	1,11
tRFC4 (min)	8Gb	160	-	160	-	ns	1,11

Note:

1. Maximum limit not applicable.
2. tDLLK values support the legacy JEDEC tDLLK specifications.
3. DDR4-1600 AC timing parameters apply if DRAM operates at lower than 1600 MT/s data rate.
4. Data rate is greater than or equal to 1066 Mb/s.
5. WRITE-to-READ when CRC and DM are both not enabled.
6. WRITE-to-READ delay when CRC and DM are both enabled.
7. The start of internal write transactions is defined as follows:
   - For BL8 (fixed by MRS and on-the-fly): rising clock edge four clock cycles after WL
   - For BC4 (on-the-fly): rising clock edge four clock cycles after WL
   - For BC4 (fixed by MRS): rising clock edge two clock cycles after WL
8. For these parameters, the device supports t*n*PARAM [*n*CK] = ROUND{tPARAM [ns]/tCK (AVG) [ns]} according to the rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section, in clock cycles, assuming all input clock jitter specifications are satisfied.
9. When operating in 1^{t}CK WRITE preamble mode.
10. When operating in 2^{t}CK WRITE preamble mode.
11. When CA parity mode is selected and the DLLoff mode is used, each REF command requires an additional "PL" added to tRFC refresh time.
12. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime and/or reduction in data retention ability.
13. Applicable from tCK (AVG) MIN to tCK (AVG) MAX as stated in the Speed Bin tables.
14. JEDEC specifies a minimum of five clocks.
15. The maximum read postamble is bound by tDQSCK (MIN) plus tQSH (MIN) on the left side and tHZ(DQS) MAX on the right side.
16. The reference level of DQ output signal is specified with a midpoint as a widest part of output signal eye, which should be approximately 0.7 x VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ.
17. JEDEC hasn't agreed upon the definition of the deterministic jitter; the user should focus on meeting the total limit.
18. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20-60 kHz with an additional 1% of tCK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below tCK (AVG) MIN.
19. The actual tCAL minimum is the larger of 3 clocks or 3.748ns/tCK; the table lists the applicable clocks required at targeted speed bin.
20. The maximum READ preamble is bounded by tLZ(DQS) MIN on the left side and tDQSCK (MAX) on the right side. See figure in the Clock to Data
21. Strobe Relationship section. Boundary of DQS Low-Z occurs one cycle earlier in 2tCK toggle mode, as illustrated in the READ Preamble section.
22. DQ falling signal middle-point of transferring from HIGH to LOW to first rising edge of DQS differential signal cross-point.
23. The tPDA_S/tPDA_H parameters may use the tDS/tDH limits, respectively, if the signal is LOW the entire BL8.

Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject t o production test.

Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$\mathrm{tCK(avg)} = \left(\sum_{\mathrm{j=1}}^{\mathrm{N}} \mathrm{tCK(avg)j}\right)/N \qquad N = 200$$

Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$\mathrm{tCH(avg)} = \left(\sum_{\mathrm{j=1}}^{\mathrm{N}} \mathrm{tCHj}\right)/\{N \times \mathrm{tCK(avg)}\} \qquad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$\mathrm{tCL(avg)} = \left(\sum_{\mathrm{j=1}}^{\mathrm{N}} \mathrm{tCLj}\right)/\{N \times \mathrm{tCK(avg)}\} \qquad N = 200$$

Definition for tERR(nper)

tERR is defined as the cumulative error across n consecutive cycles of n x tCK(avg). tERR is not subject to production test.

Definition for tJIT(per) and tJIT(per,lck)

tJIT(per) is defined as the largest deviation of any signal tCK from tCK(AVG).
tJIT(per) = MIN/MAX of {tCKi - tCK(AVG) where i = 1 to 200}.
tJIT(per) defines the single period jitter when the DLL is already locked.
tJIT(per,lck) uses the same definition for single period jitter, but only during the DLL locking period.
tJIT(per) and tJIT(per,lck) are not subject to production test.

Definition for tJIT(cc) and tJIT(cc,lck)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.
tJIT(cc) = MAX of |{tCKi +1 - tCKi}|.
tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
tJIT(cc) and tJIT(cc,lck) are not subject to production test.

Jitter Notes

Note a: Unit tCK(AVG) represents the actual tCK(AVG) of the input clock under operation. Unit *n*CK represents one clock cycle of the input clock, including the actual clock edges. Example: tMRD = 4 [*n*CK] means that if one MODE REGISTER SET command is registered at Tm, another MODE REGISTER SET command may be registered at Tm + 4, even if (Tm + 4 - Tm) is (4 tCK(AVG) + tERR (4 per) MIN).

Note b: These parameters are measured from a command/address signal (such as CKE, CS_n, RAS_n, CAS_n, WE_n, ODT, BA0, A0, or A1) transition edge to its respective clock signal (CK_t/CK_c) crossing.

The specification values are not affected by the amount of clock jitter applied (for example, tJITper, tJITcc) because the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Note c: These parameters are measured from a data strobe signal (DQS_t[L/U], DQS_c[L/U]) crossing to its respective clock signal (CK_t, CK_c) crossing. The specification values are not affected by the amount of clock jitter applied (for example, tJITper, tJITcc) because these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Note d: These parameters are measured from a data signal (such as DM[L/U], DQ[L/U]0, or DQ[L/U]1) transition edge to its respective data strobe signal (DQS_t[L/U], DQS_c[L/U]) crossing.

Note e: For these parameters, the DDR4 SDRAM device supports t*n*PARAM [*n*CK] = RU[tPARAM [ns]/tCK(AVG) [ns]], which is in clock cycles, assuming all input clock jitter specifications are satisfied.

For example, the device will support t*n*RP = RU [tRP/tCK(AVG)], which is in clock cycles, if all input clock jitter specifications are met. This means that for DDR4-800 6-6-6, tRP = 15ns, the device will support t*n*RP = RU[tRP/tCK(AVG)] = 6, as long as the input clock jitter specifications are met. For example, the PRECHARGE command at Tm and ACTIVE command at Tm + 6 is valid even if (Tm + 6 - Tm) is less than 15ns due to input clock jitter.

Note f: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper), act of the input clock, where 2 *m* 12 (output deratings are relative to the SDRAM input clock). For example, if the measured jitter into a DDR4-800 SDRAM has tERR(mper), act, MIN = -172ps and tERR(mper), act, MAX = +193ps, then tDQSCK, MIN(derated) = tDQSCK, MIN - tERR(mper), act, Max = -400ps = 193ps = -593ps and tDQSCK, MAX(derated) = tDQSCK, MAX - tERR(mper), act, MIN = 400ps + 172ps = 572ps. Similarly, tLZ(DQ) for DDR4-800 derates to tLZ(DQ), MIN(derated) = -800ps -193ps = -993ps and tLZ(DQ), MAX(derated) = 400ps + 172ps = 572ps. Note that tERR(mper), act, MIN is the minimum measured value of tERR(nper) where 2 $\leqq n \leqq$ 12, and tERR(mper), act, MAX is the maximum measured value of tERR(nper) where 2 $\leqq n \leqq$ 12.

Note g: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per), act of the input clock (output deratings are relative to the SDRAM input clock). For example, if the measured jitter into a DDR4-800 SDRAM has tCK(AVG), act = 2500ps, tJIT(per), act, MIN = -72ps and tJIT(per), act, MAX = +93ps, then tRPRE, MIN(derated) = tRPRE, MIN + tJIT(per), act, MIN = 0.9 x tCK(AVG), act + tJIT(per), act, MIN = 0.9 x 2500ps - 72ps = 2178ps. Similarly, tQH, MIN(derated) = tQH, MIN + tJIT(per), act, MIN = 0.38 x tCK(AVG), act + tJIT(per), act, MIN = 0.38 x 2500ps - 72ps = 878ps.

Converting Time-Based Specifications to Clock-Based Requirements

Software algorithms for calculation of timing parameters are subject to potential rounding errors when converting DRAM timing requirements to system clocks; for example, a memory clock with a nominal frequency of 933.33...3 MHz which yields a clock period of 1.071428571429...ns. It is unrealistic to represent all digits after the decimal point exactly and some sort of rounding needs to be done.

DDR4 SDRAM SPD-based specifications use a minimum granularity for SPD-associated timing parameters of 1ps. Clock periods such as tCK (AVG) MIN are defined to the nearest picosecond. For example, 1.071428571429...ns is stated as 1071ps. Parameters such as tAA MIN are specified in units of time (nanoseconds) and require mathematical computation to convert to system clocks (*n*CK). Rules for rounding allow optimization of device performance without violating device parameters. These SPD algorithms rely on results that are within *n*CK adjustment factors on device testing and specification to avoid losing performance due to rounding errors when using SPD-based parameters. Note that JEDEC also defines an *n*CK adjustment factor, but mandates the inverse *n*CK adjustment factor be used in case of conflicting results, so only the inverse *n*CK adjustment factor is discussed here.

Guidance converting SPD associated timing parameters to system clock requirements:

- Round the application clock period up to the nearest picosecond.
- Express the timing specification and application clock period in picoseconds; scaling a nanosecond-based parameter value by 1000 allows programmers to use integer math instead of real math by expressing timing in ps.
- Divide the picosecond-based parameter by the picoseconds based application clock period.
- Add an inverse *n*CK adjustment factor of 97.4%.
- Truncate down to the next lower integer value.
- *n*CK = Truncate[(parameter in ps)/(application tCK in ps) + (974/1000)].

Guidance converting nonSPD associated timing parameters to system clock requirements:

- Divide the time base specification (in ns) and divided by the clock period (in ns).
- The resultant is set to the next higher integer number of clocks.
- *n*CK = Ceiling[(parameter in ns/application tCK in ns)].

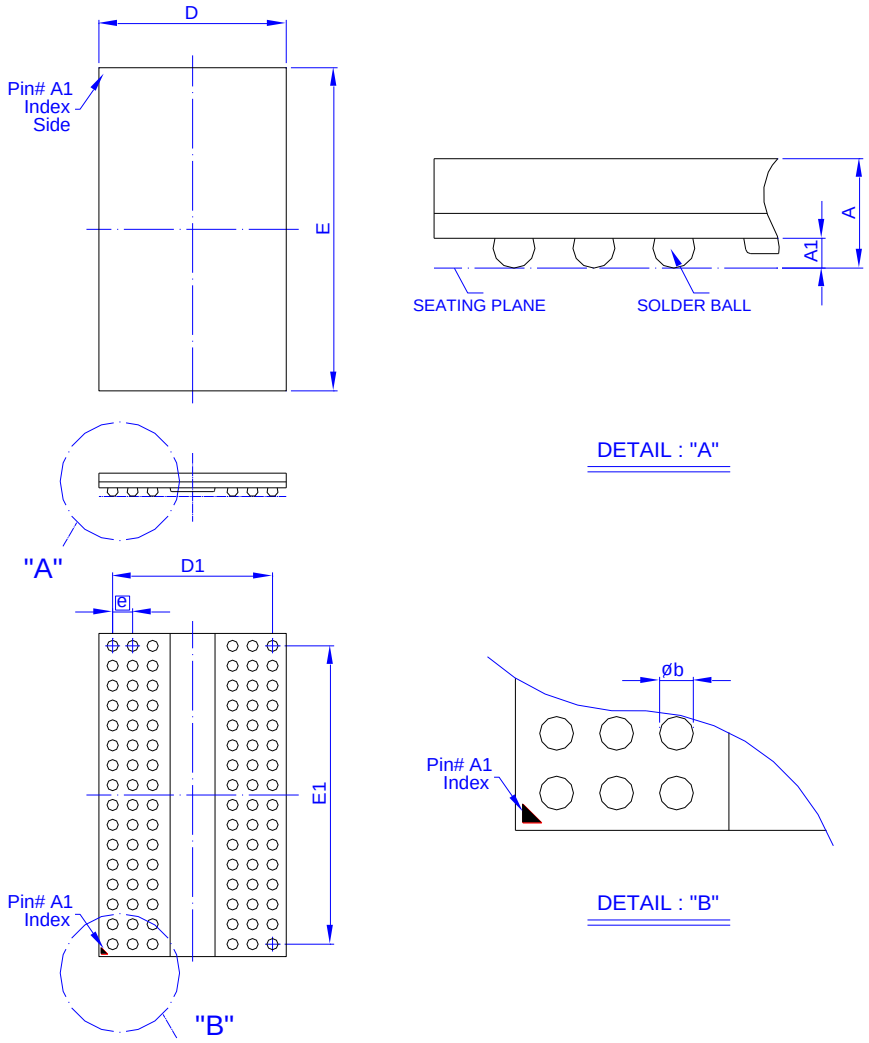
Options Tables

Table 136. Options – Width Based

Functions	Acronym	x16
Write Leveling	WL	Yes
Temperature controlled Refresh	TCR	Yes
Low Power Auto Self Refresh	LPASR	Yes
Fine Granularity Refresh	FGR	Yes
Multi Purpose Register	MR	Yes
Data Mask	DM	Yes
Data Bus Inversion	DBI	Yes
TDQS	-	**NO**
ZQ calibration	ZQ CAL	Yes
V_{REFDQ} Training	-	Yes
Per DRAM Addressability	Per DRAM	Yes
Mode Register Readout	-	Yes
CAL	CAL	Yes
WRITE CRC	CRC	Yes
CA Parity	-	Yes
Control Gear Down Mode	-	Yes
Programmable Preamble	-	Yes
Maximum power saving mode	MPSM	Yes
Additive Latency	AL	Yes
Connectivity test mode	CT	Yes
Hard post package repair mode	hPPR	Yes
Soft post package repair mode	sPPR	Yes
MBIST-PPR	MBIST-PPR	Yes

PACKING DIMENSIONS

Figure 232. 96-BALL DDR SDRAM (7.5x13 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.00	—	—	0.039
A_1	0.30	0.35	0.40	0.012	0.014	0.016
Φ_b	0.40	0.45	0.50	0.016	0.018	0.020
D	7.40	7.50	7.60	0.291	0.295	0.299
E	12.90	13.00	13.10	0.508	0.512	0.516
D_1	6.40 BSC			0.252 BSC		
E_1	12.00 BSC			0.472 BSC		
e	0.80 BSC			0.031 BSC		

Controlling dimension: Millimeter.

(Revision date: Nov172 2017)

Revision History

Revision	Date	Description
0.1	2023.08.23	Original
0.2	2023.12.12	Modify: TCR extended temperature mode related information removed
1.0	2024.03.12	Version upgrade (V1.0) / “Preliminary” deleted

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